



STE110NS20FD

N-channel 200V - 0.022Ω - 110A - ISOTOP
MESH OVERLAY™ Power MOSFET

General features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|--------------|------------------|---------------------|----------------|
| STE110NS20FD | 200V | <0.024Ω | 110A |

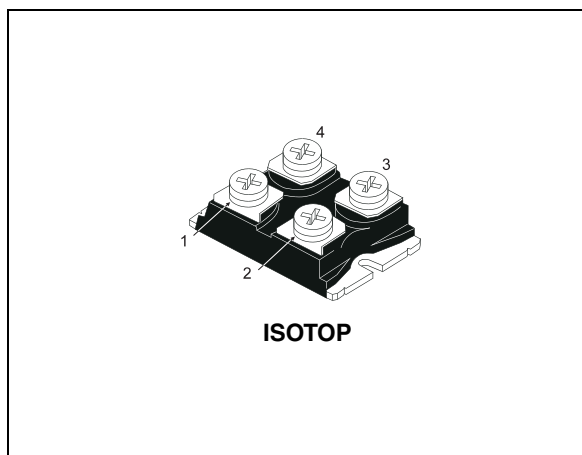
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- ± 20V gate to source voltage rating
- Low intrinsic capacitance
- Fast body-drain diode: low trr, Qrr

Description

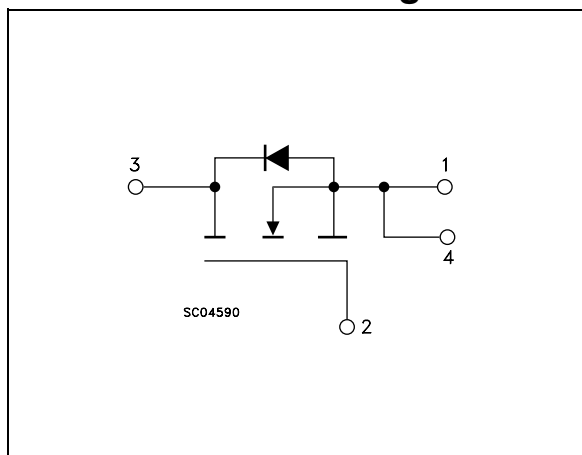
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The new patented STRip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(ON)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

Applications

- Switching application



Internal schematic diagram



Order codes

| Part number | Marking | Package | Packaging |
|--------------|------------|---------|-----------|
| STE110NS20FD | E110NS20FD | ISOTOP | Tube |

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1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|---------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 200 | V |
| V_{DGR} | Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$) | 200 | V |
| V_{GS} | Gate- source voltage | ± 20 | V |
| I_D | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 110 | A |
| I_D | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 69 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 440 | A |
| P_{TOT} | Total dissipation at $T_C = 25^\circ\text{C}$ | 500 | W |
| | Derating factor | 4 | W/ $^\circ\text{C}$ |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 25 | V/ns |
| V_{ISO} | Insulation withstand voltage (AC-RMS) | 2500 | V |
| T_{stg} | Storage temperature | -65 to 150 | $^\circ\text{C}$ |
| T_j | Max. operating junction temperature | 150 | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 110\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal resistance

| Symbol | Parameter | Value | Unit |
|----------------|--|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case Max | 0.25 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient Max | 30 | $^\circ\text{C}/\text{W}$ |
| T_l | Maximum lead temperature for soldering purpose | 300 | $^\circ\text{C}$ |

Table 3. Avalanche data

| Symbol | Parameter | Value | Unit |
|----------|---|-------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 110 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$) | 750 | mJ |

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|--|------|-------|-----------|----------|
| V _{(BR)DSS} | Drain-source breakdown voltage | I _D = 250μA, V _{GS} = 0 | 200 | | | V |
| I _{DSS} | Zero gate voltage drain current (V _{GS} = 0) | V _{DS} = Max rating V _{DS} = Max rating, @125°C | | | 10 100 | μA μA |
| I _{GSS} | Gate body leakage current (V _{DS} = 0) | V _{GS} = ± 20V | | | ±100 | nA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 250μA | 2 | 3 | 4 | V |
| R _{DS(on)} | Static drain-source on resistance | V _{GS} = 10V, I _D = 50A | | 0.022 | 0.024 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------------------|--|------|------|------|------|
| g _{fs} ⁽¹⁾ | Forward transconductance | V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 50A | | 30 | | S |
| C _{iss} | Input capacitance | V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 | | 7900 | | pF |
| C _{oss} | Output capacitance | | | 1500 | | pF |
| C _{rss} | Reverse transfer capacitance | | | 460 | | pF |
| Q _g | Total gate charge | V _{DD} = 100V, I _D = 100A, V _{GS} = 10V (see Figure 13) | | 360 | 504 | nC |
| Q _{gs} | Gate-source charge | | | 35 | | nC |
| Q _{gd} | Gate-drain charge | | | 135 | | nC |

1. Pulsed: pulse duration=300μs, duty cycle 1.5%

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---|--|------|-------------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on delay time Rise time | $V_{DD} = 100V, I_D = 50A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12) | | 40 130 | | ns ns |
| $t_{r(Voff)}$ t_f t_c | Off-voltage rise time Fall time Cross-over time | $V_{DD} = 100V, I_D = 100A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12) | | 245 140 220 | | ns ns ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|-----------------------------------|--|---|-----|-------------------|-----|--------------------|
| I_{SD} | Source-drain current | | | | 110 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 440 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 100A, V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD}=100A, T_j=150^\circ C$ $di/dt = 100A/\mu s,$ $V_{DD}=160V,$ (see Figure 17) | | 225 1.35 12 | | ns μC A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

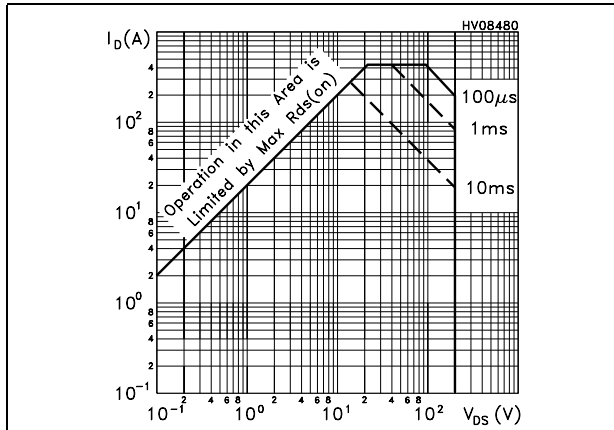


Figure 2. Thermal impedance

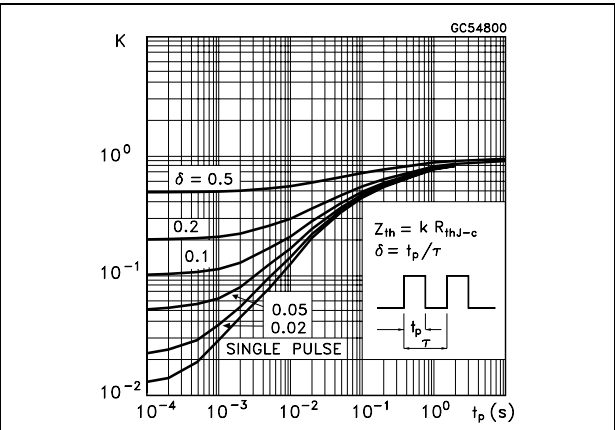


Figure 3. Output characteristics

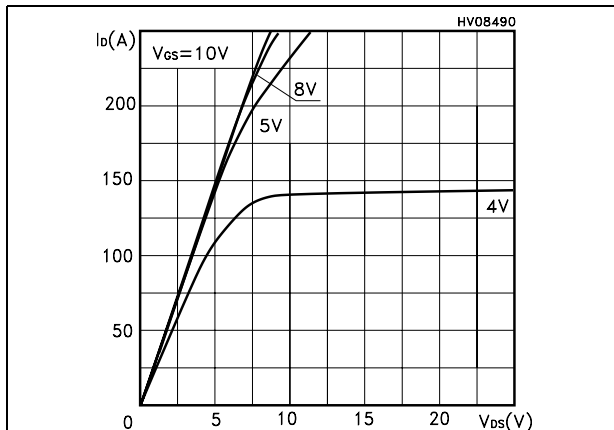


Figure 4. Transfer characteristics

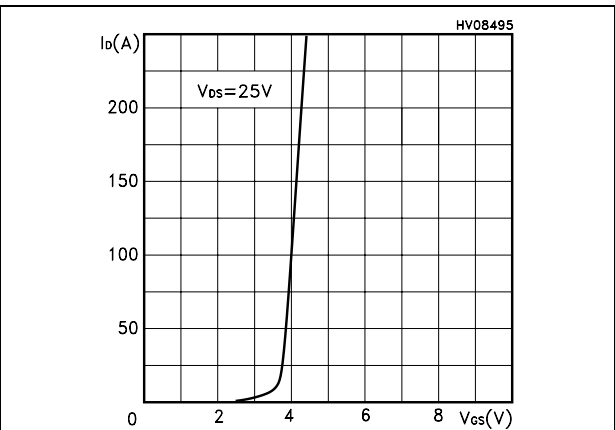


Figure 5. Transconductance

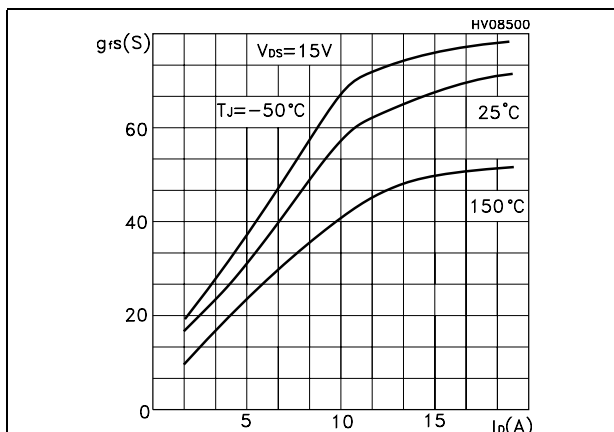


Figure 6. Static drain-source on resistance

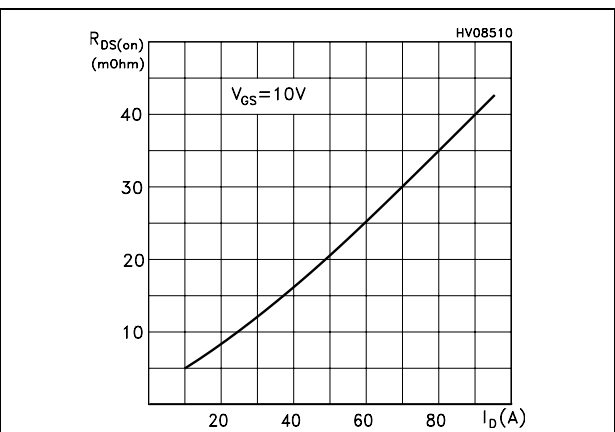


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

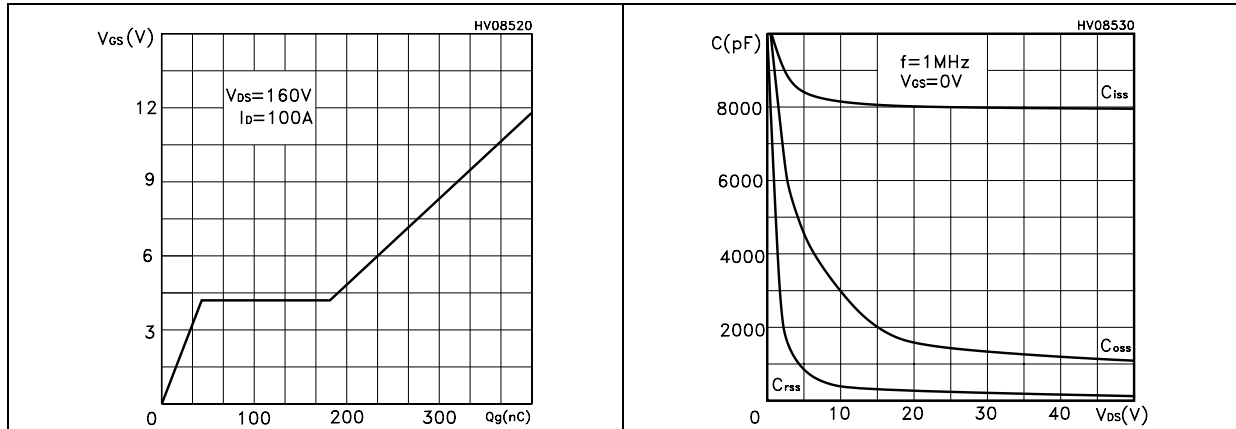


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

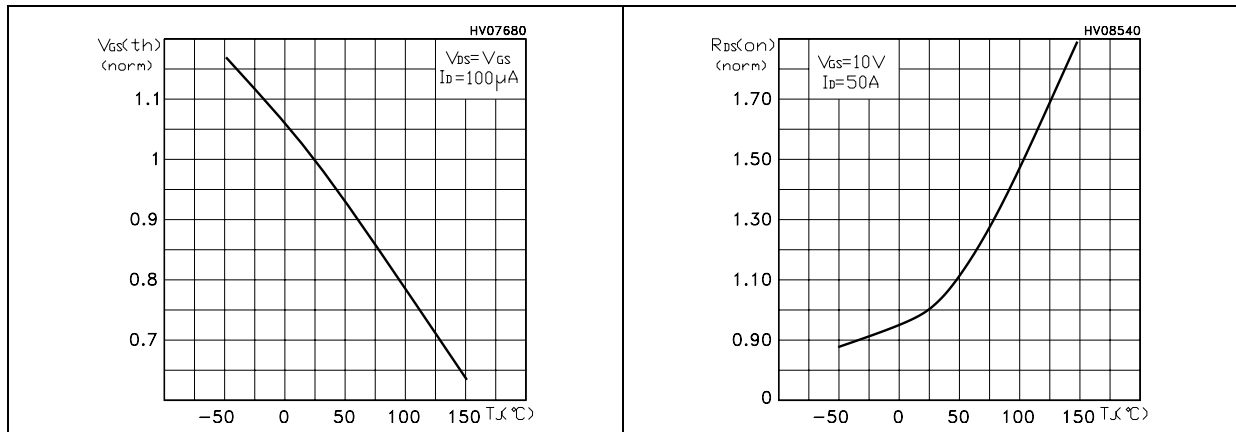
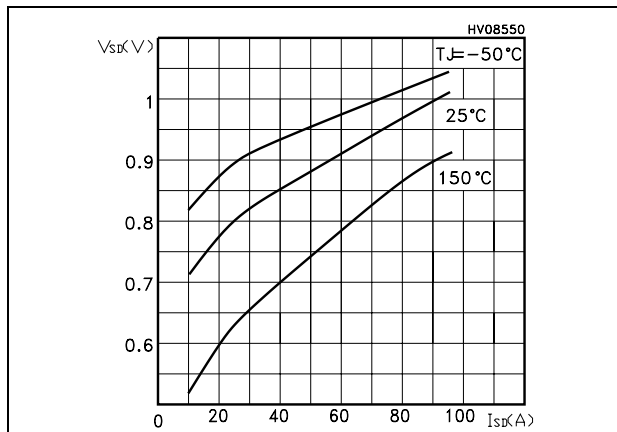


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

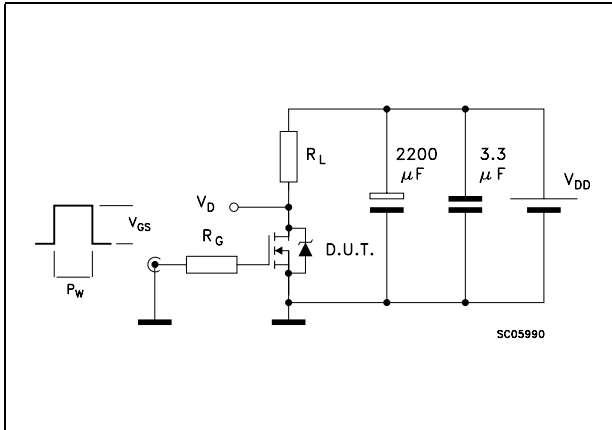


Figure 13. Gate charge test circuit

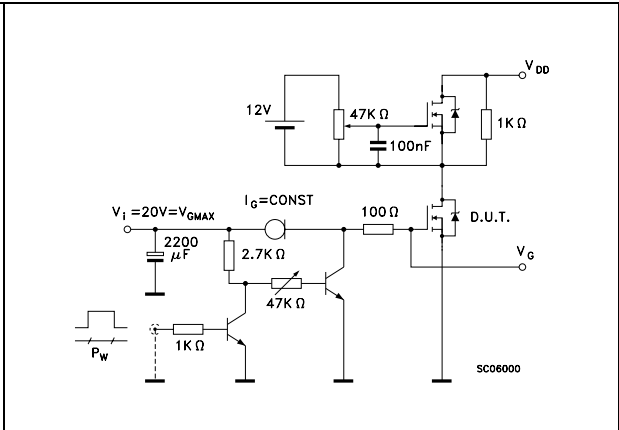


Figure 14. Test circuit for inductive load switching and diode recovery times

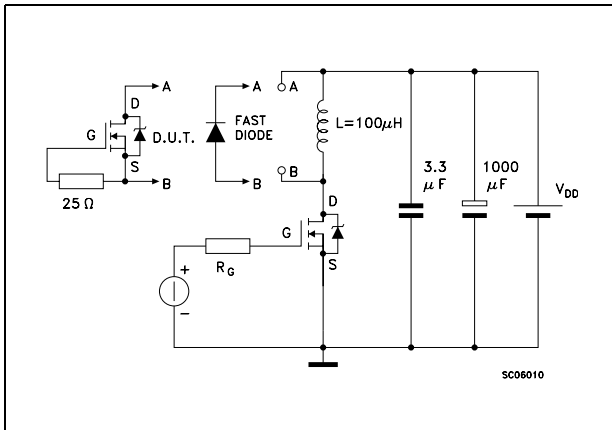


Figure 15. Unclamped inductive load test circuit

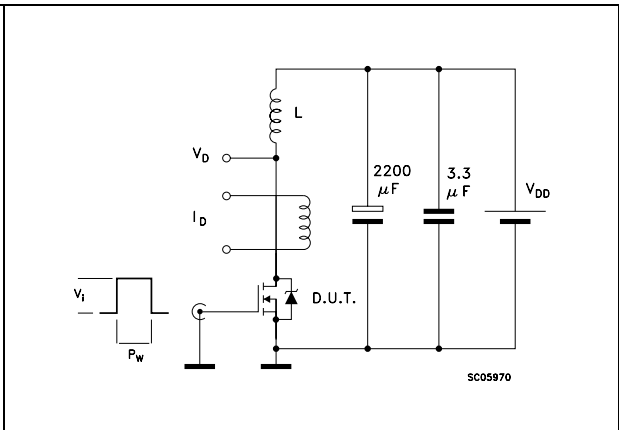


Figure 16. Unclamped inductive waveform

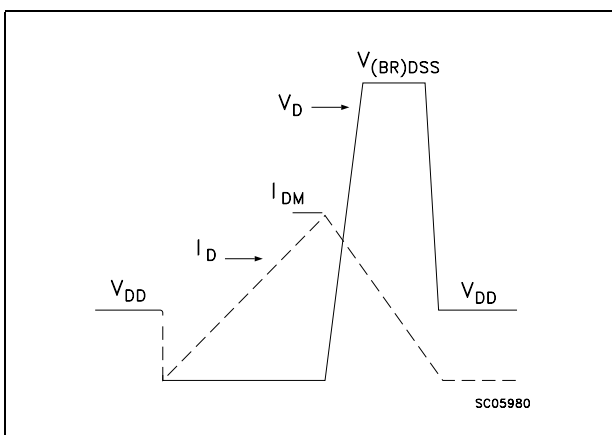
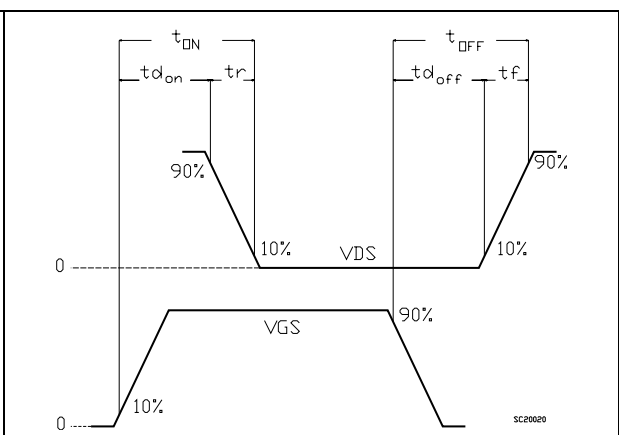


Figure 17. Switching time waveform

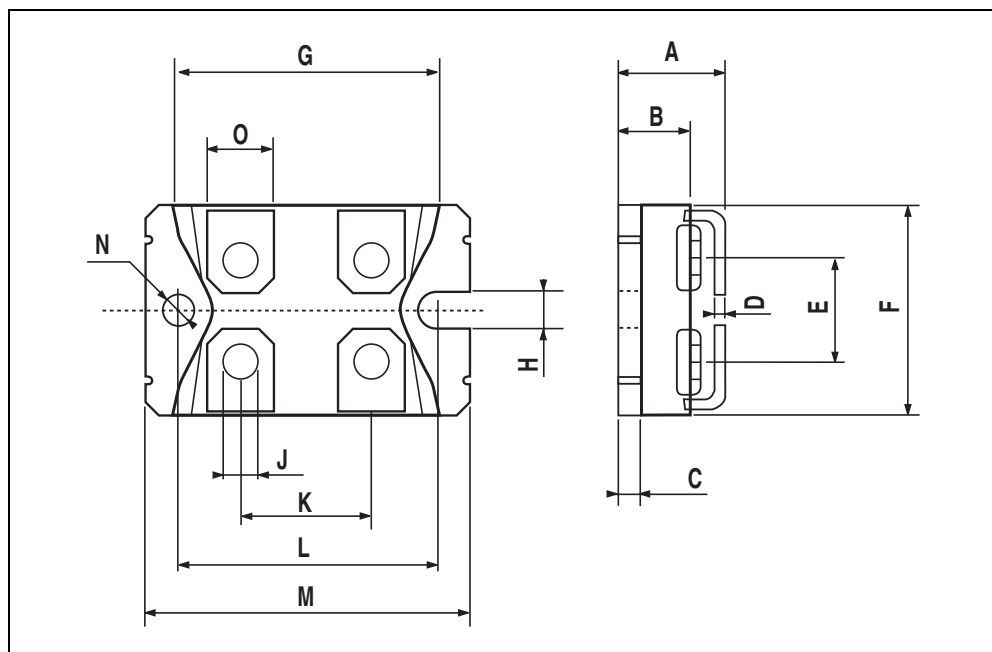


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

ISOTOP MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-------|------|------|-------|------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 11.8 | | 12.2 | 0.466 | | 0.480 |
| B | 8.9 | | 9.1 | 0.350 | | 0.358 |
| C | 1.95 | | 2.05 | 0.076 | | 0.080 |
| D | 0.75 | | 0.85 | 0.029 | | 0.033 |
| E | 12.6 | | 12.8 | 0.496 | | 0.503 |
| F | 25.15 | | 25.5 | 0.990 | | 1.003 |
| G | 31.5 | | 31.7 | 1.240 | | 1.248 |
| H | 4 | | | 0.157 | | |
| J | 4.1 | | 4.3 | 0.161 | | 0.169 |
| K | 14.9 | | 15.1 | 0.586 | | 0.594 |
| L | 30.1 | | 30.3 | 1.185 | | 1.193 |
| M | 37.8 | | 38.2 | 1.488 | | 1.503 |
| N | 4 | | | 0.157 | | |
| O | 7.8 | | 8.2 | 0.307 | | 0.322 |



5 Revision history

Table 8. Revision history

| Date | Revision | Changes |
|-------------|----------|--------------|
| 12-May-2006 | 3 | New template |

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