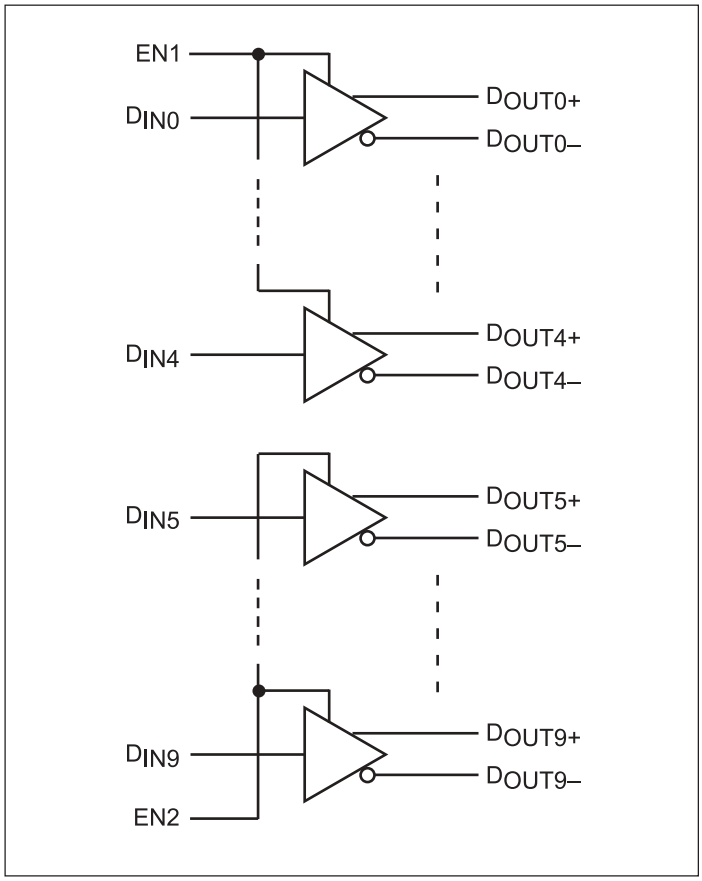
High-Speed Differential Line Drivers

Features

- Ten line drivers meet or exceed the requirements of the ANSI EIA/TIA-644 Standard
- Designed for signaling rates up to 660 Mbps with very low radiation (EMI)
- Low voltage differential signaling with typical output voltage of 350mV into a:
  100-ohm load (PI90LV3811)
  50-ohm load (PI90LVB3811)
- Propagation delay times less than 2.9ns
- Output skew is less than 150ps
- Part-to-part skew is less than 1.5ns
- 35mW total power dissipation in each driver operating at 200 MHz
- Driver is high impedance when disabled or with V_{CC} <1.5V
- Bus-pin ESD protection exceeds 10kV
- Low voltage TTL (LVTTL) logic inputs are 5V tolerant
- Package: 48-Pin TSSOP (A)

PI90LV3811 & PI90LVB3811



Description

The PI90LV3811 and PI90LVB3811 consist of ten differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers output voltage levels to reduce the power, increase switching speeds, and allow operation with a 3V supply rail. Any current-mode LVDS driver will deliver a minimum differential output voltage magnitude of 247mV into a 100-Ohm load (PI90LV3811) or 50-Ohm load (PI90LVB3811) when enabled. The PI90LVB3811 doubles the output drive current to achieve LVDS levels with a 50-Ohm load.

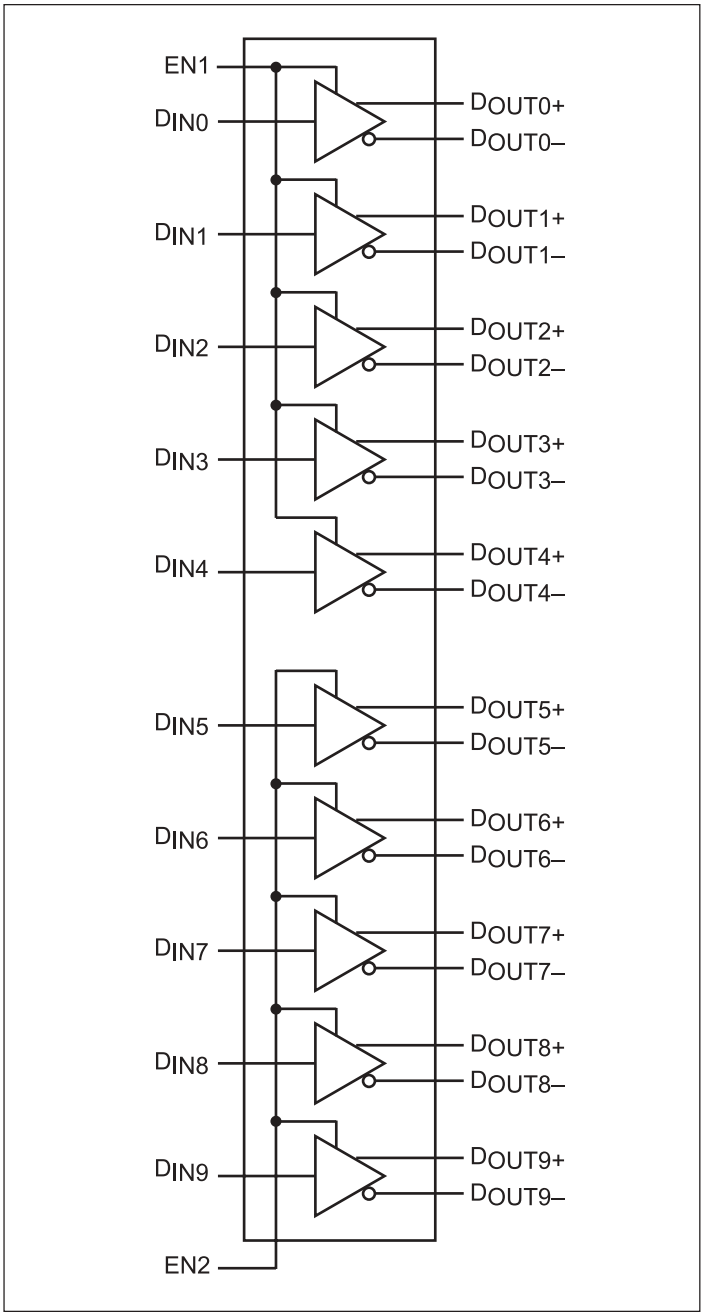
The intended application of this device and signaling technique is for point-to-point baseband (single termination) and multipoint (double termination) data transmission over a controlled impedance media of approximately 100-Ohms. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion 10-channel receivers, the PI90LV3810 or PI90LVR3810, over 300 million data transfers per second in single-edge clocked systems are possible with very little power.

(Note: The ultimate rate and distance of data transfer is dependent upon attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

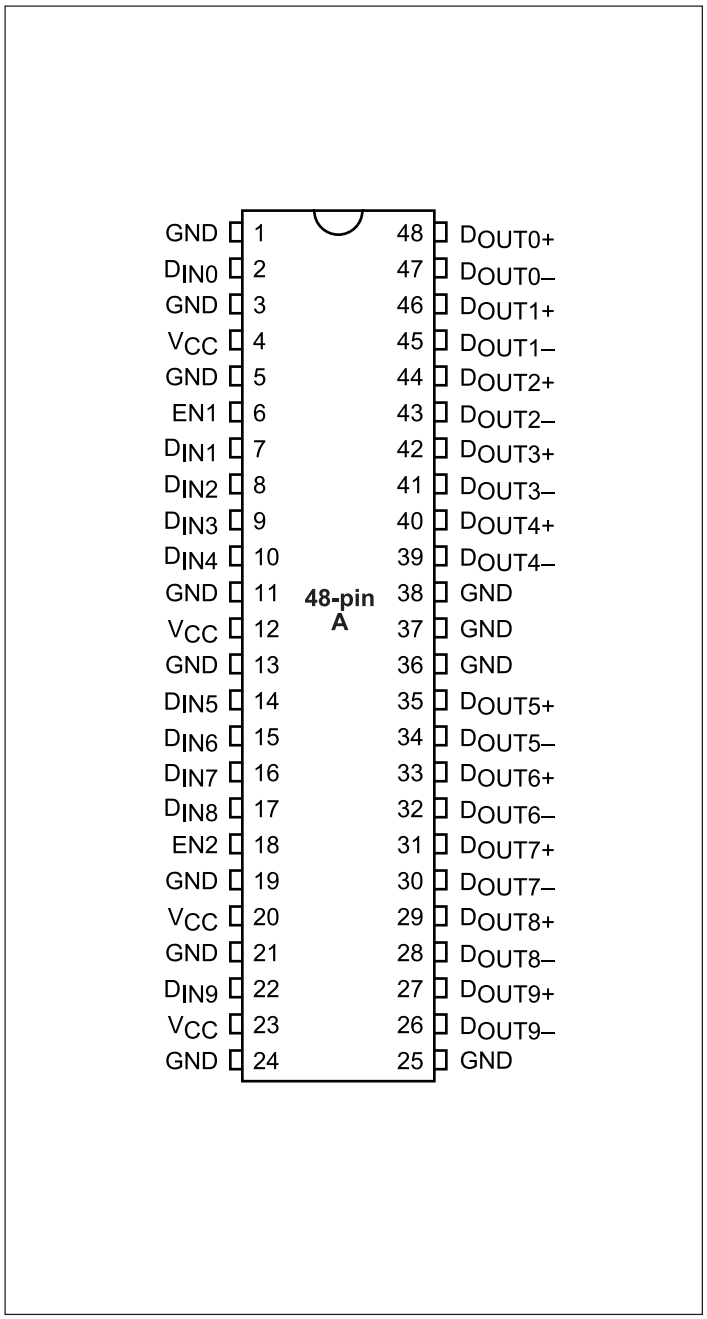
The drivers are enabled in groups of five. When disabled, the driver outputs are a high impedance. Each driver input (D_{IN}) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The PI90LV3811 and PI90LVB3811 are characterized for operation from –40°C to 85°C.

Block Diagram



Pin Configuration



Absolute Maximum Ratings Over Operating Free-Air Temperature (unless otherwise noted)†

Supply Voltage Range, V_{CC}(1) ..... –0.5V to 4V
Voltage Range: Inputs ..... –0.5V to 6V
D_{OUT+} or D_{OUT-} ..... –0.5V to 4V
Electrostatic Discharge(2):
(D_{OUT+},D_{OUT-} and GND) ..... Class 3, A: 10kV, B:700V
(All Pins) ..... Class 3, A: 8kV, B:600V
Continuous Power Dissipation .... (see dissipation rating table)
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature 1.6mm (1/16 inch)
from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:
1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

H = high level,
L = low level,
X = irrelevent,
Z = high impedance (off)

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
High-Level Input Voltage, V_{IH}	2.0			
Low-Level Input Voltage, V_{IL}			0.8	
Operating free-air temperature, T_A	–40		85	°C

Driver Function Table

Differential Input	Enables	Outputs	
D_{IN}	EN	D_{OUT+}	D_{OUT-}
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	L	H

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.(1)	Max.	Units
$\|V_{OH}\|$	Differential output voltage magnitude	R_L = 50-Ohm (PI90LVB3811) R_L = 100-Ohm (PI90LV3811) C_L = 10pF See Figures 1 and 2	247	340	454	mV
$\Delta\|V_{OH}\|$	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	
I_{CC}	Supply current	R_L = 100-Ohm (PI90LV3811) Enabled, V_{IN} = GND or V_{CC}		50	70	mA
		R_L = 50-Ohm (PI90LVB3811) Enabled, V_{IN} = GND or V_{DD}		77	120	
		Disabled, V_{IN} = GND or V_{DD}		0.5	1.5	
I_{IH}	High-level input current	V_{IN} = 2V		3	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8V		2	10	
I_{OS}	Short-circuit output current	V_{ODOUT+} or V_{ODOUT-} = 0V			± 24	mA
		V_{OD} = 0V			±12	
I_{OZ}	High-impedance output current	V_{OD} = 0V or V_{CC}			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5V, V_O= 2.45V			±1	
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) +0.5V		5		pF
C_O	Output capacitance	V_I = 0.4 sin (4E6πt) +0.5V, Disabled		9.4		

Note: 1. All typical values are at 25°C and with a 3.3V supply.

Switching Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.(1)	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50-Ohm (PI90LVB3811) R_L = 100-Ohm (PI90LV3811) C_L = 10pF See Figure 4	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low level output		0.9	1.6	2.9	
t_r	Differential output signal rise time		0.4	0.8	1.3	
t_f	Differential output signal fall time		0.4	0.8	1.3	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			150	500	ps
$t_{sk(o)}$	Output skew(2)			80	150	
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	See Figure 5		6.4	15	
t_{PZL}	Propagation delay time, high-impedance to low-level output			5.9	15	
t_{PHZ}	Propagation delay time, high-level to high-impedance output			3.5	15	
t_{PLZ}	Propagation delay time, high-level to low-impedance output			3.5	15	

Notes:
1. All typical values are at 25°C and with a 3.3V supply
2. $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
3. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits

Parameter Measurement Information

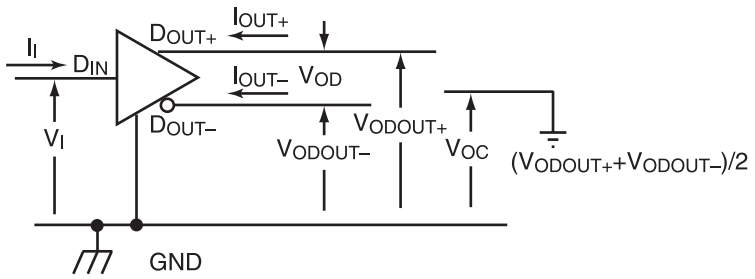


Figure 1. Voltage and Current Definitions

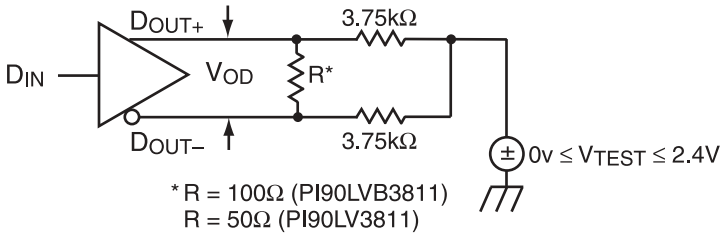
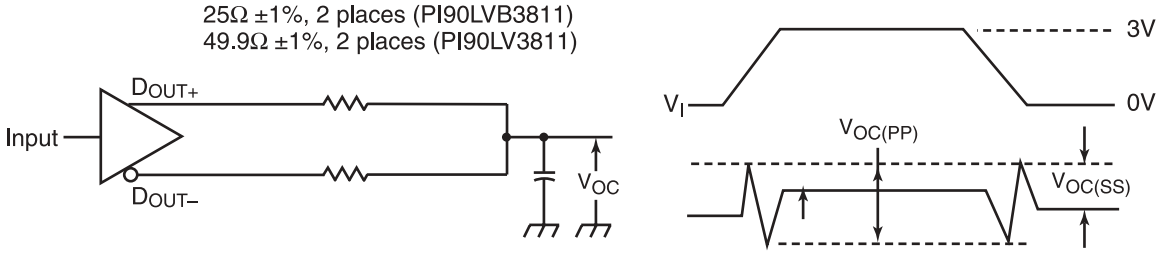


Figure 2. V_{OD} Test Circuit

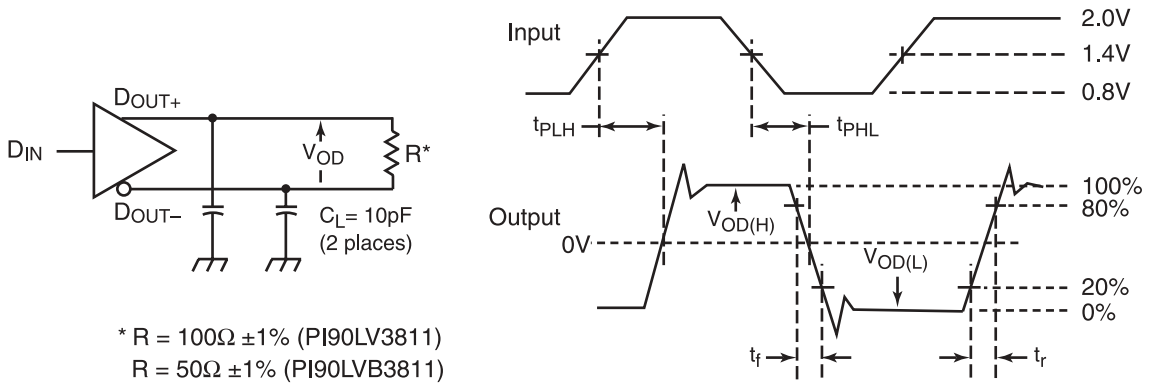


Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, Pulse Repetition Rate (PRR) = 50 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T. The measurement of VOC(PP) is made on test equipment with a –3dB bandwidth of at least 300MHz.

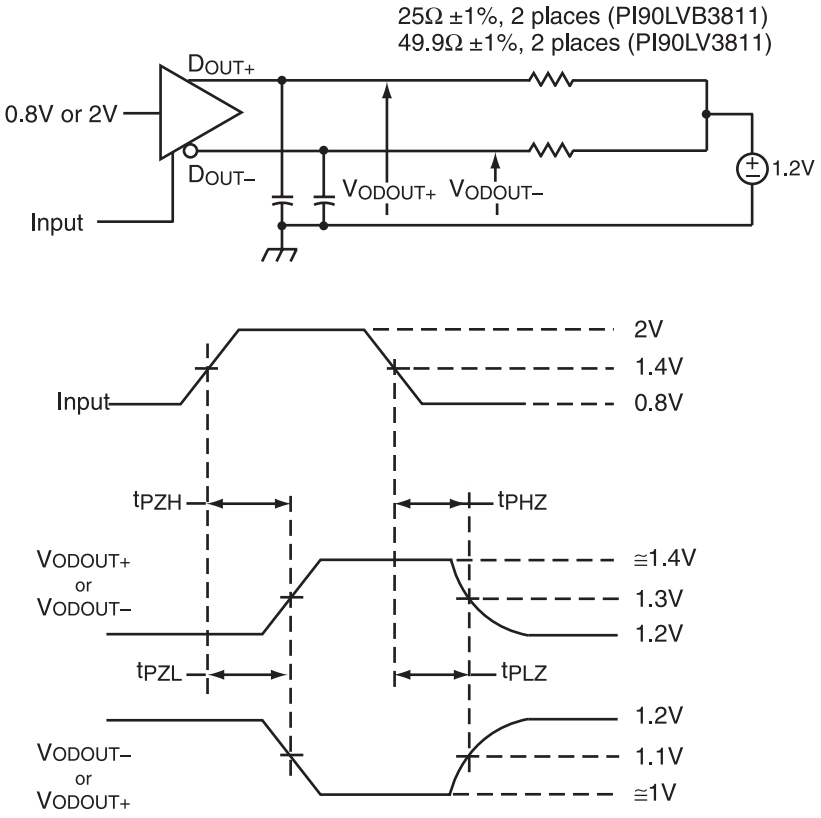
Figure 3. Test Circuit & Definitions for the Driver Common-Mode Output Voltage

Parameter Measurement Information (continued)



Note:
1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PRR) = 15 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Figure 4. Test Circuit, Timing, & Voltage Definitions for the Differential Output Signal



Note:
1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, Pulse width = 500 ±10ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Figure 5. Enable & Disable Time Circuit & Definitions

Typical Characteristics

Supply Current (RMS) vs. Switching Frequency

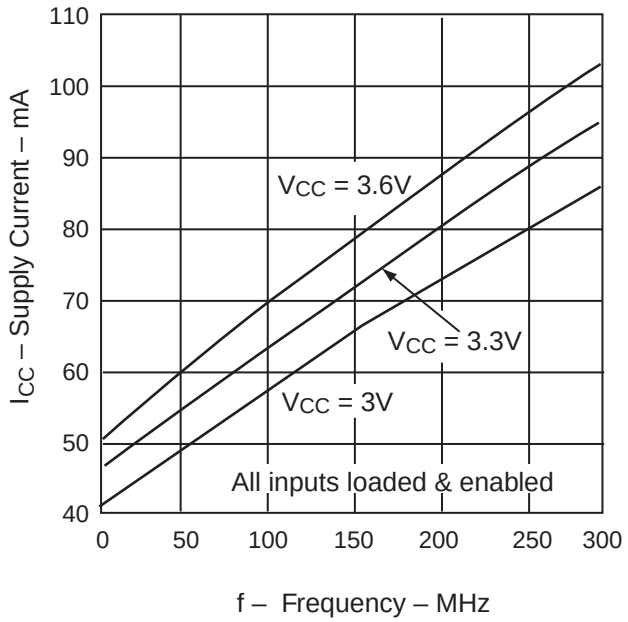


Figure 6.

Low-to-High Propagation Delay Time vs. Free-Air Temperature

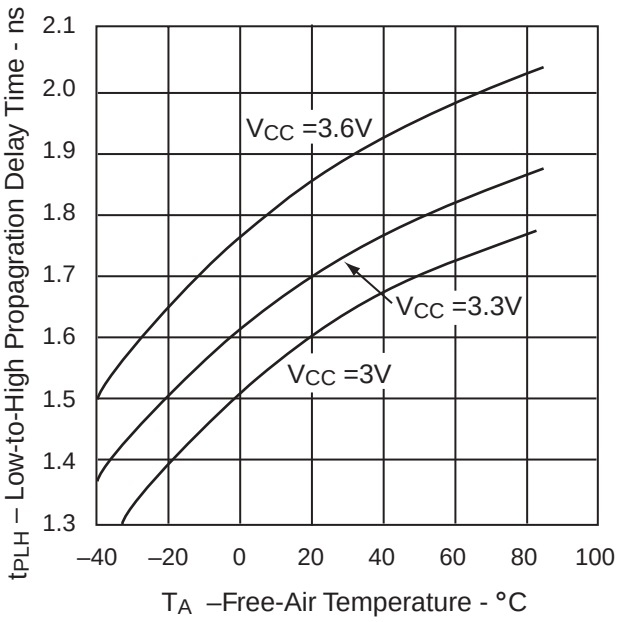


Figure 7.

High-to-Low Propagation Delay Time vs. Free-Air Temperature

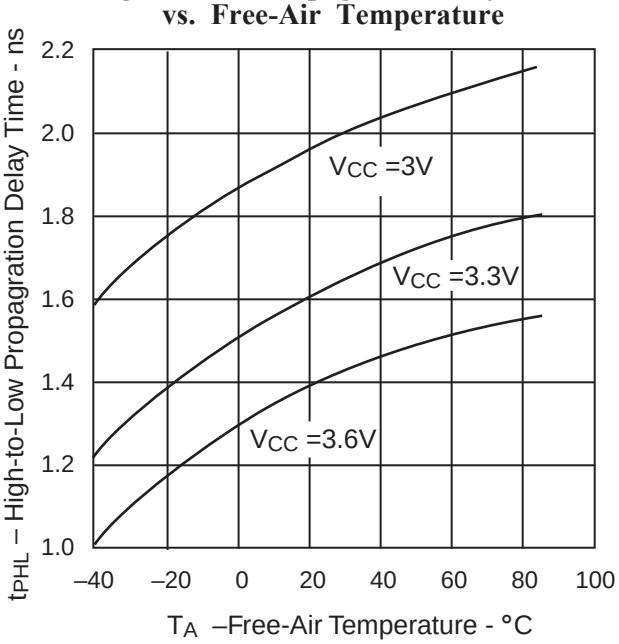
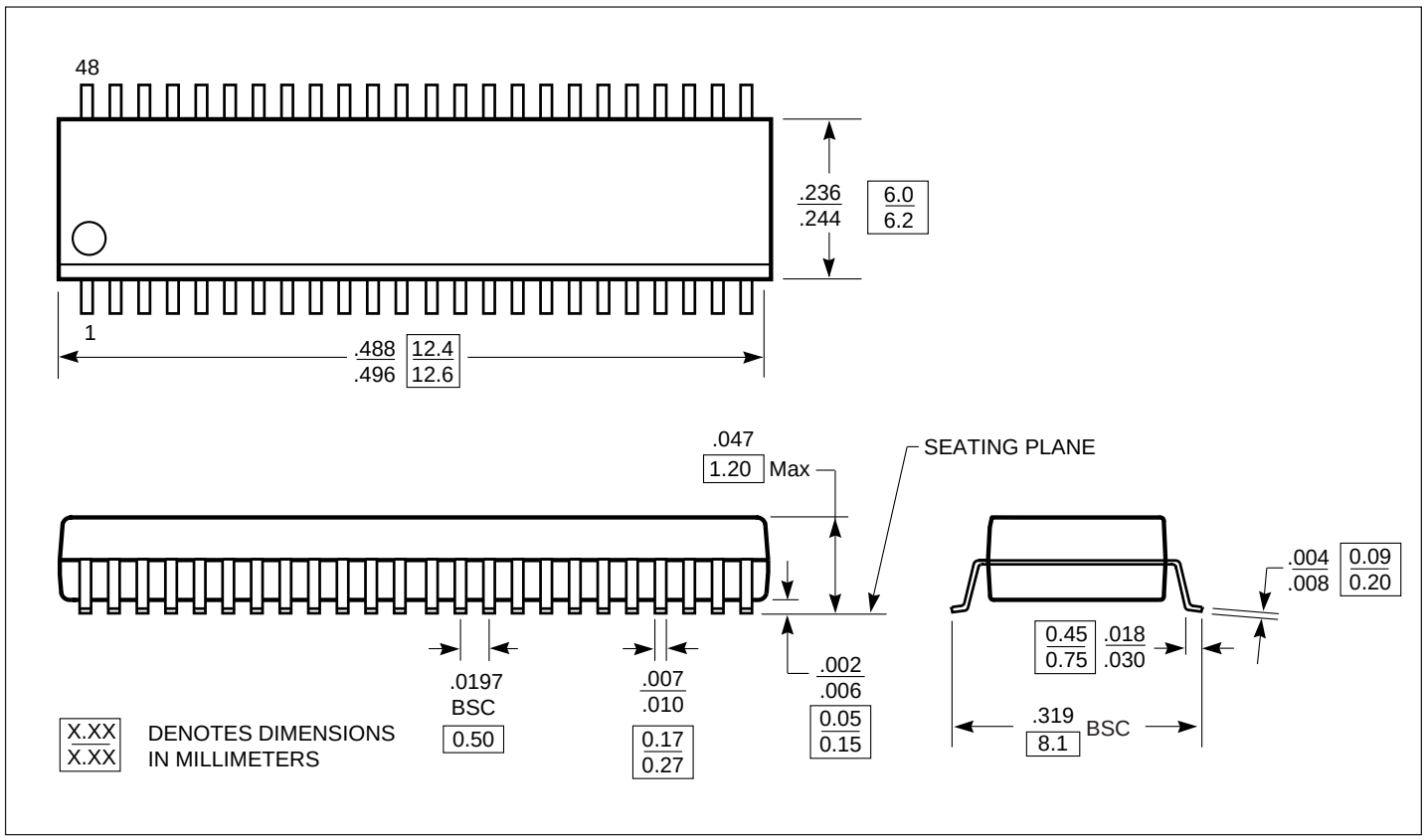


Figure 8.

Packaging Mechanical: 48-Pin TSSOP (A)



Ordering Information

Ordering Code	Package Code	Package Type	Operating Range
PI90LV3811A	A48	48-pin TSSOP	–40°C to 85°C
PI90LVB3811A	A48	48-pin TSSOP	