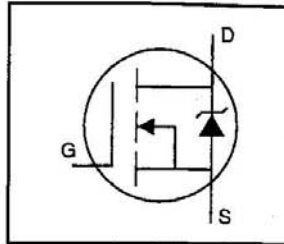


# IRFI840GLCPbF

## HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V<sub>GS</sub> Rating
- Isolated Package
- High Voltage Isolation= 2.5KV<sub>RMS</sub> ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Repetitive Avalanche Rated
- Lead-Free



$$V_{DSS} = 500V$$

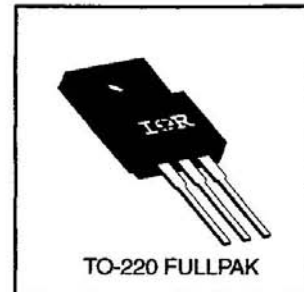
$$R_{DS(on)} = 0.85\Omega$$

$$I_D = 4.5A$$

### Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced HEXFET technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware. The moulding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.



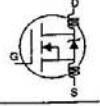
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	4.5	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	2.9	
$I_{DM}$	Pulsed Drain Current ①	18	
$P_D @ T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	±30	V
$E_{AS}$	Single Pulse Avalanche Energy ②	300	mJ
$I_{AR}$	Avalanche Current ①	4.5	A
$E_{AR}$	Repetitive Avalanche Energy ①	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

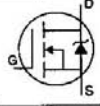
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	500	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =2.7A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	4.0	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =4.8A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =400V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	39	nC	I <sub>D</sub> =8.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	10		V <sub>DS</sub> =400V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	19		V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	12	—	ns	V <sub>DD</sub> =250V
t <sub>r</sub>	Rise Time	—	25	—		I <sub>D</sub> =8.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	27	—		R <sub>G</sub> =9.1Ω
t <sub>f</sub>	Fall Time	—	19	—		R <sub>D</sub> =30Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>ISS</sub>	Input Capacitance	—	1100	—	pF	V <sub>GS</sub> =0V
C <sub>OSS</sub>	Output Capacitance	—	170	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—		f=1.0MHz

### Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	4.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	18		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>J</sub> =25°C, I <sub>S</sub> =4.5A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	490	740	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =8.0A
Q <sub>rr</sub>	Reverse Recovery Charge	—	3.0	4.5	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

#### Notes:

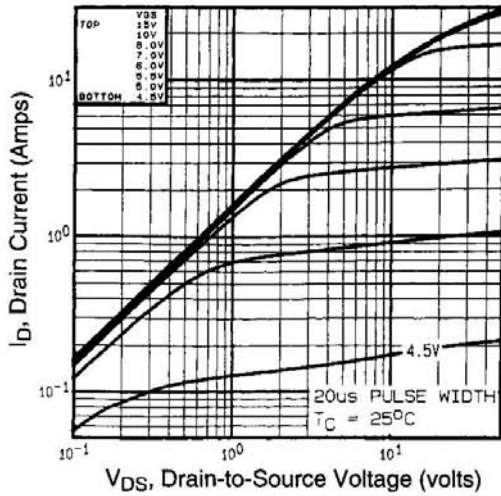
① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=26mH  
R<sub>G</sub>=25Ω, I<sub>AS</sub>=4.5A (See Figure 12)

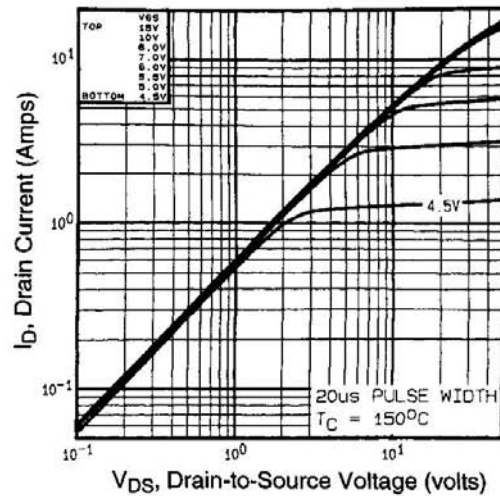
③ I<sub>SD</sub>≤8.0A, di/dt≤100A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>,  
T<sub>J</sub>≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

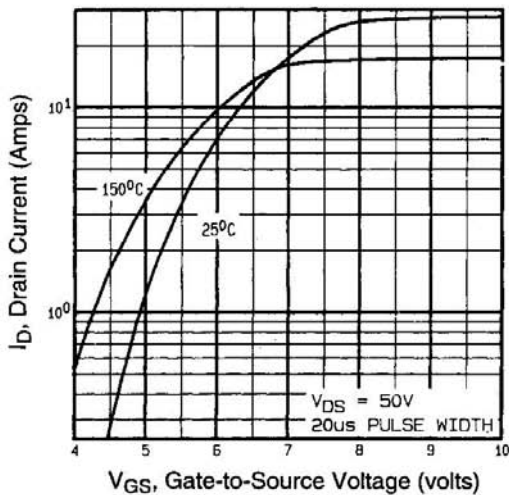
⑤ t=60s, f=60Hz



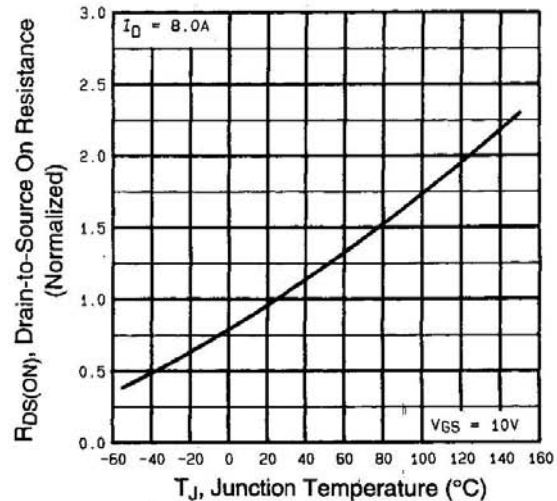
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



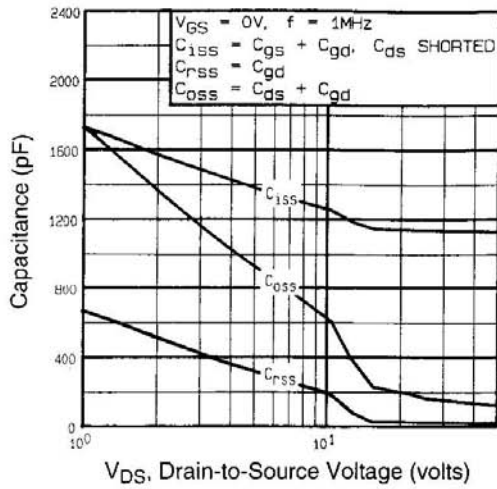
**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



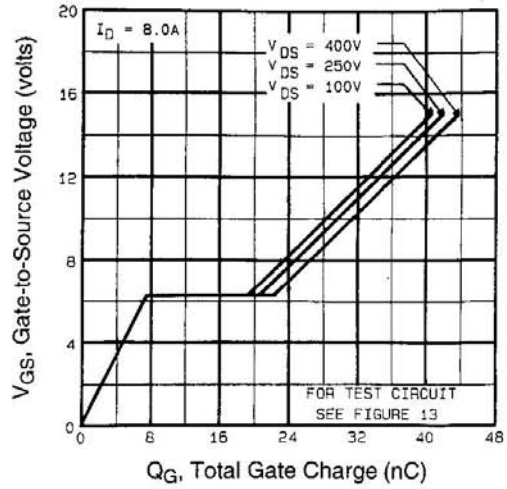
**Fig 3.** Typical Transfer Characteristics



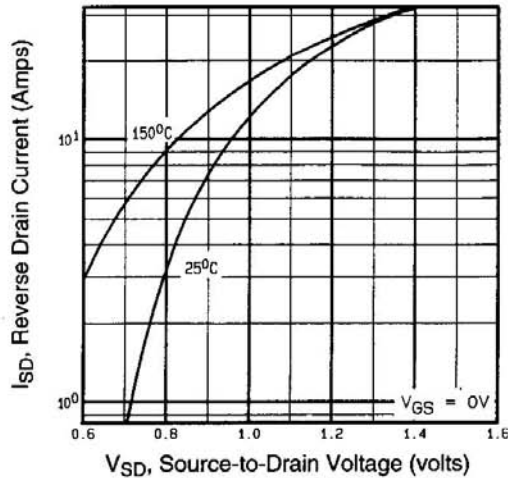
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



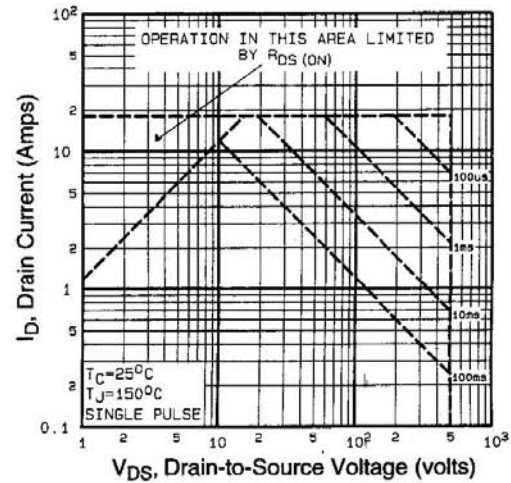
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



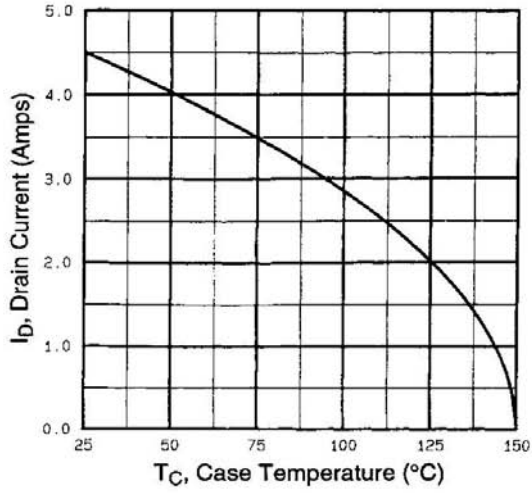
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



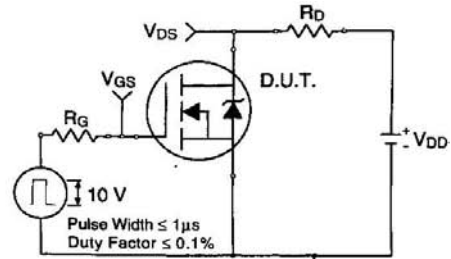
**Fig 7.** Typical Source-Drain Diode Forward Voltage



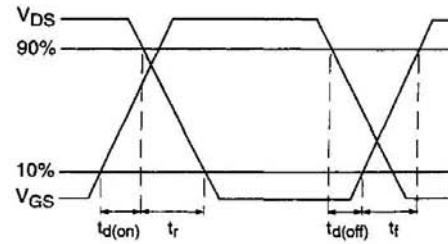
**Fig 8.** Maximum Safe Operating Area



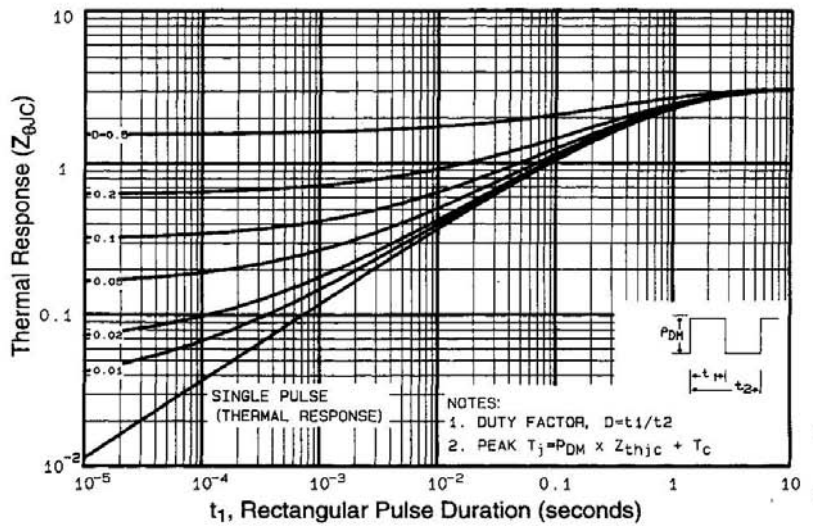
**Fig 9.** Maximum Drain Current Vs. Case Temperature



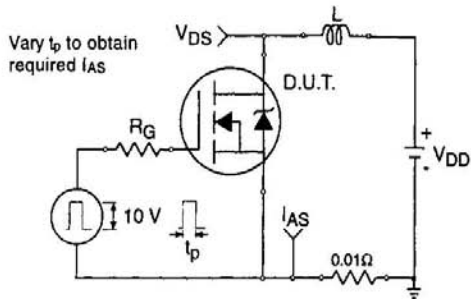
**Fig 10a.** Switching Time Test Circuit



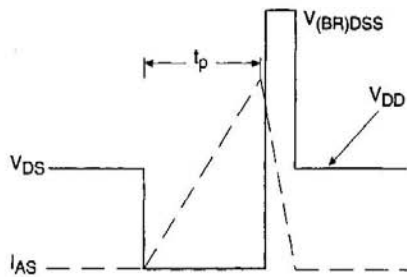
**Fig 10b.** Switching Time Waveforms



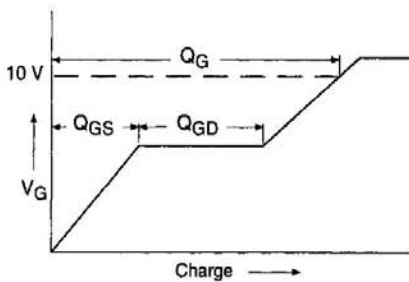
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



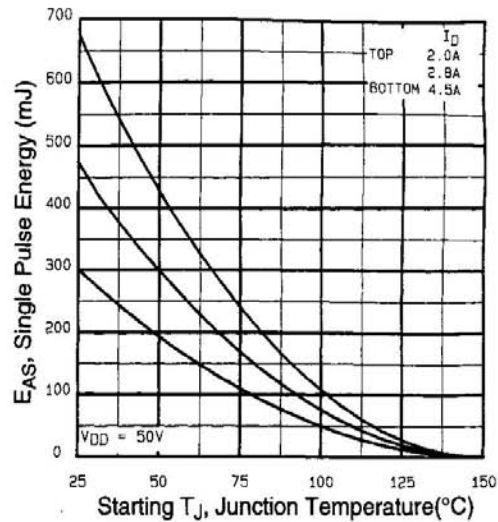
**Fig 12a.** Unclamped Inductive Test Circuit



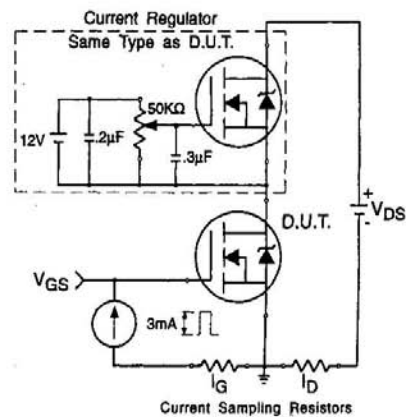
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

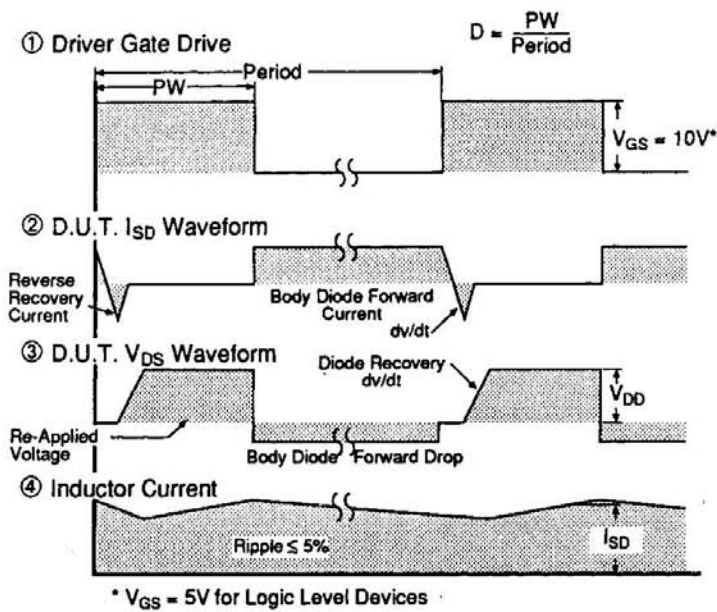
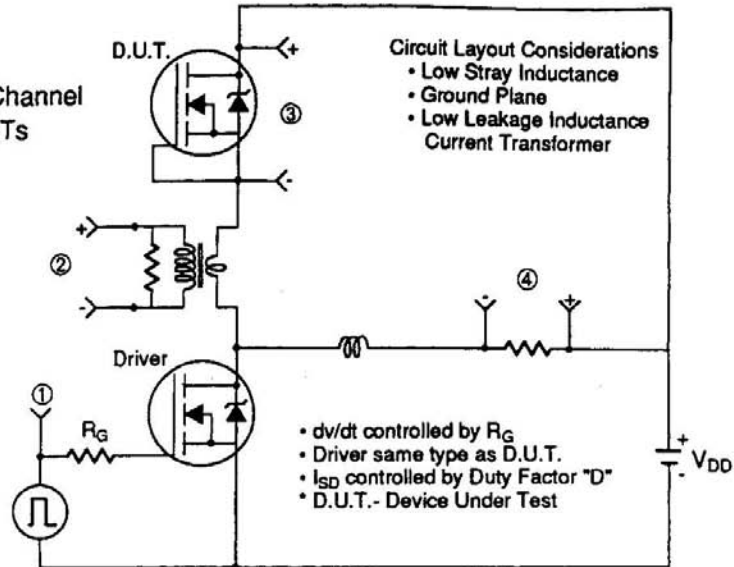


**Fig 13b.** Gate Charge Test Circuit

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

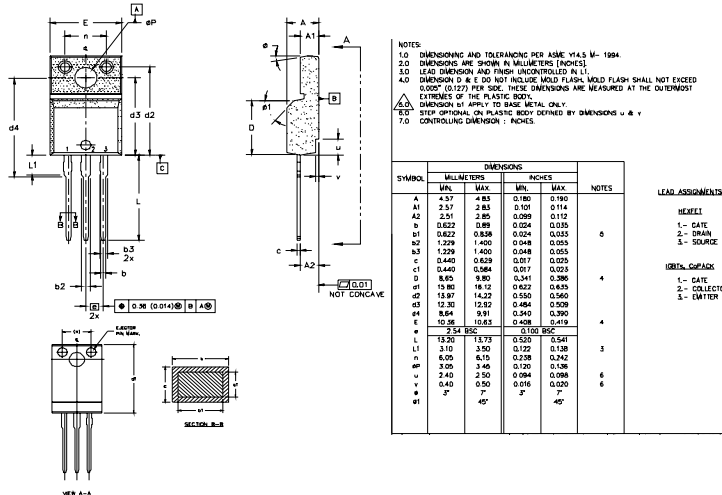


# IRFI840GLCPbF

International  
**IR** Rectifier

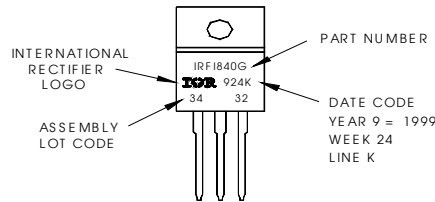
## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON WW 24 1999  
 IN THE ASSEMBLY LINE "K"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"



Data and specifications subject to change without notice.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-7903

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[www.irf.com](http://www.irf.com)



Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>