

- Extra Small Packaging Style
- Ultra Low Jitter
- Low Phase Noise
- Immediate Delivery



Part Numbering Example: CAMs C 3 Q Z - A5 B6 - XXX.XXXX TS

CAMs	C	3	Q	Z	A5	B6	XXX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	PACKAGING OPTIONS	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CAMs	C=HCMOS	3 = 3.2 X 2.5 Ceramic 5 = 5.0 X 3.2 Ceramic 7 = 5.0 X 7.0 Ceramic	Q = 1.8 V S = 2.5 V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.5~133.000 MHz	TS = Tri-State PD= Power Down

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.500		133.000	MHz
Available Stability Options:	-100 -50 -25		100 50 25	ppm ppm ppm
Supply Voltage Options: (1.5–133 MHz)	1.62 2.25 2.97	1.8 2.5 3.3	1.98 2.75 3.63	V V V
Operating Temperature Range Options:	0 -20 -40		+70 +70 +85	°C °C °C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V/2.5V			±5	
Output Level:	HCMOS			
Packaging:	Tape and Reel (1K per Reel) Tube			

Operating Conditions:

Description	Min	Max	Unit
Vdd Supply Voltage	1.62	1.98	V
Vdd Rise Time	100		µS
HCMOS Max Capacitive Load on outputs for CMOS levels Frequency: < 40 MHz Frequency: 40–133 MHz		25 15	pF pF



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Electrical Characteristics

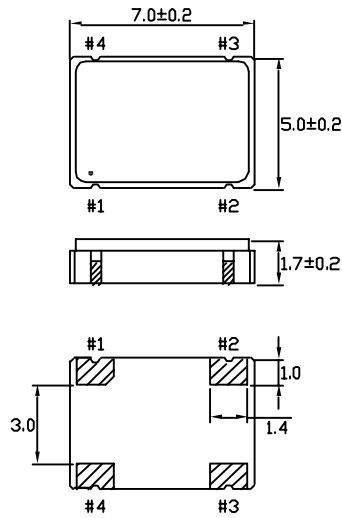
Description	TEST CONDITIONS	Min	Typ	Max	Unit
Input Characteristics (Pin 1): V _{IL} , Low-Level Input Voltage TO DISABLE OUTPUT				0.2V _{dd}	V
V _{IH} , High-Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT		0.7V _{dd}			V
I _{IL} , Input Low Current I _{IH} , Input High Current	V _{IN} = 0V V _{IN} = V _{dd}			80 10	μA μA
Output Characteristics: V _{OL} , Low-Level Output Voltage	1.8V V _{dd} , 8 mA I _{oL}			0.4	V
V _{OHC} MOS, High-level HCMOS Voltage	1.8V V _{dd} , -8 mA I _{oL}	V _{dd} -0.4			V V
Power Supply Current: (Loaded)	1.8V V _{dd} , OUTPUT FREQ < 133 MHz			15	mA
Input Pull-Up Resistor:	1.8V V _{dd}	50	70	90	kΩ
Tri-State Leakage Current:	TS option, Pin 1 low			20	μA
Power Down Current:	PD option, Pin 1 low			10	μA

Output Clock Switching Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle: HCMOS @ V _{dd} /2	1.8 V V _{dd}	45		55	%
Output Clock Rise/Fall:	0.2–0.8V _{dd} , 1.8 V _{dd} , C _L = 15		2		nS nS
Start Up Time:	From power on		3	10	mS
RMS Period Jitter:			7	10	pS
RMS Integrated Jitter:	12kHz to 20MHz		30		pS
Phase Noise:	@ 10kHz			-90	dBc/Hz

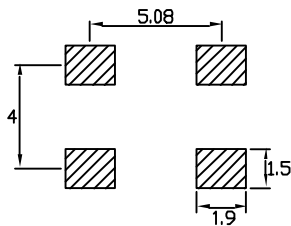


Style 7 5x7 Ceramic SMD

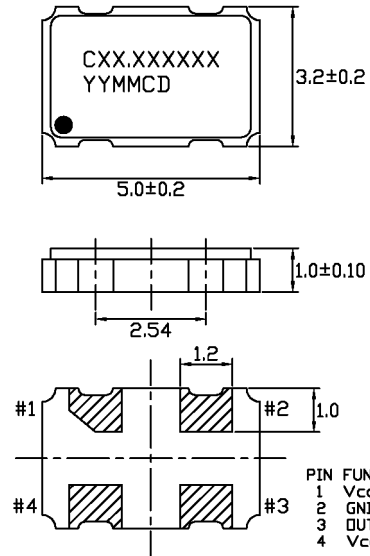


PIN FUNCTION
 1 CONTROL
 2 GND
 3 OUTPUT
 4 Vdd

Recommended Solder Pad Layout



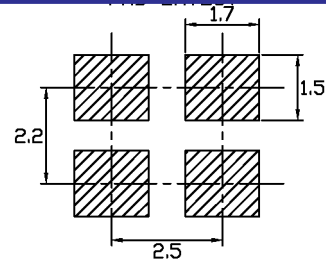
Style 5 5x3.2 Ceramic SMD



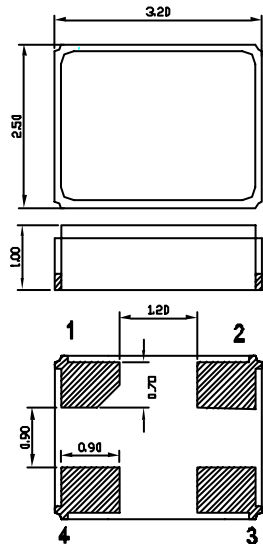
PIN FUNCTION
 1 CONTROL
 2 GND
 3 OUTPUT
 4 Vdd

PIN FUNCTION
 1 Vcont
 2 GND
 3 OUT
 4 Vcc

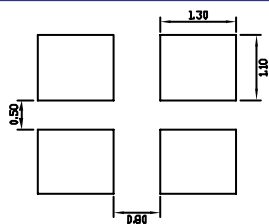
Recommended Solder Pad Layout



Style 3 3.2x2.5 Ceramic SMD



Recommended Solder Pad Layout



Note: Bypass Vdd to GND with a 0.01µF capacitor

