



ALPHA & OMEGA
SEMICONDUCTOR

AOD4106

N-Channel Enhancement Mode Field Effect Transistor



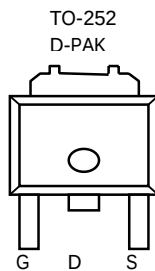
General Description

The AOD4106 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a low side switch in SMPS and general purpose applications. *Standard Product AOD4106 is Pb-free (meets ROHS & Sony 259 specifications). AOD4106L is a Green Product ordering option. AOD4106 and AOD4106L are electrically identical.*

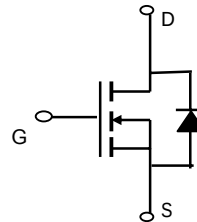
Features

V_{DS} (V) = 25V
 I_D = 50A (V_{GS} = 20V)
 $R_{DS(ON)}$ < 5m Ω (V_{GS} = 20V)
 $R_{DS(ON)}$ < 6.5m Ω (V_{GS} = 12V)
 $R_{DS(ON)}$ < 8.1m Ω (V_{GS} = 10V)

UIS Tested
Rg, Ciss, Coss, Crss Tested



Top View
Drain Connected to
Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^G	I_D	50	A
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		50	
Pulsed Drain Current ^C	I_{DM}	180	
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.3\text{mH}$ ^C	E_{AR}	135	mJ
Power Dissipation ^B	P_D	75	W
		38	
Power Dissipation ^A	P_{DSM}	6.25	W
		4	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	41	50	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case ^B	$R_{\theta JC}$	1.5	2.0	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	25			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2	3	4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=12\text{V}$, $V_{DS}=5\text{V}$	180			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=20\text{V}$, $I_D=20\text{A}$ $T_J=125^{\circ}\text{C}$		4.1 6.5	5.0	$\text{m}\Omega$
		$V_{GS}=12\text{V}$, $I_D=20\text{A}$		5.4	6.5	$\text{m}\Omega$
		$V_{GS}=10\text{V}$, $I_D=20\text{A}$		6.6	8.1	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		26		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current ^G				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=12.5\text{V}$, $f=1\text{MHz}$		1561	1875	pF
C_{oss}	Output Capacitance			642		pF
C_{rss}	Reverse Transfer Capacitance			323		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.5	3.8	Ω
SWITCHING PARAMETERS						
$Q_g(12\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $I_D=20\text{A}$		26.5	33	nC
$Q_g(10\text{V})$	Total Gate Charge			22.5		nC
Q_{gs}	Gate Source Charge			8.3		nC
Q_{gd}	Gate Drain Charge			10		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $R_L=0.63\Omega$, $R_{GEN}=3\Omega$		12		ns
t_r	Turn-On Rise Time			19		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			9.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		32	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		24		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $t<10\text{s}$ $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.

Re0: Sept. 2006

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

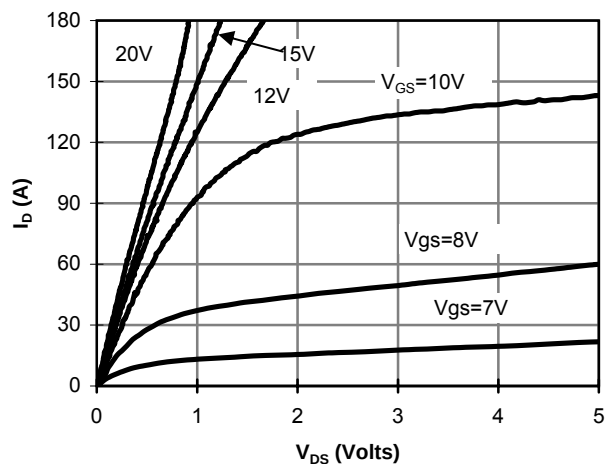


Figure 1: On-Region Characteristics

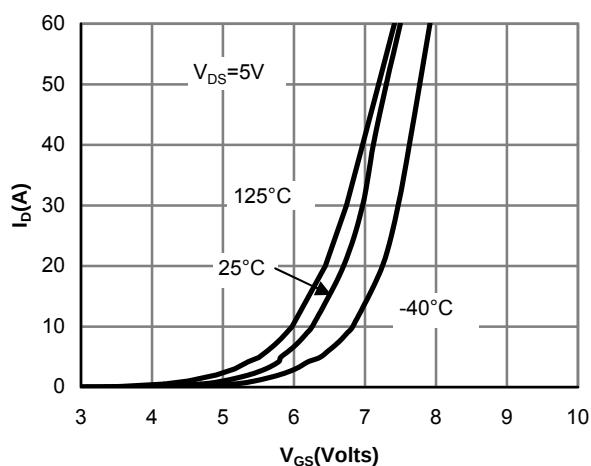


Figure 2: Transfer Characteristics

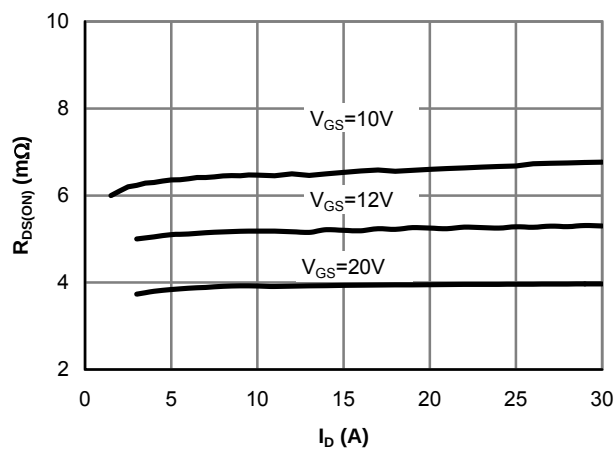


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

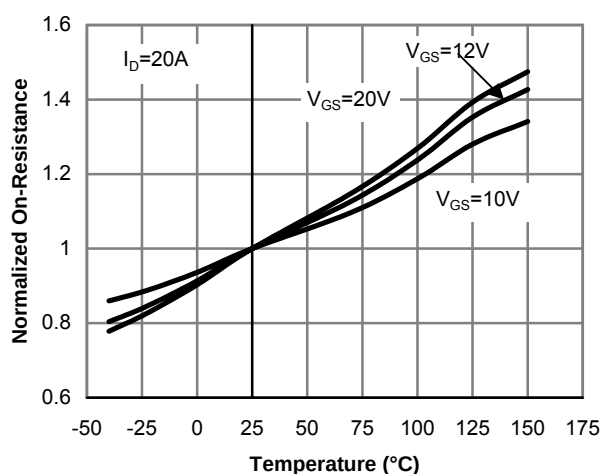


Figure 4: On-Resistance vs. Junction Temperature

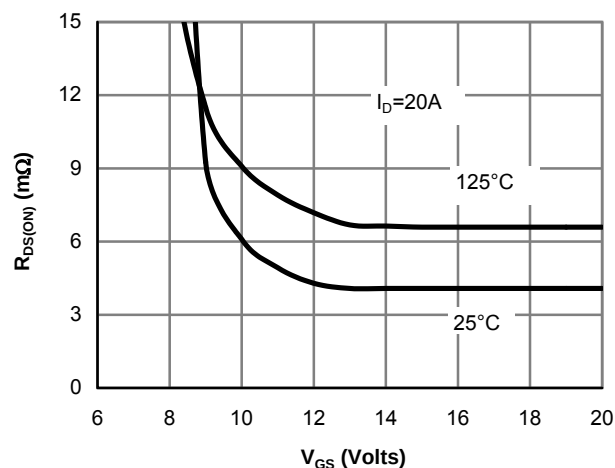


Figure 5: On-Resistance vs. Gate-Source Voltage

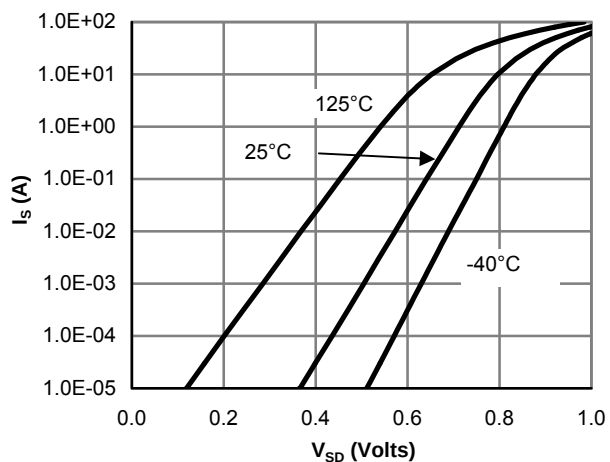


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

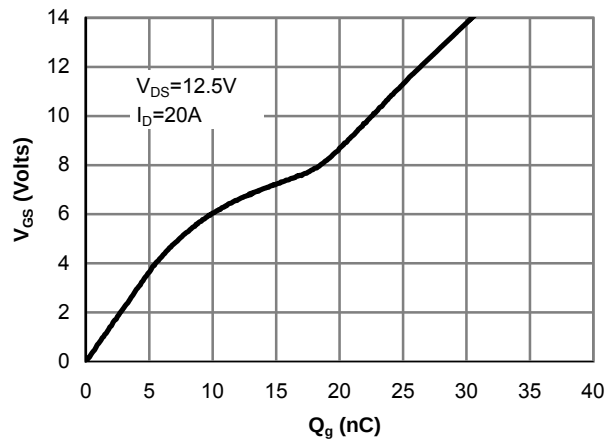


Figure 7: Gate-Charge Characteristics

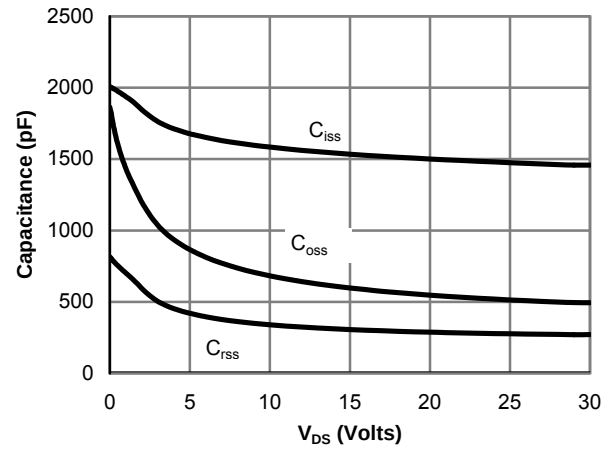


Figure 8: Capacitance Characteristics

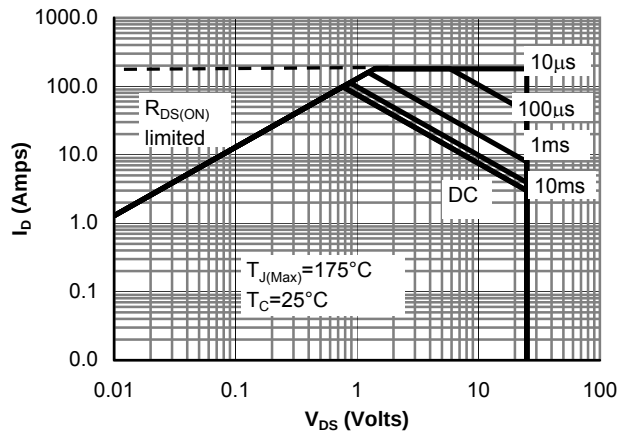


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

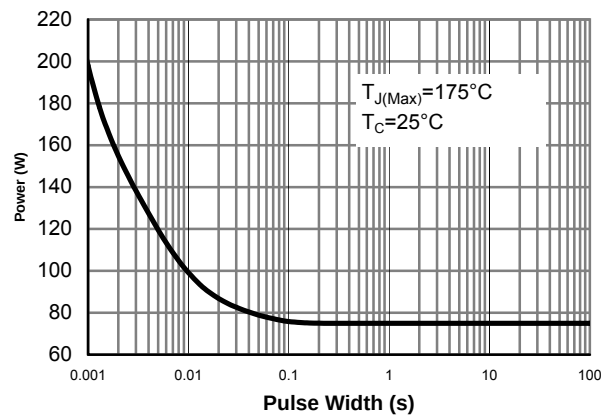


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

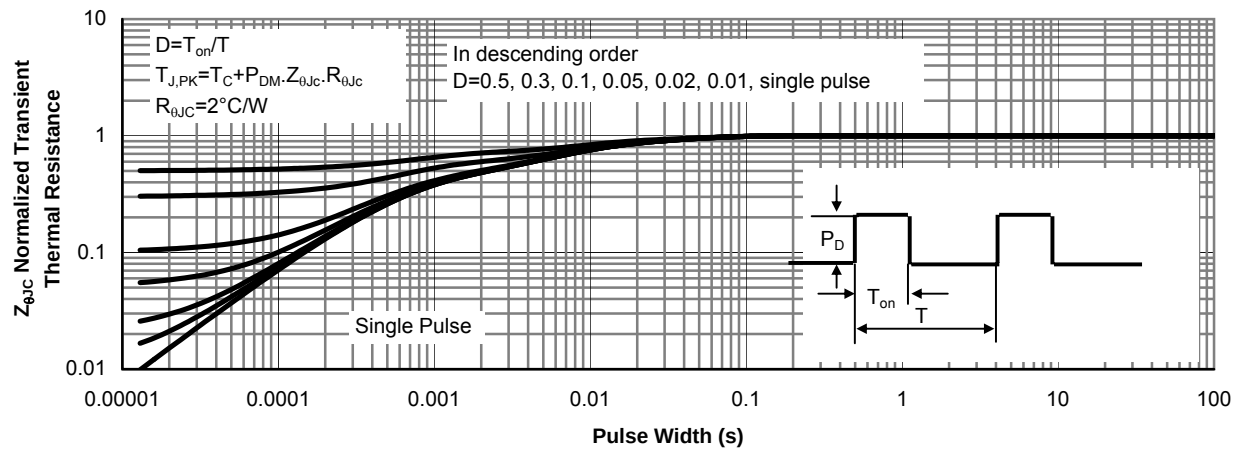


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

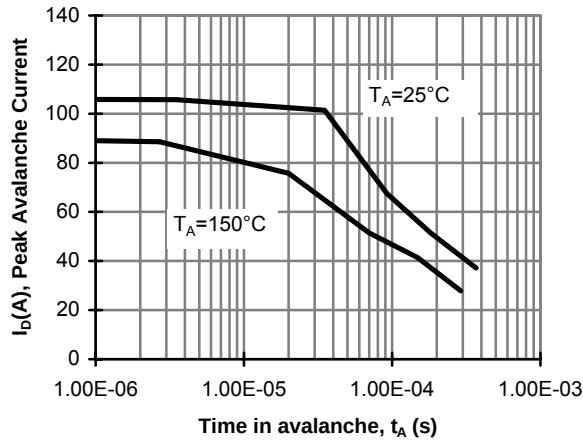


Figure 12: Single Pulse Avalanche capability

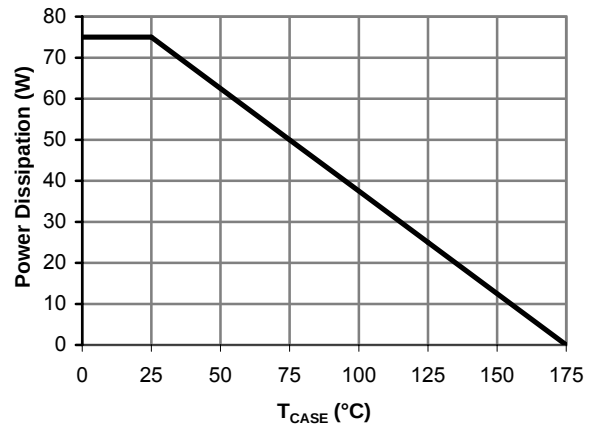


Figure 13: Power De-rating (Note B)

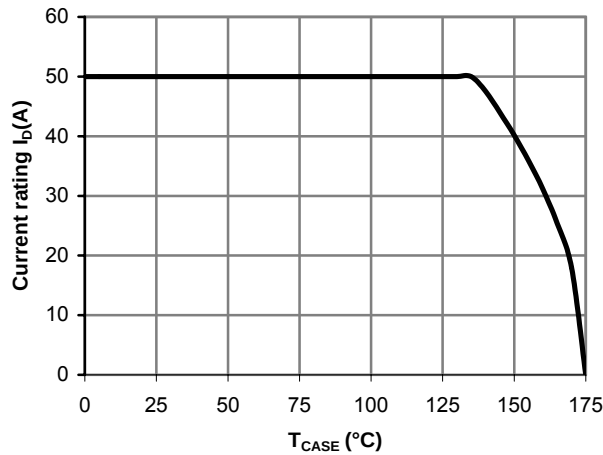


Figure 14: Current De-rating (Note B)

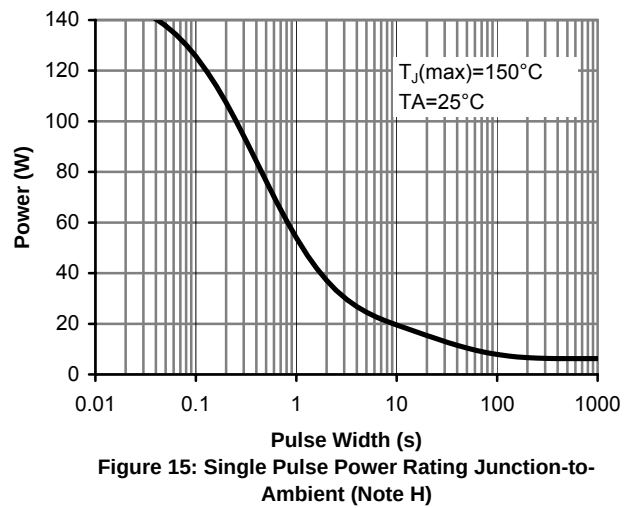


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

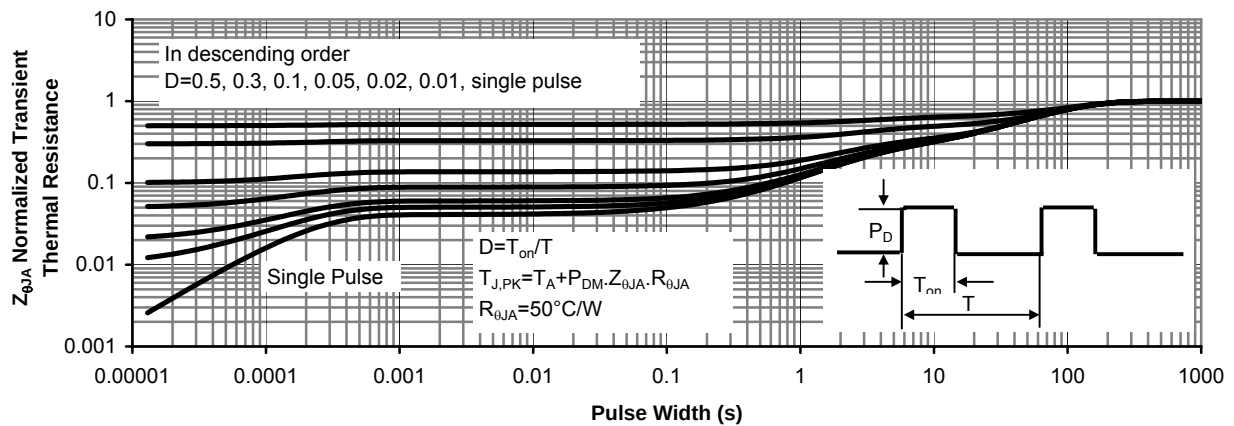


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)