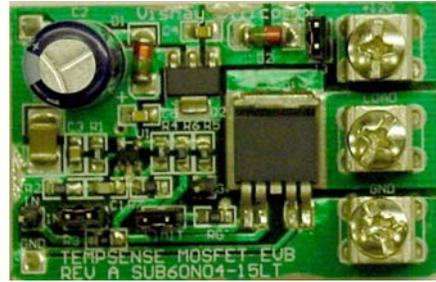


Temperature Sensing MOSFET Evaluation Board

FEATURES

- Turns Off MOSFET Before T_J Exceeds 175°C Rating
- 5-V Logic Level Operation of Control Circuit
- 12-V Battery Level Operation of Power MOSFET Circuit
- Sense Diode Bias Current, $I_F = 250 \mu A$
- Built-In Hysteresis to Ensure Jitter Free Operation
- Cyclic Operation of MOSFET (Turn-On and Turn-Off) Under Continuous Fault Condition
- Flexibility to Set MOSFET Turn-Off Temperature



ORDERING INFORMATION: SiDB766761

DESCRIPTION

The Vishay Siliconix SUB60N04-15LT, temperature sensing MOSFET, provides the capabilities to sense the junction temperature, T_J , and implement self-protection in a control circuit. An electrically isolated poly-silicon diode, which is located in the close proximity to MOSFET junction on the same die, facilitates temperature sensing. The forward voltage drop of sense diode has a negative temperature co-efficient of approximately $-2mV/^\circ C$. In other words, the forward voltage drop of the sense diode is inversely proportional to the MOSFET junction temperature.

This evaluation board demonstrates the self-protection feature in a control circuit, using SUB60N04-15LT, the temperature sensing MOSFET. The cyclic turn-off and turn-on of the MOSFET under the fault condition protects it from catastrophic failure.

The appendix includes, a schematic diagram, test setup, bill-of-materials, and PCB layouts. Using this information, one can incorporate the basic control scheme described here, in any core system design of an application.

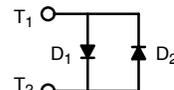
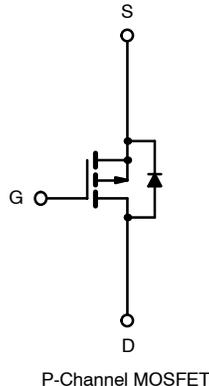
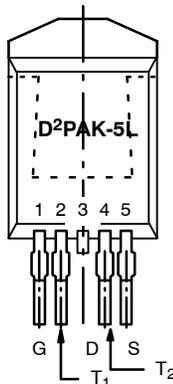
The demonstration board layout is available in Gerber file format. Contact your Vishay Siliconix sales representative/ distributor for a copy.

CIRCUIT DESCRIPTION

The schematic diagram shown in Appendix (A) is a simple comparator circuit that uses a low cost op-amp, LMV321. This IC is identified as "U1." The op-amp output Pin 4 provides gate drive approximately 4.8 V through resistor R6 to the temperature sensing MOSFET, Q1. The latter in turn controls the "load" connected between its drain, Pin 3, and +12 V. The voltage divider, resistors R1 and R2, establishes reference voltage $V_{REF} = 490 mV$. 5-V logic level input at the INPUT terminal provides the bias current, $I_F = 250 \mu A$, for the sense diode on Pins 2 and 4 of Q1. The op-amp is configured for

non-inverting mode by connecting the sense diode forward voltage drop to Pin 1, the "+" input through resistors R7. The feedback resistor R4 establishes 20-mV hysteresis on R7 to ensure jitter free operation. Resistor R5 facilitates monitoring of gate drive signal. Resistor R_G when connected to the MOSFET gate via jumper J2, cuts down the MOSFET gate drive to 2.8 V and shifts the MOSFET operation to linear mode.

The peripheral capacitors C1 through C5 are for power supply filter and noise suppression.



TEST SETUP

(a) Laboratory Equipment

This configuration facilitates testing with two laboratory power supplies. Refer to Appendix (B). A 5-V/2-A regulated power supply between +5 and GND powers up the control circuit. A separate 12-V/20-A power supply between +12 V and GND powers the load and MOSFET drain Pin 3 and source Pin 5. Remove the jumper 3. Thereby, the 5-V logic level power supply, V_{LL} , for the control circuit is independent of over load or shorted load on MOSFET side. Diodes D1 and D2 prevent reverse current flow in case of accidental connection of both power supplies when the jumper J3 is not removed.

Connect a suitable load that would draw about 1 A, e.g. a lamp (12 V, 1 A) or a resistor (12 Ω , 25 W) between terminal +12 V and load.

(b) Field Simulated Testing

Using a 12-V battery can simulate field level testing. This power source on the load side is capable of supplying continuous over load/short circuit current. In other words, the battery will have the capacity to maintain the terminal voltage of the 12-V even under short circuit conditions. Connect the battery between +12 V and GND. In this case, a separate 5-V logic level power supply is not required. The jumper J3 must be in place. The latter provides the 5-V logic level, V_{LL} , to the control circuit via on-board voltage regulator LM2937. The IC is identified as Q2.

OPERATION

Either step (a) or step (B) of the Test Setup enables the testing and demonstration of the self-protection feature as follows:

(a) Normal Operation

- Remove jumpers J1 and J2.
- Power-up the circuit
- Connect the Oscilloscope or DMM to monitoring Pin G.
- Observe $V_{(G)} = 0$ (or < 0.2 V), MOSFET in “off” state. No current flow in the load.

- Connect the jumper J1. This provides 5-V logic level signal on the INPUT terminal. Observe $V_{(G)} = 4.8$ V (approximately) The MOSFET turns on. The current flows through the load (lighted lamp, if a lamp load is used).

(b) Fault Condition

- Connect the jumper J4, Which is an external shorting link (not supplied), to short-circuit the load. Monitor $V_{(G)} = 4.8$ V, the MOSFET is still in “on” state. Observe excessive current flow from the 12-V supply. The MOSFET starts heating up. After sometime, the MOSFET turns off, monitor $V_{(G)} = 0$ (< 0.2 V). The load current drops to zero. The MOSFET starts cooling down. The MOSFET turns on again when cooling is complete. Observe $V_{(G)} = 4.8$ V and the load current flow from the power supply.
- The cycle repeats as long as jumper J4 is connected across the +12 V and load terminals and the setup is powered.
- Removing jumper J4 restores normal operation. The MOSFET maintains an “on” state with jumper J1 in place, with 5 V at the INPUT terminal.

ACCELERATED TESTING

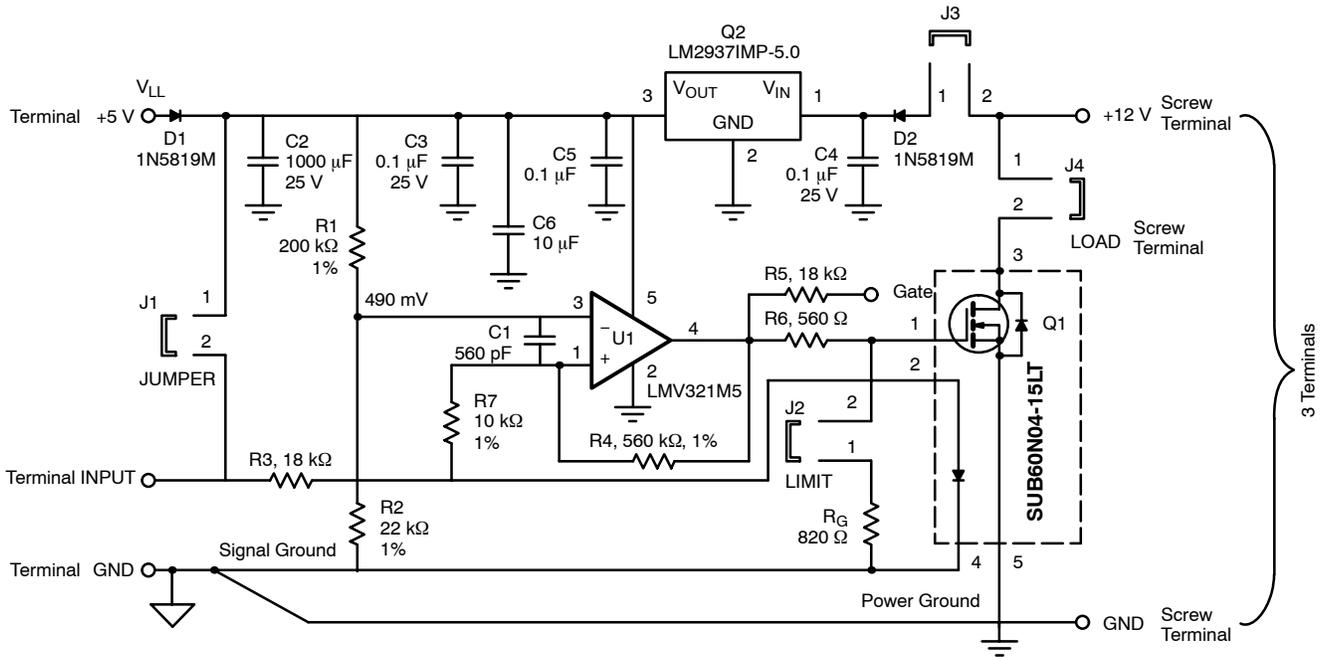
Jumper J2 facilitates accelerated testing. Now the actual gate voltage drops to 2.8 V because of voltage divider formed at the MOSFET gate Pin 1, by resistors R6 and R_G . Refer to the schematic diagram in Appendix (A). This drives the MOSFET in linear mode, resulting in accelerated heating of the MOSFET and faster turn off. The cycle time of fault condition is reduced.

SUMMARY

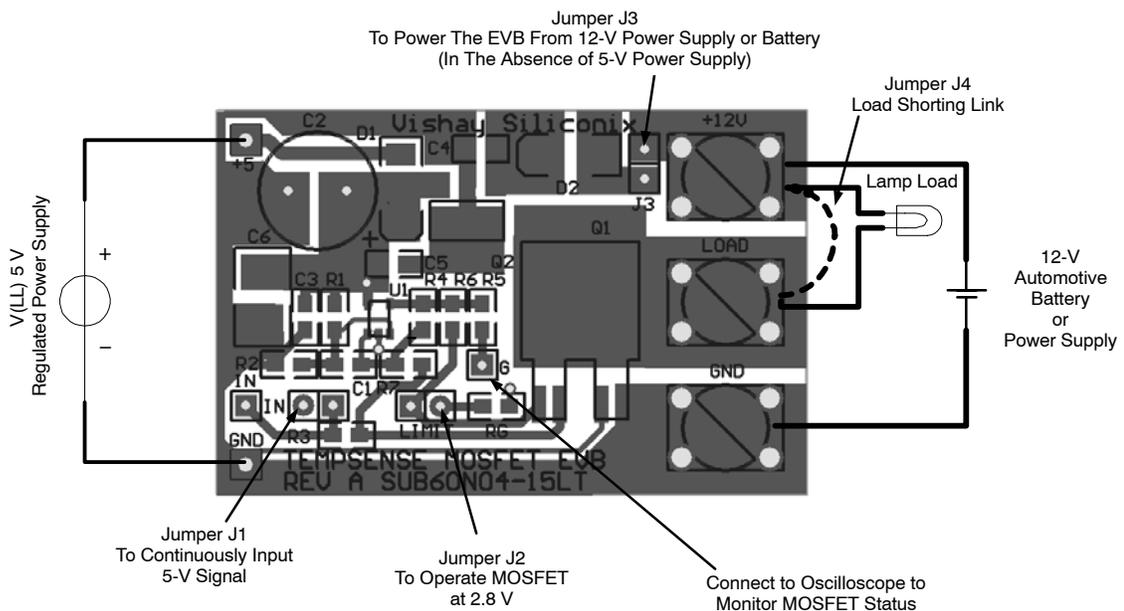
The evaluation board shows implementation of a self-protecting feature in a control circuit for a high-side connected floating load, using the temperature sensing MOSFET, SUB60N04-15LT. The circuit operation, under normal and fault conditions, demonstrates that the MOSFET can provide the desired load control function and also sustain continuous fault condition while exhibiting a self-protection feature. The basic control circuit can be easily incorporated into the core design of an application using the information provided in the Appendix.

For additional information on temperature sensing MOSFETs and actual design example refer to application note AN820 available via the Vishay web site, www.vishay.com.

APPENDIX A: SCHEMATIC DIAGRAM



APPENDIX B: TEST SETUP



APPENDIX C: LAYOUT

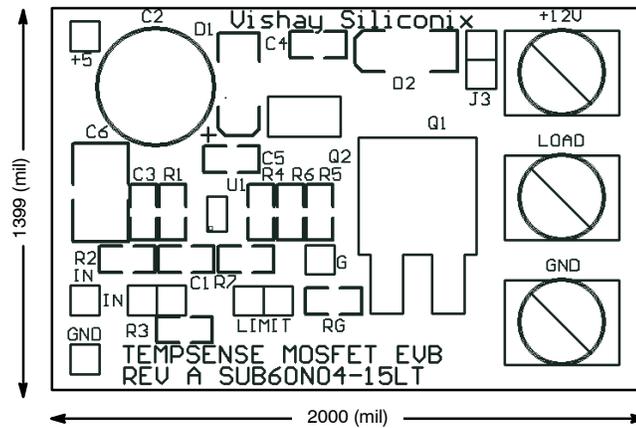


FIGURE 3. Silk Screen

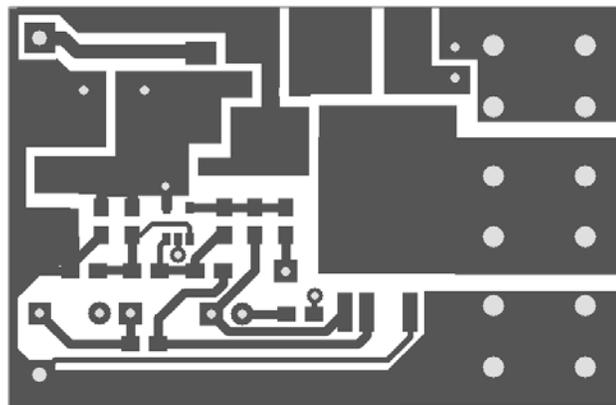


FIGURE 4. Top Layer

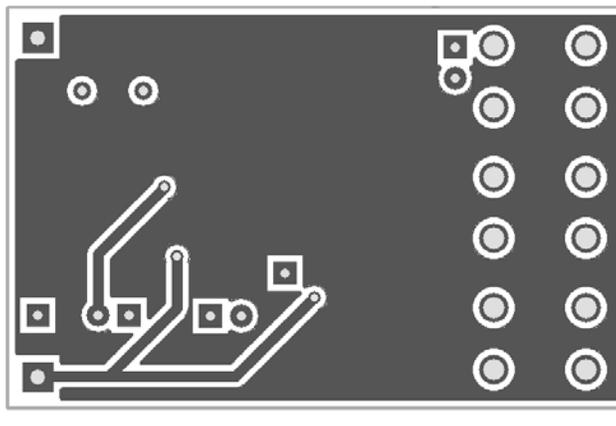


FIGURE 5. Bottom Layer



EVALUATION BOARD DISCLAIMER

Vishay Siliconix (Vishay) provides this evaluation board (EVB) under the following conditions:

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APPENDIX D: BILL-OF-MATERIAL

Item	Qty	Designator	Description	Footprint	Part Number	Manufacturer
1	1	R1	200-kΩ Resistor, 1%	805	CRCW0805, 200 kΩ, 1%	Vishay Dale
2	1	R2	22-kΩ Resistor, 1%	805	CRCW0805, 22 kΩ, 1%	Vishay Dale
3	2	R3, R5	18-kΩ Resistor, 5%	805	CRCW0805, 18 k, 5%	Vishay Dale
4	1	R4	560-kΩ Resistor, 1%	805	CRCW0805, 560 kΩ, 1%	Vishay Dale
5	1	R6	560-Ω Resistor, 5%	805	CRCW0805, 560 Ω, 5%	Vishay Dale
6	1	R7	10-kΩ Resistor, 1%	805	CRCW0805, 10 kΩ, 1%	Vishay Dale
7	1	R _G	820-Ω Resistor, 5%	805	CRCW0805, 820 Ω, 5%	Vishay Dale
8	1	C1	560-pF/25-V Ceramic Capacitor	805	VJ0805Y561JXAA	Vishay Vitramon
9	1	C2	1000-μF/25-V, Electrolytic Capacitor	RB-0.2/0.4		
10	3	C3, C4, C5	0.1-μF/25-V, Ceramic Capacitor	805	VJ0805Y104JXAA	Vishay Vitramon
11	1	C6	10-μF/25-V, Ceramic Capacitor	2512	VJ2225V106MXAA	Vishay Vitramon
12	2	D1, D2	1N5819M, Schottky Diode, 40 V, 1 A, SOD87	MELF		
13	1	Q1	SUB60N04-15LT, Temperature Sense MOSFET, 40 V	D ² PAK-5L	SUB60N04-15LT	Vishay Siliconix
14	1	Q2	LM2937IMP-5.0, IC, 5 V, 500 mA, LDO V _{REG}	SOT-223		
15	1	U1	LMV321M5, IC, Low Voltage Op Amp	SC70-5		
16	3	J1, J2, J3	Jumper Pins	SIP-2	929834-02-36-ND	Digi-Key
17	3	JMP Shunt	Jumper Shunts		A26228-ND	Digi-Key
18	2	+5 V, GND	In Board Pins	TURRET	V1055-ND	Digi-Key
19	2	IN, G	Press-In Terminal	TURRET	V1073-ND	Digi-Key
20	3	+12 V. Load, GND	Terminal, 12-V, GND	LOADCON	7693-ND	Digi-Key
21	1	PCB	Evaluation PC Board		TSM1	Vishay Siliconix