1. General Description

This EPROM-Based 4-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 0.5K words of ROM, and 30 nibbles of static RAM.

2. Features

The followings are some of the features on the hardware and software :

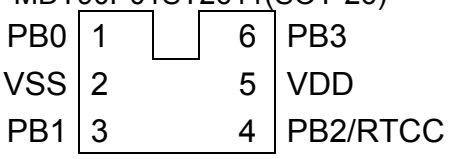
- Fully COMS static design
- 4-bit data bus
- On chip EPROM size : 0.5 K words
- Internal RAM size : 30 nibbles
  (24 general purpose registers, 6 special registers)
- 24 single word instructions
- 11-bit instructions
- 2-level stacks
- Operating voltage : 2.5 V ~ 5.5 V
- Internal RC oscillator : 4MHz / 8MHz
- Power-on Reset
- Sleep Mode for power saving
- oscillator start-up time : 20ms
- 8 bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- On-chip RC oscillator based Watchdog Timer(WDT)
- Wake-up from sleep on pin change

3. Applications

The application areas of this MDT90P01 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC pe-ripheral … etc.

4. Pin Assignment

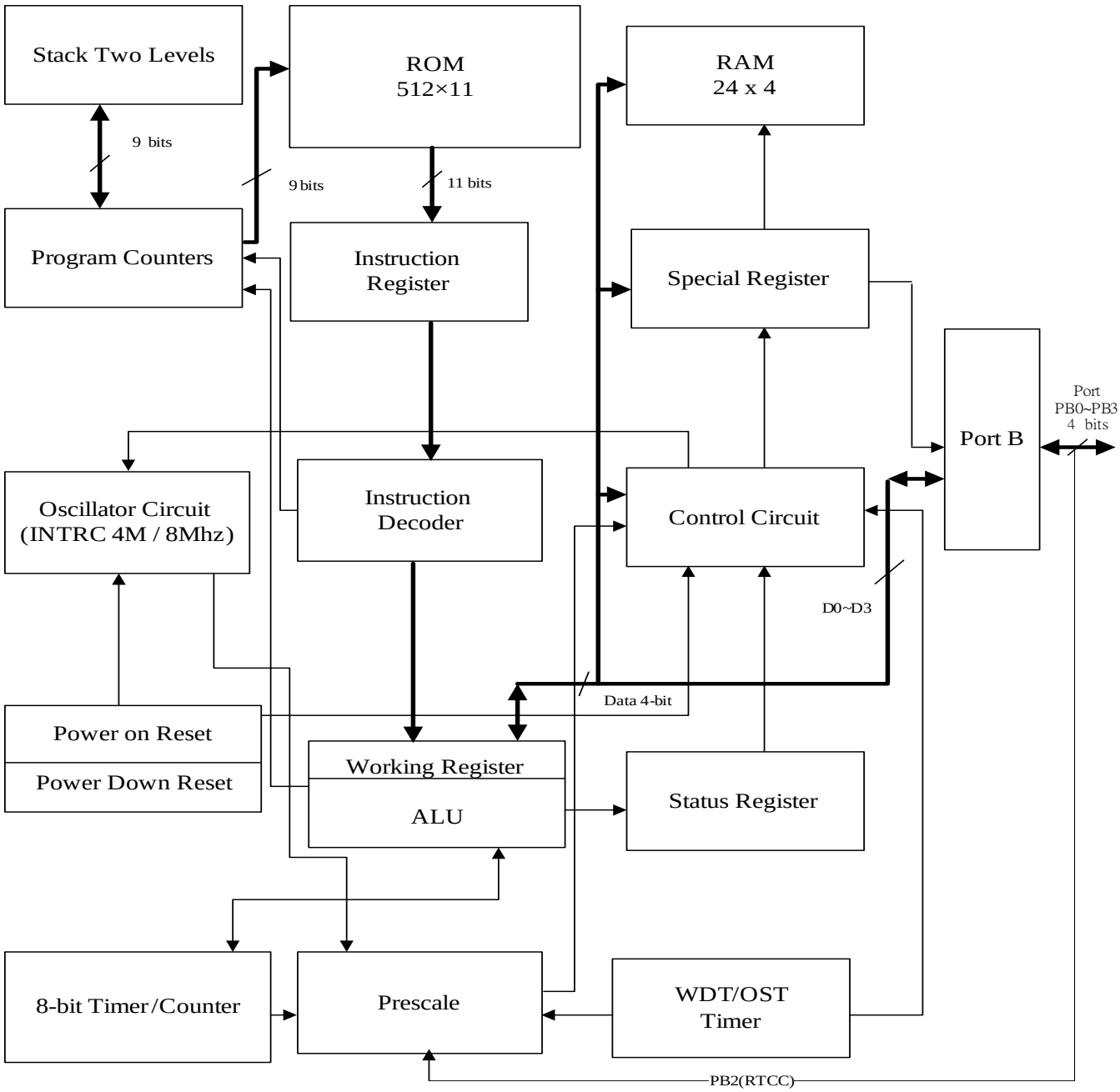
MDT90P01ST2611(SOT-26)



5. Order Information

Device	ROM (Words)	RAM (Nibbles)	I/O	Timer (8 Bit)	Package	Remark
MDT90P01ST2611	512	24	4	1	SOT-26	-

6. Block Diagram



7. Pin Function Description

Pin Name	I/O	Function Description
PB0	I/O	Port B, TTL input level .Can be software programmed for internal weak pill-up and wake-up from SLEEP on pin change
PB1	I/O	Port B, TTL input level .Output is open drain type. Can be software programmed for wake-up from SLEEP on pin change
PB2/RTCC	I/O	Real Time Clock/Counter, Schmitt Trigger input levels. .Output is open drain type.
PB3	I/O	Port B, TTL input level . Can be software programmed for internal weak pill-up and wake-up from SLEEP on pin change
V_{dd}		Power supply
V_{ss}		Ground

8. Memory Map

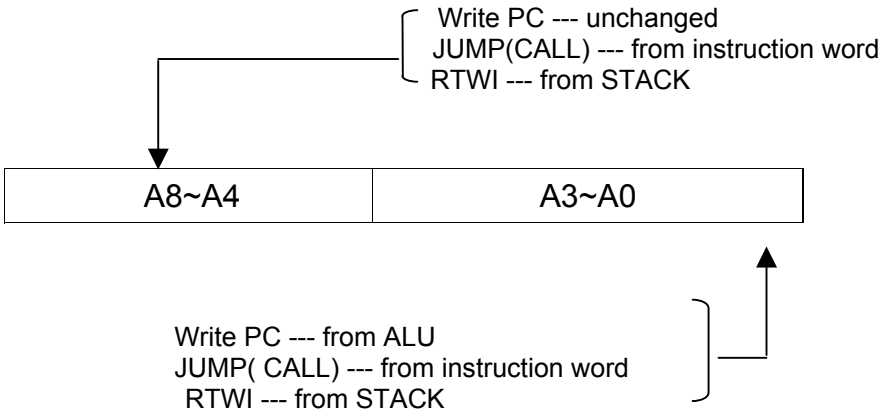
(A) Register Map

Address	Description
BANK0	
01	RTCCL
02	PCL
03	STATUSL
04	STATUSH
05	IODS
06	PORTB
07	RTCCH
08~1F	General purpose registers

(1) RTCCL (Real Time Counter/Counter Register) : R1

RTCCH (Real Time Counter/Counter Register) : R7

(2) PC (Program Counter) : R2



(3) STATUSL (Status register) : R3

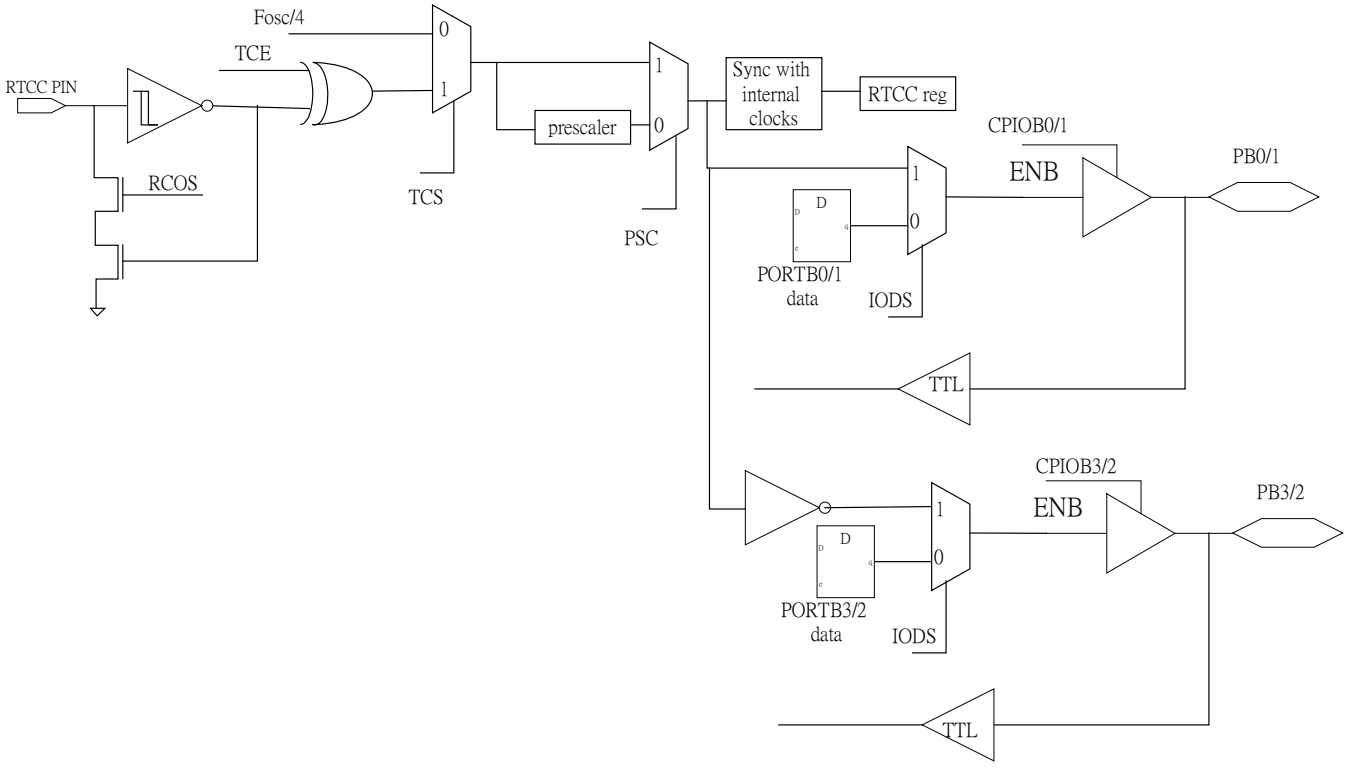
Bit	Symbol	Function
0	TF	WDT Timer overflow Flag bit
1	C	Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit

STATUSH(Status register) : R4

Bit	Symbol	Function
0	——	Unimplemented
1	——	Unimplemented
2	SCALL	0: JUMP (initial) 1: CALL (Change JUMP instruction to CALL instruction. This bit will be clear to zero automatically after CALL was executed)
3	PCWUF	Pin change wake up from sleep

(4) IODS(I/O data select) : R5

Bit	Symbol	Function
0	IODS0	0: Output the PORTB0 register data to PB0(initial) Output the PORTB3 register data to PB3(initial) 1: Output the input clock of RTCC register to PB0 Output the inverted input clock of RTCC register to PB3
1	IODS1	0: Output the PORTB1 register data to PB1(initial) Output the PORTB2 register data to PB2(initial) 1: Output the input clock of RTCC register to PB1 Output the inverted input clock of RTCC register to PB2
2	RCOS	0: RTCC PIN can also be the clock input (initial) 1: RTCC PIN can also be the RC oscillater input
3	——	Unimplemented



(5) PORT B : R6

PB3~PB0, I/O Register

(6) TMRL (Time Mode Register Low Nibble) (only write)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS1—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		

TMRH (Time Mode Register High Nibble) (only write)

Bit	Symbol	Function
0	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin
1	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin
2	PBPHB	PortB pull-high : 0 — Enable 1 — Disable
3	PBWUB	PortB wake-up : 0 — Enable 1 — Disable

(7) CPIO B (Control Port I/O Mode Register)
The CPIO register is “write-only”
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(8) Configurable options for EPROM (Set by writer) :

Oscilltor Type
INTRC 4Mhz
INTRC 8Mhz

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power Edge Detect
PED Disable
PED Enable

Security state
Security Disable
Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-1FF	Program memory
000	The starting address of power on , pin change or WDT time-out reset.

9. Reset Condition for all Registers

Register	Address	Power-On Reset	WDT Reset
RTCCL	01h	xxxx	uuuu
PC	02h	0000	0000
STATUSL	03h	1xx1	#uu#
STATUSH	04h	0000	0000
PORT B	06h	xxxx	uuuu
RTCCH	07h	xxxx	uuuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as "0"

#＝value depends on the condition of the following table

Condition	STATUSH: bit 3	STATUSL: bit 3	STATUSL: bit 0
WDT reset (not during SLEEP)	0	1	0
WDT reset during SLEEP	0	0	0
Wake-up from SLEEP on pin change	1	0	1

10. Instruction Set :

Instruction Code	Mnemonic Operands	Function	Operating	Status
100 0000 0000	NOP	No operation	None	
100 0000 0001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
100 0000 0010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
100 0000 0011	TMODEL	Load W to TMRL register	W→TMRL	None
100 0000 0101	TMODEH	Load W to TMRH register	W→TMRH	None
100 1010 iiii	RTWI	Return,place immediate to W	Stack→PC , I→W	None
100 0000 0rrr	CPIO R	Control I/O port register	W→CPIO r	None
111 100r rrrr	STWR R	Store W to register	W→R	None
1t1 101r rrrr	LDR R, t	Load register	R→t	Z
100 1000 iiii	LDWI I	Load immediate to W	I→W	None
1t1 110r rrrr	ADDWR R, t	Add W and register	W + R→t	C, Z
1t1 111r rrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
1t1 001r rrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
100 0010 iiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
1t1 011r rrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
100 0110 iiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
1t1 010r rrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
100 0100 iiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
1t1 000r rrrr	RRR R, t	Rotate right register	R(n) →R(n-1), 0→R(3), R(0)→x	None
010 0bbr rrrr	BCR R, b	Bit clear	0→R(b)	None
011 0bbr rrrr	BSR R, b	Bit set	1→R(b)	None
010 1bb rrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
011 1bbr rrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
00n nnnn nnnn	JUMP n	JUMP(CALL) to address	n→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMRL	:	Time mode register low nibble			0 : Working register
TMRH	:	TIme mode register high nibble			1 : General register
CPIO	:	Control I/O port register			
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter			
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'			
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (4 bits)
			n	:	Immediate address

11. Oscillator start up timer condition :

Oscillator Type	Power-on reset	Subsequest resets
INTRC	20ms	20ms

12. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} ： 2.5V ~ 5.5 V

Frequency： 4 Hz & 8 MHz

(B) Input Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃

	Port	Min.	Max.
V_{il}	PB3, PB0	V_{ss}	1.0 V
	PB1	V_{ss}	1.0V
	PB2	V_{ss}	1.2V
V_{ih}	PB3, PB0	2.0 V	Vdd
	PB1	3.6 V	V_{dd}
	PB2	3.6 V	V_{dd}

Threshold Voltage :

PB3 & PB0 V_{th}＝1.55V

PB1 V_{il}＝1.1 V, V_{ih}＝3.5 V (Schmitt Trigger)

PB2 V_{il}＝1.4 V, V_{ih}＝3.4 V (Schmitt Trigger)

(C) Output Voltage：

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

PB Port	
I_{oh}＝－20.0 mA	V_{oh}＝3.8 V
I_{ol}＝20.0 mA	V_{ol}＝0.4V
I_{oh}＝－5.0 mA	V_{oh}＝4.5 V
I_{ol}＝5.0 mA	V_{ol}＝0.12 V

*PB1 & PB2 : Output is open drain type.

(D) Leakage Current

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

I_{il}	－ 0.1μA (Max.)
I_{ih}	＋ 0.1μA (Max.)

(E) Sleep Current

@***WDT－Disable***, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.5 V	I_{dd}＜1.0 μA
V_{dd}＝3.0 V	I_{dd}＜1.0 μA
V_{dd}＝4.0 V	I_{dd}＜1.0 μA
V_{dd}＝5.0 V	I_{dd}＜1.0 μA
V_{dd}＝5.5V	I_{dd}＜1.0 μA

@***WDT－Enable***, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.5 V	I_{dd}=1.5 μA
V_{dd}＝3.0 V	I_{dd}＝2.5 μA
V_{dd}＝4.0 V	I_{dd}＝5.0 μA
V_{dd}＝5.0 V	I_{dd}＝10.0 μA
V_{dd}＝5.5 V	I_{dd}＝15.0 μA

(F) Operating Current

Temperature＝25 ℃, the typical value as followings :

(i) WDT－Enable & PED －Enable

Voltage/Frequency	4 M	8 M	Sleep
2.5 V	240uA	255uA	1.5 μA
3.0 V	320uA	360uA	2.5 μA
4.0 V	440uA	470uA	5.0 μA
5.0 V	565uA	610uA	10.0 μA
5.5 V	635uA	700uA	15.0 μA

(G) The basic WDT time-out cycle time

@ Vdd=5.0v ,Temperature＝25 ℃, the typical value as followings :

Voltage (V)	Basic WDT time-out cycle time (ms)
2.5	26.6
3.0	24.0
4.0	21.2
5.0	19.4
5.5	18.8