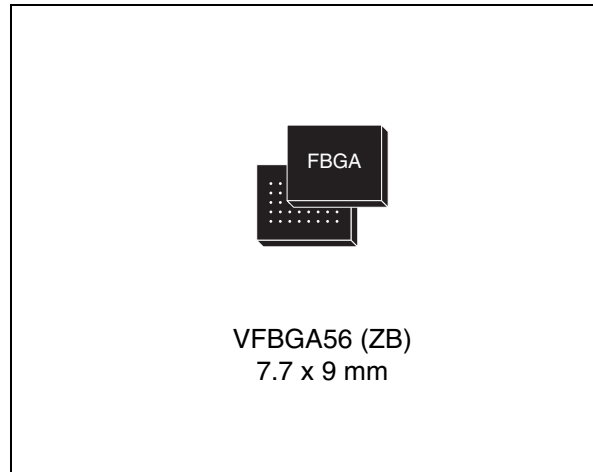


Feature summary

- Supply voltage
 - $V_{DD} = 1.7V$ to $2V$ for Program, Erase and Read
 - $V_{DDQ} = 1.7V$ to $2.24V$ for I/O Buffers
 - $V_{PP} = 12V$ for fast Program (optional)
- Synchronous / Asynchronous Read
 - Synchronous Burst Read mode: 66MHz
 - Asynchronous/ Synchronous Page Read mode
 - Random access: 60ns, 70ns, 80ns
- Synchronous Burst Read Suspend
- Programming time
 - $8\mu s$ by Word typical for Fast Factory Program
 - Double/Quadruple Word Program option
 - Enhanced Factory Program options
- Memory blocks
 - Multiple Bank memory array: 4 Mbit Banks
 - Parameter blocks (top or bottom location)
- Dual operations
 - Program Erase in one bank while Read in others
 - No delay between Read and Write operations
- Block locking
 - All blocks locked at Power up
 - Any combination of blocks can be locked
 - \overline{WP} for Block Lock-Down
- Security
 - 128 bit user programmable OTP cells
 - 64 bit unique device number
- Common Flash Interface (CFI)
- 100,000 program/erase cycles per block



- Electronic signature
 - Manufacturer Code: 20h
 - Device Codes:
 - M58WR016QT (Top): 8812h.
 - M58WR016QB (Bottom): 8813h
 - M58WR032QT (Top): 8814h
 - M58WR032QB (Bottom): 8815h
- ECOPACK® package available

Contents

1	Summary description	8
2	Signal descriptions	14
2.1	Address Inputs (A0-Amax)	14
2.2	Data Input/Output (DQ0-DQ15)	14
2.3	Chip Enable (\bar{E})	14
2.4	Output Enable (\bar{G})	14
2.5	Write Enable (\bar{W})	14
2.6	Write Protect (\bar{WP})	14
2.7	Reset (\bar{RP})	15
2.8	Latch Enable (\bar{L})	15
2.9	Clock (K)	15
2.10	Wait (WAIT)	15
2.11	V _{DD} supply voltage	15
2.12	V _{DDQ} supply voltage	15
2.13	V _{PP} Program supply voltage	16
2.14	V _{SS} Ground	16
2.15	V _{SSQ} Ground	16
3	Bus operations	17
3.1	Bus Read	17
3.2	Bus Write	17
3.3	Address Latch	17
3.4	Output Disable	17
3.5	Standby	18
3.6	Reset	18
4	Command interface	19
5	Command interface - standard commands	20
5.1	Read Array command	20
5.2	Read Status Register command	20

5.3	Read Electronic Signature command	20
5.4	Read CFI Query command	21
5.5	Clear Status Register command	21
5.6	Block Erase command	22
5.7	Program command	22
5.8	Program/Erase Suspend command	23
5.9	Program/Erase Resume command	23
5.10	Protection Register Program command	24
5.11	Set Configuration Register command	24
5.12	Block Lock command	25
5.13	Block Unlock command	25
5.14	Block Lock-Down command	25
6	Command interface - factory program commands	28
6.1	Bank Erase command	28
6.2	Double Word Program command	29
6.3	Quadruple Word Program command	30
6.4	Enhanced Factory Program command	30
6.4.1	Setup Phase	31
6.4.2	Program Phase	31
6.4.3	Verify Phase	32
6.4.4	Exit Phase	32
6.5	Quadruple Enhanced Factory Program command	32
6.5.1	Setup Phase	33
6.5.2	Load Phase	33
6.5.3	Program and Verify Phase	33
6.5.4	Exit Phase	33
7	Status Register	35
7.0.1	Program/Erase Controller Status Bit (SR7)	35
7.0.2	Erase Suspend Status Bit (SR6)	35
7.0.3	Erase Status Bit (SR5)	36
7.0.4	Program Status Bit (SR4)	36
7.0.5	V _{PP} Status Bit (SR3)	36
7.0.6	Program Suspend Status Bit (SR2)	37

7.0.7	Block Protection Status Bit (SR1)	37
7.0.8	Bank Write/Multiple Word Program Status Bit (SR0)	37
8	Configuration Register	39
8.1	Read Select Bit (CR15)	39
8.2	X-Latency Bits (CR13-CR11)	39
8.3	Wait Polarity Bit (CR10)	40
8.4	Data Output Configuration Bit (CR9)	40
8.5	Wait Configuration Bit (CR8)	40
8.6	Burst Type Bit (CR7)	40
8.7	Valid Clock Edge Bit (CR6)	40
8.8	Wrap Burst Bit (CR3)	40
8.9	Burst length Bits (CR2-CR0)	41
9	Read modes	46
9.1	Asynchronous Read mode	46
9.2	Synchronous Burst Read mode	47
9.2.1	Synchronous Burst Read Suspend	48
9.3	Single Synchronous Read mode	48
10	Dual operations and Multiple Bank architecture	49
11	Block locking	51
11.1	Reading a Block's lock status	51
11.2	Locked state	51
11.3	Unlocked state	51
11.4	Lock-Down state	52
11.5	Locking operations during Erase Suspend	52
12	Program and erase times and endurance cycles	54
13	Maximum rating	56
14	DC and AC parameters	57
15	Package mechanical	73

16	Part numbering	74
	Appendix A Block address tables	76
	Appendix B Common Flash Interface	83
	Appendix C Flowcharts and pseudo codes	93
	C.1 Enhanced Factory Program pseudo code	102
	C.2 Quadruple Enhanced Factory Program Pseudo Code	104
	Appendix D Command interface state tables	105
17	Revision history	109

List of tables

Table 1.	Signal names	10
Table 2.	M58WR016QT/B Bank architecture	11
Table 3.	M58WR032QT/B Bank architecture	12
Table 4.	Bus operations	18
Table 5.	Command codes	19
Table 6.	Standard commands	26
Table 7.	Electronic signature codes	27
Table 8.	Factory Program commands	34
Table 9.	Status Register bits	38
Table 10.	Configuration Register bits	42
Table 11.	Burst type definition	43
Table 12.	Dual operations allowed in other banks	49
Table 13.	Dual operations allowed in same bank	50
Table 14.	Lock status	53
Table 15.	Program/Erase times and endurance cycles	54
Table 16.	Absolute maximum ratings	56
Table 17.	Operating and AC measurement conditions	57
Table 18.	Capacitance	58
Table 19.	DC characteristics - currents	59
Table 20.	DC characteristics - voltages	60
Table 21.	Asynchronous Read AC characteristics	63
Table 22.	Synchronous Read AC characteristics	67
Table 23.	Write AC characteristics, Write Enable controlled	69
Table 24.	Write AC characteristics, Chip Enable controlled	71
Table 25.	Reset and Power-up AC characteristics	72
Table 26.	VFBGA56 - 7.7x9mm, 8x7 ball array, 0.75mm pitch, package mechanical data	73
Table 27.	Ordering information scheme	74
Table 28.	Daisy chain ordering scheme	75
Table 29.	Top boot block addresses, M58WR016QT	76
Table 30.	Bottom boot block addresses, M58WR016QB	77
Table 31.	Top boot block addresses, M58WR032QT	78
Table 32.	Bottom boot block addresses, M58WR032QB	80
Table 33.	Query structure overview	83
Table 34.	CFI Query identification string	84
Table 35.	CFI query system interface information	85
Table 36.	Device geometry definition	86
Table 37.	Primary algorithm-specific extended query table	87
Table 38.	Protection Register Information	88
Table 39.	Burst Read information	88
Table 40.	Bank and erase block region information	88
Table 41.	Bank and erase block region 1 information	89
Table 42.	Bank and erase block region 2 information	91
Table 43.	Command interface states - modify table, next state	105
Table 44.	Command interface states - modify table, next output state	106
Table 45.	Command interface states - lock table, next state	107
Table 46.	Command interface states - lock table, next output state	108
Table 47.	Document revision history	109

List of figures

Figure 1.	Logic Diagram	10
Figure 2.	VFBGA Connections (Top view through package)	11
Figure 3.	M58WR016QT/B memory map	12
Figure 4.	M58WR032QT/B memory map	13
Figure 5.	Protection Register Memory Map	27
Figure 6.	X-Latency and data output configuration example	44
Figure 7.	Wait configuration example	45
Figure 8.	AC measurement I/O waveform	57
Figure 9.	AC measurement load circuit	58
Figure 10.	Asynchronous Random Access Read AC waveforms	61
Figure 11.	Asynchronous Page Read AC waveforms	62
Figure 12.	Synchronous Burst Read AC waveforms	64
Figure 13.	Single Synchronous Read AC waveforms	65
Figure 14.	Synchronous Burst Read Suspend AC waveforms	66
Figure 15.	Clock input AC waveform	67
Figure 16.	Write AC waveforms, Write Enable controlled	68
Figure 17.	Write AC waveforms, Chip Enable controlled	70
Figure 18.	Reset and Power-up AC waveforms	72
Figure 19.	VFBGA56 - 7.7x9mm, 8x7 ball array, 0.75mm pitch, Bottom View Package Outline	73
Figure 20.	Program flowchart and pseudo code	93
Figure 21.	Double Word Program flowchart and pseudo code	94
Figure 22.	Quadruple Word Program flowchart and pseudo code	95
Figure 23.	Program Suspend & Resume flowchart and pseudo code	96
Figure 24.	Block Erase flowchart and pseudo code	97
Figure 25.	Erase Suspend & Resume flowchart and pseudo code	98
Figure 26.	Locking operations flowchart and pseudo code	99
Figure 27.	Protection Register Program flowchart and pseudo code	100
Figure 28.	Enhanced Factory Program flowchart	101
Figure 29.	Quadruple Enhanced Factory Program flowchart	103

1 Summary description

The M58WR016QT/B and M58WR032QT/B are 16 Mbit (1 Mbit x16) and 32 Mbit (2 Mbit x16) non-volatile Flash memories, respectively. They will be referred to as M58WRxxxQT/B throughout the document unless otherwise specified.

The M58WRxxxQT/B may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.7V to 2V V_{DD} supply for the circuitry and a 1.7V to 2.24V V_{DDQ} supply for the Input/Output pins. An optional 12V V_{PP} power supply is provided to speed up customer programming.

The V_{PP} pin can also be used as a control pin to provide absolute protection against program or erase.

The device features an asymmetrical block architecture.

- M58WR016QT/B has an array of 39 blocks, and is divided into 4 Mbit banks. There are 3 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords.
- M58WR032QT/B has an array of 71 blocks, and is divided into 4 Mbit banks. There are 7 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords.

The Multiple Bank Architecture allows Dual Operations, while programming or erasing in one bank, Read operations are possible in other banks. Only one bank at a time is allowed to be in Program or Erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architectures are summarized in [Table 2](#) and [Table 3](#), and the memory maps are shown in [Figure 3](#) and [Figure 4](#). The Parameter Blocks are located at the top of the memory address space for the M58WR016QT and M58WR032QT, and at the bottom for the M58WR016QB and M58WR032QB.

Each block can be erased separately. Erase can be suspended, in order to perform program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage V_{DD} . There are two Enhanced Factory programming commands available to speed up programming.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 66MHz. The synchronous burst read operation can be suspended and resumed.

The device features an Automatic Standby mode. When the bus is inactive during Asynchronous Read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value I_{DD4} and the outputs are still driven.

The M58WRxxxQT/B features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually

preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power-Up.

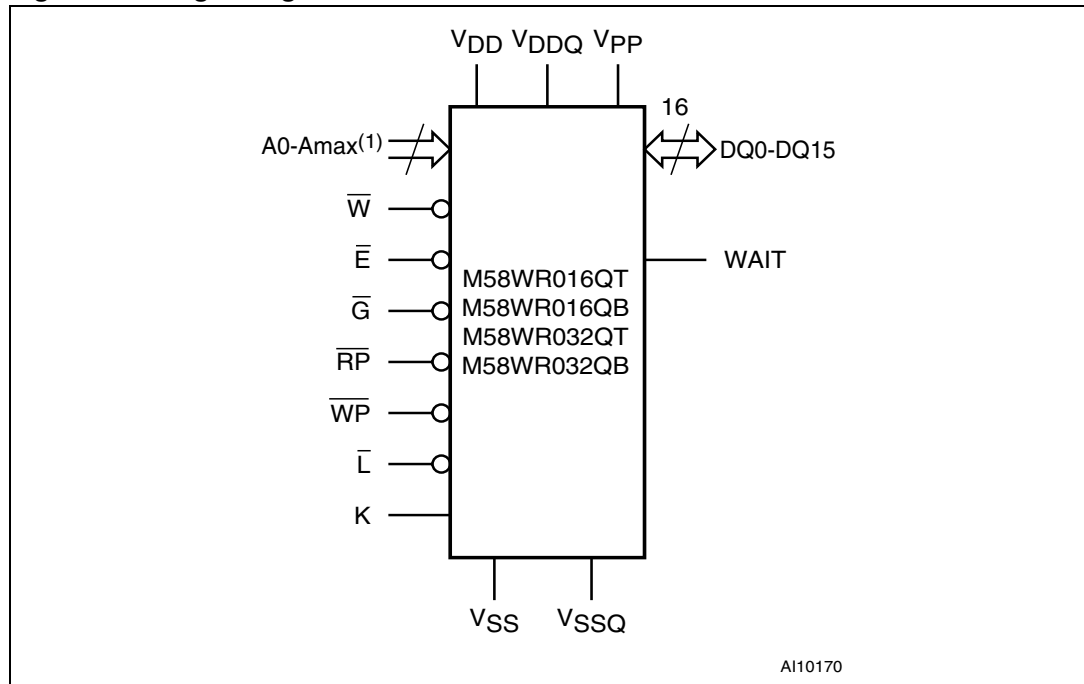
The device includes a Protection Register to increase the protection of a system's design. The Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by Numonyx, and a 128 bit segment One-Time-Programmable (OTP) by the user. The user programmable segment can be permanently protected. [Figure 5](#) shows the Protection Register Memory Map.

The memory is offered in a VFBGA56, 7.7 x 9mm, 8x7 active ball array, 0.75 mm pitch package and is supplied with all the bits erased (set to '1').

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 1. Logic Diagram



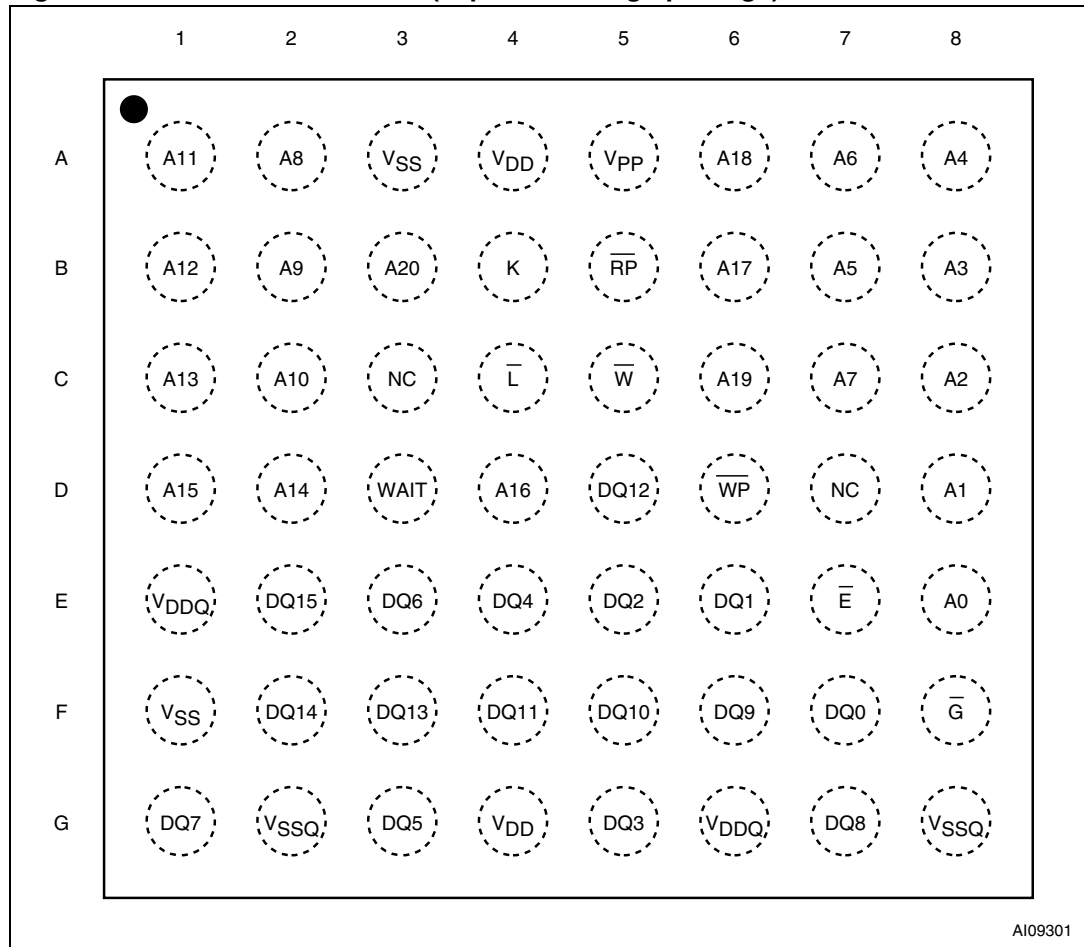
1. Amax is equal to A19 for the M58WR016QT/B and to A20 for the M58WR032QT/B.

Table 1. Signal names

A0-Amax ⁽¹⁾	Address Inputs
DQ0-DQ15	Data Input/Outputs, Command Inputs
E	Chip Enable
G	Output Enable
W	Write Enable
RP	Reset
WP	Write Protect
K	Clock
L	Latch Enable
WAIT	Wait
V _{DD}	Supply Voltage
V _{DDQ}	Supply Voltage for Input/Output Buffers
V _{PP}	Optional Supply Voltage for Fast Program & Erase
V _{SS}	Ground
V _{SSQ}	Ground Input/Output Supply
NC	Not Connected Internally

1. Amax is equal to A19 for the M58WR016QT/B and to A20 for the M58WR032QT/B.

Figure 2. VFBGA Connections (Top view through package)



1. Ball B3 is A20 in the M58WR032QT/B and it is Not Connected internally (NC) in the M58WR016QT/B.

Table 2. M58WR016QT/B Bank architecture

Number	Bank Size	Parameter Blocks	Main Blocks
Parameter Bank	4 Mbits	8 blocks of 4 KWords	7 blocks of 32 KWords
Bank 1	4 Mbits	-	8 blocks of 32 KWords
Bank 2	4 Mbits	-	8 blocks of 32 KWords
Bank 3	4 Mbits	-	8 blocks of 32 KWords

Table 3. M58WR032QT/B Bank architecture

Number	Bank Size	Parameter Blocks	Main Blocks
Parameter Bank	4 Mbits	8 blocks of 4 KWords	7 blocks of 32 KWords
Bank 1	4 Mbits	-	8 blocks of 32 KWords
Bank 2	4 Mbits	-	8 blocks of 32 KWords
Bank 3	4 Mbits	-	8 blocks of 32 KWords
⋮	⋮	⋮	⋮
Bank 6	4 Mbits	-	8 blocks of 32 KWords
Bank 7	4 Mbits	-	8 blocks of 32 KWords

Figure 3. M58WR016QT/B memory map

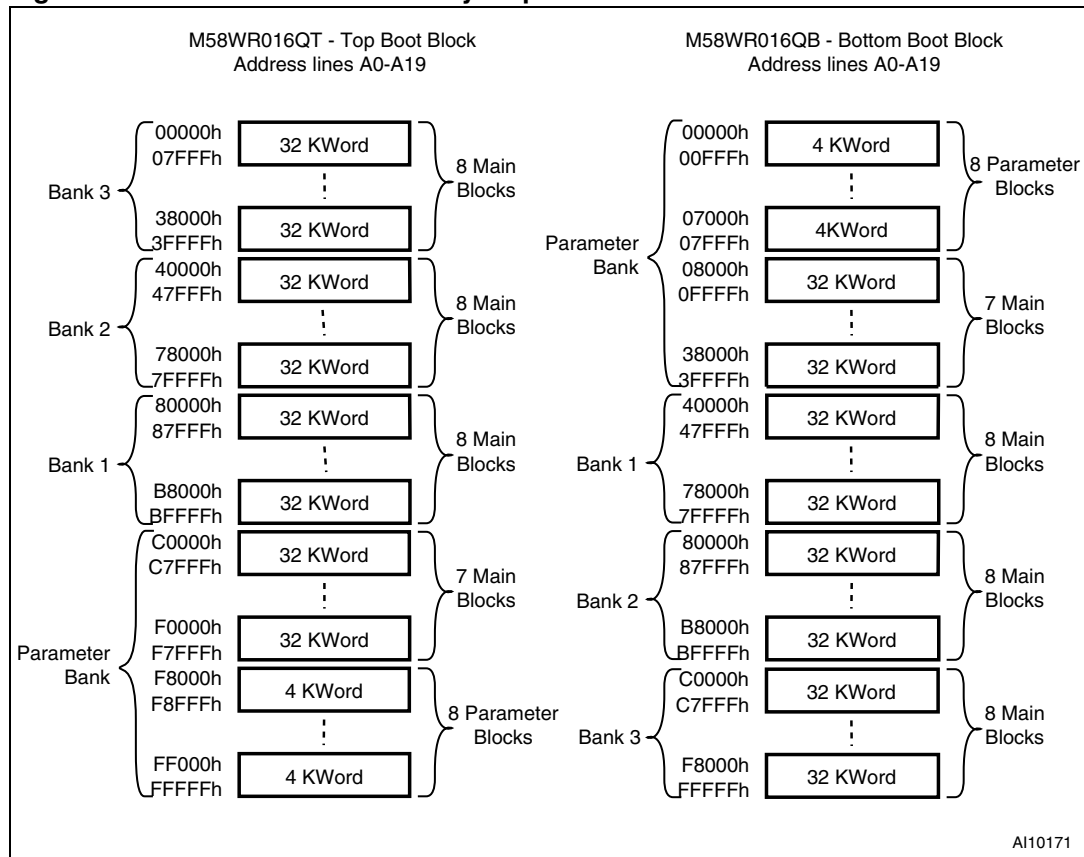
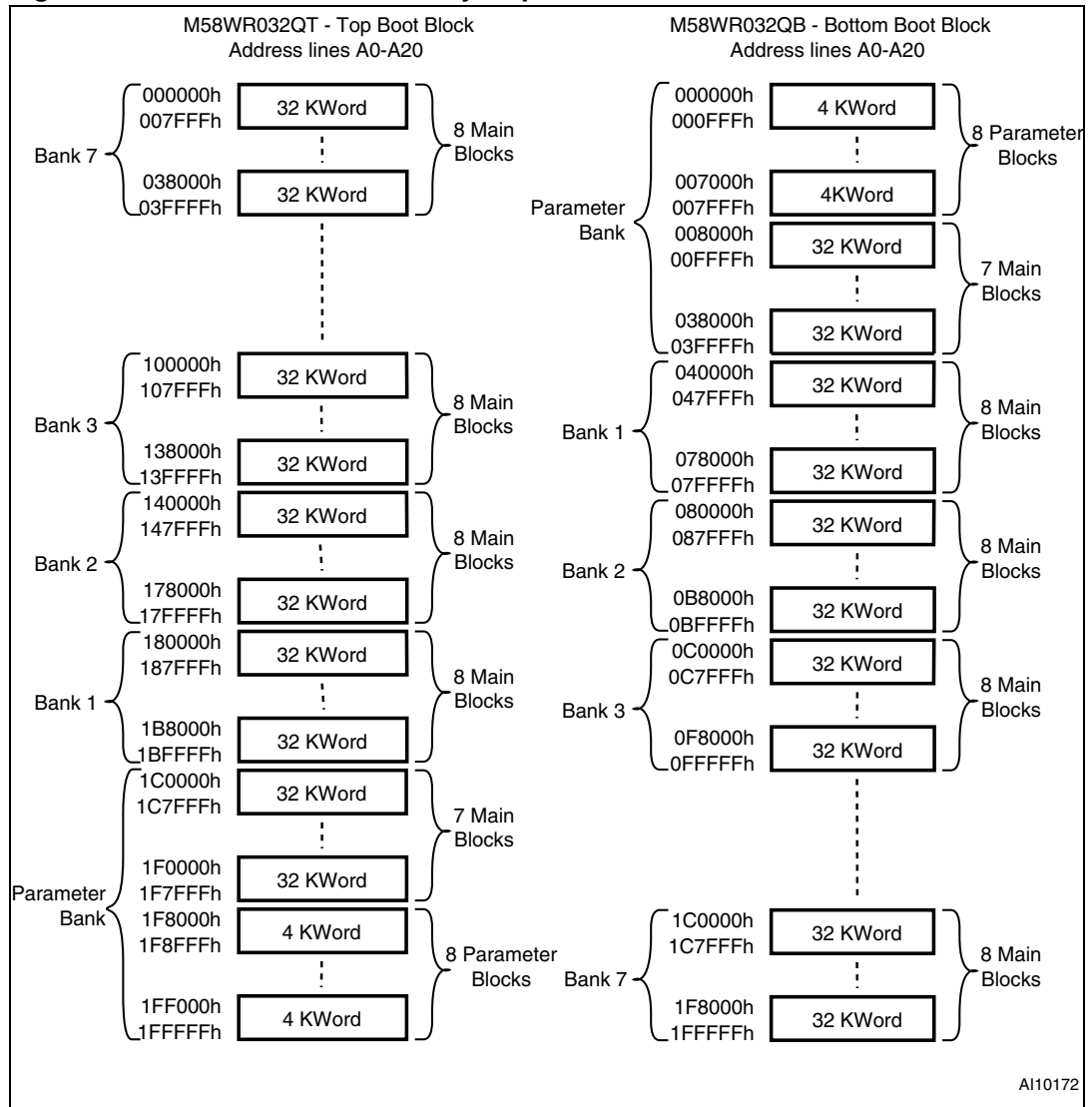


Figure 4. M58WR032QT/B memory map



2 Signal descriptions

See [Figure 1: Logic Diagram](#) and [Table 1: Signal names](#), for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-Amax)

Amax is equal to A19 in the M58WR016QT/B and to A20 in the M58WR032QT/B.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

2.2 Data Input/Output (DQ0-DQ15)

The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Bus Write operation.

2.3 Chip Enable (\overline{E})

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

2.4 Output Enable (\overline{G})

The Output Enable controls data outputs during the Bus Read operation of the memory.

2.5 Write Enable (\overline{W})

The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.6 Write Protect (\overline{WP})

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL} , the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH} , the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (refer to [Table 14: Lock status](#)).

2.7 Reset (\overline{RP})

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL} , the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2} . Refer to [Table 19: DC characteristics - currents](#) for the value of I_{DD2} . After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH} , the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to [Table 20: DC characteristics - voltages](#)).

2.8 Latch Enable (\overline{L})

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH} . Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.9 Clock (K)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL} . Clock is don't care during asynchronous read and in write operations.

2.10 Wait (WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH} or Reset is at V_{IL} . It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT signal is not gated by Output Enable.

2.11 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

2.12 V_{DDQ} supply voltage

V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD} . V_{DDQ} can be tied to V_{DD} or can use a separate supply.

2.13 V_{PP} Program supply voltage

V_{PP} is a power supply pin. The Supply Voltage V_{DD} and the Program Supply Voltage V_{PP} can be applied in any order. The pin can also be used as a control input.

The two functions are selected by the voltage range applied to the pin. If V_{PP} is kept in a low voltage range (0V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than $V_{PP_{LK}}$ gives an absolute protection against program or erase, while V_{PP} in the V_{PP1} range enables these functions (see Tables 19 and 20, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed.

2.14 V_{SS} Ground

V_{SS} ground is the reference for the core supply. It must be connected to the system ground.

2.15 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ} . V_{SSQ} must be connected to V_{SS} .

Note: Each device in a system should have V_{DD} , V_{DDQ} and V_{PP} decoupled with a 0.1 μ F ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See [Figure 9: AC measurement load circuit](#). The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

3 Bus operations

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Address Latch, Output Disable, Standby and Reset. See [Table 4: Bus operations](#), for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

3.1 Bus Read

Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See [Figures 10, 11, 12 and 13](#) Read AC Waveforms, and [Tables 21 and 22](#) Read AC Characteristics, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write Commands to the memory or latch Input Data to be programmed. A bus write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH} . Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses can also be latched prior to the write operation by toggling Latch Enable. In this case the Latch Enable should be tied to V_{IH} during the bus write operation.

See [Figures 16 and 17](#), Write AC Waveforms, and [Tables 23 and 24](#), Write AC Characteristics, for details of the timing requirements.

3.3 Address Latch

Address latch operations input valid addresses. Both Chip enable and Latch Enable must be at V_{IL} during address latch operations. The addresses are latched on the rising edge of Latch Enable.

3.4 Output Disable

The outputs are high impedance when the Output Enable is at V_{IH} .

3.5 Standby

Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable and Reset are at V_{IH} . The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

3.6 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL} . The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Table 4. Bus operations⁽¹⁾

Operation	\bar{E}	\bar{G}	\bar{W}	\bar{L}	\bar{RP}	WAIT ⁽²⁾	DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IL} ⁽³⁾	V_{IH}		Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IL} ⁽³⁾	V_{IH}		Data Input
Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}		Data Output or Hi-Z ⁽⁴⁾
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Hi-Z
Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z	Hi-Z
Reset	X	X	X	X	V_{IL}	Hi-Z	Hi-Z

1. X = Don't care.
2. WAIT signal polarity is configured using the Set Configuration Register command.
3. \bar{L} can be tied to V_{IH} if the valid address has been previously latched.
4. Depends on \bar{G} .

4 Command interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface is reset to read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO} . Command sequences must be followed exactly. Any invalid combination of commands will be ignored.

Refer to [Table 5: Command codes](#) and [Appendix D](#), Tables [43](#), [44](#), [45](#) and [46](#), Command Interface States - Modify and Lock Tables, for a summary of the Command Interface.

The Command Interface is split into two types of commands: Standard commands and Factory Program commands. The following sections explain in detail how to perform each command.

Table 5. Command codes

Hex Code	Command
01h	Block Lock Confirm
03h	Set Configuration Register Confirm
10h	Alternative Program Setup
20h	Block Erase Setup
2Fh	Block Lock-Down Confirm
30h	Enhanced Factory Program Setup
35h	Double Word Program Setup
40h	Program Setup
50h	Clear Status Register
56h	Quadruple Word Program Setup
60h	Block Lock Setup, Block Unlock Setup, Block Lock Down Setup and Set Configuration Register Setup
70h	Read Status Register
75h	Quadruple Enhanced Factory Program Setup
80h	Bank Erase Setup
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
C0h	Protection Register Program
D0h	Program/Erase Resume, Block Erase Confirm, Bank Erase Confirm, Block Unlock Confirm or Enhanced Factory Program Confirm
FFh	Read Array

5 Command interface - standard commands

The following commands are the basic commands used to read, write to and configure the device. Refer to [Table 6: Standard commands](#), in conjunction with the following text descriptions.

5.1 Read Array command

The Read Array command returns the addressed bank to Read Array mode. One Bus Write cycle is required to issue the Read Array command and return the addressed bank to Read Array mode. Subsequent read operations will read the addressed location and output the data. A Read Array command can be issued in one bank while programming or erasing in another bank. However if a Read Array command is issued to a bank currently executing a Program or Erase operation the command will be executed but the output data is not guaranteed.

5.2 Read Status Register command

The Status Register indicates when a Program or Erase operation is complete and the success or failure of operation itself. Issue a Read Status Register command to read the Status Register content. The Read Status Register command can be issued at any time, even during Program or Erase operations.

The following read operations output the content of the Status Register of the addressed bank. The Status Register is latched on the falling edge of \bar{E} or \bar{G} signals, and can be read until \bar{E} or \bar{G} returns to V_{IH} . Either \bar{E} or \bar{G} must be toggled to update the latched data. See [Table 9](#) for the description of the Status Register Bits. This mode supports asynchronous or single synchronous reads only.

5.3 Read Electronic Signature command

The Read Electronic Signature command reads the Manufacturer and Device Codes, the Block Locking Status, the Protection Register, and the Configuration Register.

The Read Electronic Signature command consists of one write cycle to an address within one of the banks. A subsequent Read operation in the same bank will output the Manufacturer Code, the Device Code, the protection Status of the blocks in the targeted bank, the Protection Register, or the Configuration Register (see [Table 7](#)).

If a Read Electronic Signature command is issued in a bank that is executing a Program or Erase operation the bank will go into Read Electronic Signature mode, subsequent Bus Read cycles will output the Electronic Signature data and the Program/Erase controller will continue to program or erase in the background. This mode supports asynchronous or single synchronous reads only, it does not support page mode or synchronous burst reads.

5.4 Read CFI Query command

The Read CFI Query command is used to read data from the Common Flash Interface (CFI). The Read CFI Query Command consists of one Bus Write cycle, to an address within one of the banks. Once the command is issued subsequent Bus Read operations in the same bank read from the Common Flash Interface.

If a Read CFI Query command is issued in a bank that is executing a Program or Erase operation the bank will go into Read CFI Query mode, subsequent Bus Read cycles will output the CFI data and the Program/Erase controller will continue to Program or Erase in the background. This mode supports asynchronous or single synchronous reads only, it does not support page mode or synchronous burst reads.

The status of the other banks is not affected by the command (see [Table 12](#)). After issuing a Read CFI Query command, a Read Array command should be issued to the addressed bank to return the bank to Read Array mode.

See [Appendix B](#), Tables [33](#), [34](#), [35](#), [36](#), [37](#), [38](#), [39](#), [40](#), [41](#) and [42](#) for details on the information contained in the Common Flash Interface memory area.

5.5 Clear Status Register command

The Clear Status Register command can be used to reset (set to '0') error bits SR1, SR3, SR4 and SR5 in the Status Register. One bus write cycle is required to issue the Clear Status Register command. The Clear Status Register command does not change the Read mode of the bank.

The error bits in the Status Register do not automatically return to '0' when a new command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

5.6 Block Erase command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error. The Block Erase command can be issued at any moment, regardless of whether the block has been programmed or not.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits SR4 and SR5 are set and the command aborts. Erase aborts if Reset turns to V_{IL} . As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register mode until a Read Array, Read CFI Query or Read Electronic Signature command is issued.

During Erase operations the bank containing the block being erased will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command, all other commands will be ignored. Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being erased. Typical Erase times are given in [Table 15: Program/Erase times and endurance cycles](#).

See [Appendix C, Figure 24: Block Erase flowchart and pseudo code](#), for a suggested flowchart for using the Block Erase command.

5.7 Program command

The memory array can be programmed Word-by-Word. Only one Word in one bank can be programmed at any one time. If the block is protected, the program operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

After programming has started, read operations in the bank being programmed output the Status Register content.

During Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command. Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being programmed. Typical Program times are given in [Table 15: Program/Erase times and endurance cycles](#).

Programming aborts if Reset goes to V_{IL} . As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be reprogrammed.

See [Appendix C, Figure 20: Program flowchart and pseudo code](#), for the flowchart for using the Program command.

5.8 Program/Erase Suspend command

The Program/Erase Suspend command is used to pause a Program or Block Erase operation. A Bank Erase operation cannot be suspended.

One bus write cycle is required to issue the Program/Erase command. Once the Program/Erase Controller has paused bits SR7, SR6 and/ or SR2 of the Status Register will be set to '1'. The command can be addressed to any bank.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array (cannot read the erase-suspended block or the program-suspended Word), Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Clear status Register, Program, Block Lock, Block Lock-Down or Block Unlock commands will also be accepted. The block being erased may be protected by issuing the Block Lock, Block Lock-Down or Protection Register Program commands. Only the blocks not being erased may be read or programmed correctly. When the Program/Erase Resume command is issued the operation will complete. Refer to the Dual Operations section for detailed information about simultaneous operations allowed during Program/Erase Suspend.

During a Program/Erase Suspend, the device can be placed in standby mode by taking Chip Enable to V_{IH} . Program/Erase is aborted if Reset turns to V_{IL} .

See [Appendix C, Figure 23: Program Suspend & Resume flowchart and pseudo code](#), and [Figure 25: Erase Suspend & Resume flowchart and pseudo code](#) for flowcharts for using the Program/Erase Suspend command.

5.9 Program/Erase Resume command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend command has paused it. One Bus Write cycle is required to issue the command. The command can be written to any address.

The Program/Erase Resume command does not change the read mode of the banks. If the suspended bank was in Read Status Register, Read Electronic signature or Read CFI Query mode the bank remains in that mode and outputs the corresponding data. If the bank was in Read Array mode subsequent read operations will output invalid data.

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the programming operation has completed. It is possible to accumulate suspend operations. For example: suspend an erase operation, start a programming operation, suspend the programming operation then read the array. See [Appendix C, Figure 23: Program Suspend & Resume flowchart and pseudo code](#), and [Figure 25: Erase Suspend & Resume flowchart and pseudo code](#), for flowcharts for using the Program/Erase Resume command.

5.10 Protection Register Program command

The Protection Register Program command is used to Program the 128 bit user One-Time-Programmable (OTP) segment of the Protection Register and the Protection Register Lock. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register (see [Figure 5: Protection Register Memory Map](#)). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register is not reversible.

The Protection Register Program cannot be suspended. See [Appendix C, Figure 27: Protection Register Program flowchart and pseudo code](#), for a flowchart for using the Protection Register Program command.

5.11 Set Configuration Register command

The Set Configuration Register command is used to write a new value to the Configuration Register which defines the burst length, type, X latency, Synchronous/Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Configuration Register command.

- The first cycle writes the setup command and the address corresponding to the Configuration Register content.
- The second cycle writes the Configuration Register data and the confirm command.

Read operations output the memory array content after the Set Configuration Register command is issued.

The value for the Configuration Register is always presented on A0-A15. CR0 is on A0, CR1 on A1, etc.; the other address bits are ignored.

5.12 Block Lock command

The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. [Table 14](#) shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware reset or power-down/power-up. They are cleared by a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation. See [Appendix C, Figure 26: Locking operations flowchart and pseudo code](#), for a flowchart for using the Lock command.

5.13 Block Unlock command

The Block Unlock command is used to unlock a block, allowing the block to be programmed or erased. Two Bus Write cycles are required to issue the Block Unlock command.

- The first bus cycle sets up the Block Unlock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. [Table 14](#) shows the protection status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation and [Appendix C, Figure 26: Locking operations flowchart and pseudo code](#), for a flowchart for using the Unlock command.

5.14 Block Lock-Down command

A locked or unlocked block can be locked-down by issuing the Block Lock-Down command. A locked-down block cannot be programmed or erased, or have its protection status changed when \overline{WP} is low, V_{IL} . When \overline{WP} is high, V_{IH} , the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Two Bus Write cycles are required to issue the Block Lock-Down command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Locked-Down blocks revert to the locked (and not locked-down) state when the device is reset on power-down. [Table 14](#) shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation and [Appendix C, Figure 26: Locking operations flowchart and pseudo code](#), for a flowchart for using the Lock-Down command.

Table 6. Standard commands⁽¹⁾

Commands	Cycles	Bus Operations					
		1st Cycle			2nd Cycle		
		Op.	Add	Data	Op.	Add	Data
Read Array	1+	Write	BKA	FFh	Read	WA	RD
Read Status Register	1+	Write	BKA	70h	Read	BKA ⁽²⁾	SRD
Read Electronic Signature	1+	Write	BKA	90h	Read	BKA ⁽²⁾	ESD
Read CFI Query	1+	Write	BKA	98h	Read	BKA ⁽²⁾	QD
Clear Status Register	1	Write	X	50h			
Block Erase	2	Write	BKA or BA ⁽³⁾	20h	Write	BA	D0h
Program	2	Write	BKA or WA ⁽³⁾	40h or 10h	Write	WA	PD
Program/Erase Suspend	1	Write	X	B0h			
Program/Erase Resume	1	Write	X	D0h			
Protection Register Program	2	Write	PRA	C0h	Write	PRA	PRD
Set Configuration Register	2	Write	CRD	60h	Write	CRD	03h
Block Lock	2	Write	BKA or BA ⁽³⁾	60h	Write	BA	01h
Block Unlock	2	Write	BKA or BA ⁽³⁾	60h	Write	BA	D0h
Block Lock-Down	2	Write	BKA or BA ⁽³⁾	60h	Write	BA	2Fh

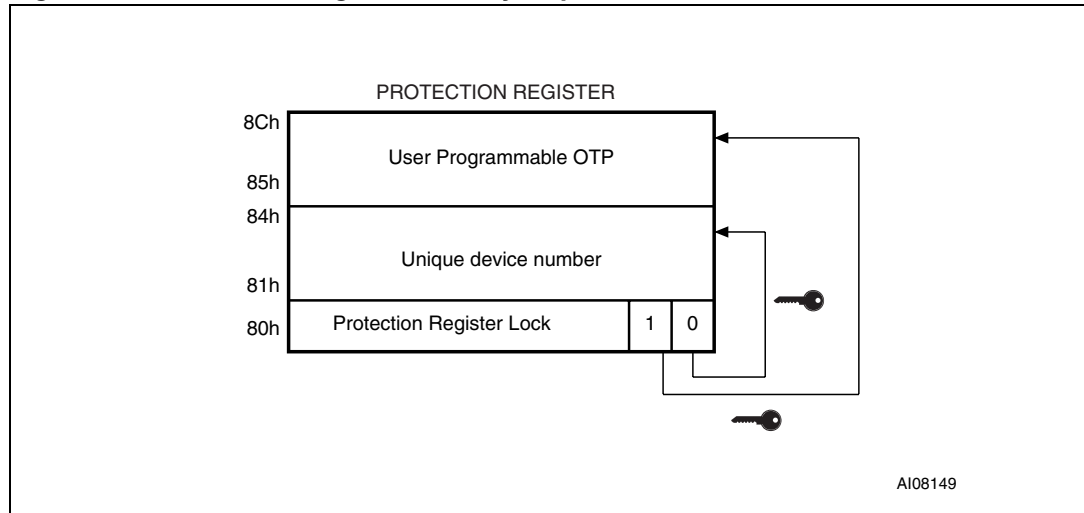
1. X = Don't Care, WA=Word Address in targeted bank, RD=Read Data, SRD=Status Register Data, ESD=Electronic Signature Data, QD=Query Data, BA=Block Address, BKA= Bank Address, PD=Program Data, PRA=Protection Register Address, PRD=Protection Register Data, CRD=Configuration Register Data.
2. Must be same bank as in the first cycle. The signature addresses are listed in [Table 7](#).
3. Any address within the bank can be used.

Table 7. Electronic signature codes

Code		Address (h)	Data (h)
Manufacturer Code		Bank Address + 00	0020
Device Code	Top	Bank Address + 01	8812h (M58WR016QT) 8814h (M58WR032QT)
	Bottom	Bank Address + 01	8813h (M58WR016QB) 8815h (M58WR032QB)
Block Protection	Locked	Block Address + 02	0001
	Unlocked		0000
	Locked and Locked-Down		0003
	Unlocked and Locked-Down		0002
Reserved		Bank Address + 03	Reserved
Configuration Register		Bank Address + 05	CR ⁽¹⁾
Protection Register Lock	Numonyx Factory Default	Bank Address + 80	0002
	OTP Area Permanently Locked		0000
Protection Register		Bank Address + 81 Bank Address + 84	Unique Device Number
		Bank Address + 85 Bank Address + 8C	OTP Area

1. CR = Configuration Register.

Figure 5. Protection Register Memory Map



6 Command interface - factory program commands

The Factory Program commands are used to speed up programming. They require V_{PP} to be at V_{PPH} except for the Bank Erase command which also operates at $V_{PP} = V_{DD}$. Refer to [Table 8: Factory Program commands](#), in conjunction with the following text descriptions.

The use of Factory Program commands requires certain operating conditions.

- V_{PP} must be set to V_{PPH} (except for Bank Erase command),
- V_{DD} must be within operating range,
- Ambient temperature, T_A must be $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$,
- The targeted block must be unlocked.

6.1 Bank Erase command

The Bank Erase command can be used to erase a bank. It sets all the bits within the selected bank to '1'. All previous data in the bank is lost. The Bank Erase command will ignore any protected blocks within the bank. If all blocks in the bank are protected then the Bank Erase operation will abort and the data in the bank will not be changed. The Status Register will not output any error.

Bank Erase operations can be performed at both $V_{PP} = V_{PPH}$ and $V_{PP} = V_{DD}$.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Bank Erase command.
- The second latches the bank address in the internal state machine and starts the Program/Erase Controller.

If the second bus cycle is not Write Bank Erase Confirm (D0h), Status Register bits SR4 and SR5 are set and the command aborts. Erase aborts if Reset turns to V_{IL} . As data integrity cannot be guaranteed when the Erase operation is aborted, the bank must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register mode until a Read Array, Read CFI Query or Read Electronic Signature command is issued.

During Bank Erase operations the bank being erased will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored.

For optimum performance, Bank Erase commands should be limited to a maximum of 100 Program/Erase cycles per Block. After 100 Program/Erase cycles the internal algorithm will still operate properly but some degradation in performance may occur.

Dual Operations are not supported during Bank Erase operations and the command cannot be suspended.

Typical Erase times are given in [Table 15: Program/Erase times and endurance cycles](#).

6.2 Double Word Program command

The Double Word Program command improves the programming throughput by writing a page of two adjacent words in parallel. The two words must differ only for the address A0. If the block is protected, the Double Word Program operation will abort, the data in the block will not be changed and the Status Register will output the error.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations in the bank being programmed output the Status Register content after the programming has started.

During Double Word Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored. Dual operations are not supported during Double Word Program operations and the command cannot be suspended. Typical Program times are given in [Table 15: Program/Erase times and endurance cycles](#).

Programming aborts if Reset goes to V_{IL} . As data integrity cannot be guaranteed when the program operation is aborted, the memory locations must be reprogrammed.

See [Appendix C, Figure 21: Double Word Program flowchart and pseudo code](#), for the flowchart for using the Double Word Program command.

6.3 Quadruple Word Program command

The Quadruple Word Program command improves the programming throughput by writing a page of four adjacent words in parallel. The four words must differ only for the addresses A0 and A1. If the block is protected, the Quadruple Word Program operation will abort, the data in the block will not be changed and the Status Register will output the error.

Five bus write cycles are necessary to issue the Quadruple Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written.
- The fourth bus cycle latches the Address and the Data of the third word to be written.
- The fifth bus cycle latches the Address and the Data of the fourth word to be written and starts the Program/Erase Controller.

Read operations to the bank being programmed output the Status Register content after the programming has started.

Programming aborts if Reset goes to V_{IL} . As data integrity cannot be guaranteed when the program operation is aborted, the memory locations must be reprogrammed.

During Quadruple Word Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored.

Dual operations are not supported during Quadruple Word Program operations and the command cannot be suspended. Typical Program times are given in [Table 15: Program/Erase times and endurance cycles](#).

See [Appendix C, Figure 22: Quadruple Word Program flowchart and pseudo code](#), for the flowchart for using the Quadruple Word Program command.

6.4 Enhanced Factory Program command

The Enhanced Factory Program command can be used to program large streams of data within any one block. It greatly reduces the total programming time when a large number of Words are written to a block at any one time.

Dual operations are not supported during the Enhanced Factory Program operation and the command cannot be suspended.

For optimum performance the Enhanced Factory Program commands should be limited to a maximum of 10 program/erase cycles per block. If this limit is exceeded the internal algorithm will continue to work properly but some degradation in performance is possible. Typical Program times are given in [Table 15](#). If the block is protected, the Enhanced Factory Program operation will abort, the data in the block will not be changed and the Status Register will output the error.

The Enhanced Factory Program command has four phases: the Setup Phase, the Program Phase to program the data to the memory, the Verify Phase to check that the data has been correctly programmed and reprogram if necessary and the Exit Phase. Refer to [Table 8: Factory Program commands](#), and [Figure 28: Enhanced Factory Program flowchart](#).

6.4.1 Setup Phase

The Enhanced Factory Program command requires two Bus Write operations to initiate the command.

- The first bus cycle sets up the Enhanced Factory Program command.
- The second bus cycle confirms the command.

The Status Register P/E.C. Bit SR7 should be read to check that the P/E.C. is ready. After the confirm command is issued, read operations output the Status Register data. The read Status Register command must not be issued as it will be interpreted as data to program.

6.4.2 Program Phase

The Program Phase requires $n+1$ cycles, where n is the number of Words (refer to [Table 8: Factory Program commands](#), and [Figure 28: Enhanced Factory Program flowchart](#)).

Three successive steps are required to issue and execute the Program Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word to be programmed. The Status Register Bank Write Status bit SR0 should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address can either remain the Start Address, in which case the P/E.C. increments the address location or the address can be incremented in which case the P/E.C. jumps to the new address. If any address that is not in the same block as the Start Address is given with data FFFFh, the Program Phase terminates and the Verify Phase begins. The Status Register bit SR0 should be read between each Bus Write cycle to check that the P/E.C. is ready for the next Word.
3. Finally, after all Words have been programmed, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the programming phase. If the data is not FFFFh, the command is ignored.

The memory is now set to enter the Verify Phase.

6.4.3 Verify Phase

The Verify Phase is similar to the Program Phase in that all Words must be resent to the memory for them to be checked against the programmed data. The Program/Erase Controller checks the stream of data with the data that was programmed in the Program Phase and reprograms the memory location if necessary.

Three successive steps are required to execute the Verify Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word, to be verified. The Status Register bit SR0 should be read to check that the Program/Erase Controller is ready for the next Word.
2. Each subsequent Word to be verified is latched with a new Bus Write operation. The Words must be written in the same order as in the Program Phase. The address can remain the Start Address or be incremented. If any address that is not in the same block as the Start Address is given with data FFFFh, the Verify Phase terminates. Status Register bit SR0 should be read to check that the P/E.C. is ready for the next Word.
3. Finally, after all Words have been verified, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the Verify Phase.

If the Verify Phase is successfully completed the memory remains in Read Status Register mode. If the Program/Erase Controller fails to reprogram a given location, the error will be signaled in the Status Register.

6.4.4 Exit Phase

Status Register P/E.C. bit SR7 set to '1' indicates that the device has returned to Read mode. A full Status Register check should be done to ensure that the block has been successfully programmed. See the section on the Status Register for more details.

6.5 Quadruple Enhanced Factory Program command

The Quadruple Enhanced Factory Program command can be used to program one or more pages of four adjacent words in parallel. The four words must differ only for the addresses A0 and A1.

Dual operations are not supported during Quadruple Enhanced Factory Program operations and the command cannot be suspended. If the block is protected, the Quadruple Enhanced Factory Program operation will abort, the data in the block will not be changed and the Status Register will output the error.

The Quadruple Enhanced Factory Program command has four phases: the Setup Phase, the Load Phase where the data is loaded into the buffer, the combined Program and Verify Phase where the loaded data is programmed to the memory and then automatically checked and reprogrammed if necessary and the Exit Phase. Unlike the Enhanced Factory Program it is not necessary to resubmit the data for the Verify Phase. The Load Phase and the Program and Verify Phase can be repeated to program any number of pages within the block.

6.5.1 Setup Phase

The Quadruple Enhanced Factory Program command requires one Bus Write operation to initiate the load phase. After the setup command is issued, read operations output the Status Register data. The Read Status Register command must not be issued as it will be interpreted as data to program.

6.5.2 Load Phase

The Load Phase requires 4 cycles to load the data (refer to [Table 8: Factory Program commands](#), and [Figure 29: Quadruple Enhanced Factory Program flowchart](#)). Once the first Word of each Page is written it is impossible to exit the Load phase until all four Words have been written.

Two successive steps are required to issue and execute the Load Phase of the Quadruple Enhanced Factory Program command.

1. Use one Bus Write operation to latch the Start Address and the first Word of the first Page to be programmed. For subsequent Pages the first Word address can remain the Start Address (in which case the next Page is programmed) or can be any address in the same block. If any address with data FFFFh is given that is not in the same block as the Start Address, the device enters the Exit Phase. For the first Load Phase Status Register bit SR7 should be read after the first Word has been issued to check that the command has been accepted (bit SR7 set to '0'). This check is not required for subsequent Load Phases.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address is only checked for the first Word of each Page as the order of the Words to be programmed is fixed.

The memory is now set to enter the Program and Verify Phase.

6.5.3 Program and Verify Phase

In the Program and Verify Phase the four Words that were loaded in the Load Phase are programmed in the memory array and then verified by the Program/Erase Controller. If any errors are found the Program/Erase Controller reprograms the location. During this phase the Status Register shows that the Program/Erase Controller is busy, Status Register bit SR7 set to '0', and that the device is not waiting for new data, Status Register bit SR0 set to '1'. When Status Register bit SR0 is set to '0' the Program and Verify phase has terminated.

Once the Verify Phase has successfully completed subsequent pages in the same block can be loaded and programmed. The device returns to the beginning of the Load Phase by issuing one Bus Write operation to latch the Address and the first of the four new Words to be programmed.

6.5.4 Exit Phase

Finally, after all the pages have been programmed, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the Load and Program and Verify Phases.

Status Register bit SR7 set to '1' and bit SR0 set to '0' indicate that the Quadruple Enhanced Factory Program command has terminated. A full Status Register check should be done to ensure that the block has been successfully programmed. See the section on the Status Register for more details.

If the Program and Verify Phase has successfully completed the memory returns to Read mode. If the P/E.C. fails to program and reprogram a given location, the error will be signaled in the Status Register.

Table 8. Factory Program commands⁽¹⁾

Command	Phase	Cycles	Bus Write Operations											
			1st		2nd		3rd		Final -1		Final			
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data		
Bank Erase		2	BKA	80h	BKA	D0h								
Double Word Program ⁽²⁾		3	BKA or WA1 ⁽³⁾	35h	WA1	PD1	WA2	PD2						
Quadruple Word Program ⁽⁴⁾		5	BKA or WA1 ⁽³⁾	56h	WA1	PD1	WA2	PD2	WA3	PD3	WA4	PD4		
Enhanced Factory Program ⁽⁵⁾	Setup, Program	2+ n+1	BKA or WA1 ⁽³⁾	30h	BA or WA1 ⁽⁶⁾	D0h	WA1 ⁽⁷⁾	PD1	WAn ⁽⁸⁾	PAn	NOT WA1 ⁽⁷⁾	FFFFh		
	Verify, Exit	n+1	WA1 ⁽⁷⁾	PD1	WA2 ⁽⁸⁾	PD2	WA3 ⁽⁸⁾	PD3	WAn ⁽⁸⁾	PAn	NOT WA1 ⁽⁷⁾	FFFFh		
Quadruple Enhanced Factory Program ⁽⁴⁾⁽⁵⁾	Setup, first Load	5	BKA or WA1 ⁽³⁾	75h	WA1 ⁽⁷⁾	PD1	WA2 ⁽⁹⁾	PD2	WA3 ⁽⁹⁾	PD3	WA4 ⁽⁹⁾	PD4		
	First Program & Verify		Automatic											
	Subsequent Loads	4	WA1i ⁽⁷⁾	PD1i	WA2i ⁽⁹⁾	PD2i	WA3i ⁽⁹⁾	PD3i			WA4i ⁽⁹⁾	PD4i		
	Subsequent Program & Verify		Automatic											
	Exit	1	NOT WA1 ⁽⁷⁾	FFFFh										

1. WA=Word Address in targeted bank, BKA= Bank Address, PD=Program Data, BA=Block Address.
2. Word Addresses 1 and 2 must be consecutive Addresses differing only for A0.
3. Any address within the bank can be used.
4. Word Addresses 1,2,3 and 4 must be consecutive Addresses differing only for A0 and A1.
5. A Bus Read must be done between each Write cycle where the data is programmed or verified to read the Status Register and check that the memory is ready to accept the next data. n = number of Words, i = number of Pages to be programmed.
6. Any address within the block can be used.
7. WA1 is the Start Address. NOT WA1 is any address that is not in the same block as WA1.
8. Address can remain Starting Address WA1 or be incremented.
9. Address is only checked for the first Word of each Page as the order to program the Words in each page is fixed so subsequent Words in each Page can be written to any address.

7 Status Register

The Status Register provides information on the current or previous Program or Erase operations. Issue a Read Status Register command to read the contents of the Status Register, refer to Read Status Register Command section for more details. To output the contents, the Status Register is latched and updated on the falling edge of the Chip Enable or Output Enable signals and can be read until Chip Enable or Output Enable returns to V_{IH} . The Status Register can only be read using single asynchronous or single synchronous reads. Bus Read operations from any address within the bank, always read the Status Register during Program and Erase operations.

The various bits convey information about the status and any errors of the operation. Bits SR7, SR6, SR2 and SR0 give information on the status of the device and are set and reset by the device. Bits SR5, SR4, SR3 and SR1 give information on errors, they are set by the device but must be reset by issuing a Clear Status Register command or a hardware reset. If an error bit is set to '1' the Status Register should be reset before issuing another command. SR7 to SR1 refer to the status of the device while SR0 refers to the status of the addressed bank.

The bits in the Status Register are summarized in [Table 9: Status Register bits](#). Refer to [Table 9](#) in conjunction with the following text descriptions.

7.0.1 Program/Erase Controller Status Bit (SR7)

The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive in any bank. When the Program/Erase Controller Status bit is Low (set to '0'), the Program/Erase Controller is active; when the bit is High (set to '1'), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, operations the Program/Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Lock Status bits should be tested for errors.

7.0.2 Erase Suspend Status Bit (SR6)

The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended in the addressed block. When the Erase Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). SR7 is set within the Erase Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

7.0.3 Erase Status Bit (SR5)

The Erase Status bit can be used to identify if the memory has failed to verify that the block or bank has erased correctly. When the Erase Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the block or bank and still failed to verify that it has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

7.0.4 Program Status Bit (SR4)

The Program Status bit is used to identify a Program failure or an attempt to program a '1' to an already programmed bit when $V_{PP} = V_{PPH}$.

When the Program Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly.

After an attempt to program a '1' to an already programmed bit, the Program Status bit SR4 only goes High (set to '1') if $V_{PP} = V_{PPH}$ (if V_{PP} is different from V_{PPH} , SR4 remains Low (set to '0') and the attempt is not shown).

The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

7.0.5 V_{PP} Status Bit (SR3)

The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to '0'), the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High (set to '1'), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK} , the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

7.0.6 Program Suspend Status Bit (SR2)

The Program Suspend Status bit indicates that a Program operation has been suspended in the addressed block. When the Program Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). SR2 is set within the Program Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

7.0.7 Block Protection Status Bit (SR1)

The Block Protection Status bit can be used to identify if a Program or Block Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to '1'), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

7.0.8 Bank Write/Multiple Word Program Status Bit (SR0)

The Bank Write Status bit indicates whether the addressed bank is programming or erasing. In Enhanced Factory Program mode the Multiple Word Program bit shows if a Word has finished programming or verifying depending on the phase. The Bank Write Status bit should only be considered valid when the Program/Erase Controller Status SR7 is Low (set to '0').

When both the Program/Erase Controller Status bit and the Bank Write Status bit are Low (set to '0'), the addressed bank is executing a Program or Erase operation. When the Program/Erase Controller Status bit is Low (set to '0') and the Bank Write Status bit is High (set to '1'), a Program or Erase operation is being executed in a bank other than the one being addressed.

In Enhanced Factory Program mode if Multiple Word Program Status bit is Low (set to '0'), the device is ready for the next Word, if the Multiple Word Program Status bit is High (set to '1') the device is not ready for the next Word.

Note: Refer to [Appendix C: Flowcharts and pseudo codes](#), for using the Status Register.

Table 9. Status Register bits

Bit	Name	Type	Logic Level ⁽¹⁾	Definition	
SR7	P/E.C. Status	Status	'1'	Ready	
			'0'	Busy	
SR6	Erase Suspend Status	Status	'1'	Erase Suspended	
			'0'	Erase In progress or Completed	
SR5	Erase Status	Error	'1'	Erase Error	
			'0'	Erase Success	
SR4	Program Status	Error	'1'	Program Error	
			'0'	Program Success	
SR3	V _{PP} Status	Error	'1'	V _{PP} Invalid, Abort	
			'0'	V _{PP} OK	
SR2	Program Suspend Status	Status	'1'	Program Suspended	
			'0'	Program In Progress or Completed	
SR1	Block Protection Status	Error	'1'	Program/Erase on protected Block, Abort	
			'0'	No operation to protected blocks	
SR0	Bank Write Status	Status	'1'	SR7 = '1'	Not Allowed
				SR7 = '0'	Program or erase operation in a bank other than the addressed bank
			'0'	SR7 = '1'	No Program or erase operation in the device
				SR7 = '0'	Program or erase operation in addressed bank
	Multiple Word Program Status (Enhanced Factory Program mode)	Status	'1'	SR7 = '1'	Not Allowed
				SR7 = '0'	the device is NOT ready for the next word
			'0'	SR7 = '1'	the device is exiting from EFP
				SR7 = '0'	the device is ready for the next Word

1. Logic level '1' is High, '0' is Low.

8 Configuration Register

The Configuration Register is used to configure the type of bus access that the memory will perform. Refer to Read Modes section for details on read operations.

The Configuration Register is set through the Command Interface. After a Reset or Power-Up the device is configured for asynchronous page read (CR15 = 1). The Configuration Register bits are described in [Table 10](#). They specify the selection of the burst length, burst type, burst X latency and the Read operation. Refer to [Figures 6 and 7](#) for examples of synchronous burst configurations.

8.1 Read Select Bit (CR15)

The Read Select bit, CR15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', read operations are asynchronous; when the Read Select bit is set to '0', read operations are synchronous. Synchronous Burst Read is supported in both parameter and main blocks and can be performed across banks.

On reset or power-up the Read Select bit is set to '1' for asynchronous access.

8.2 X-Latency Bits (CR13-CR11)

The X-Latency bits are used during Synchronous Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in [Table 10: Configuration Register bits](#).

The correspondence between X-Latency settings and the maximum sustainable frequency must be calculated taking into account some system parameters. Two conditions must be satisfied:

1. Depending on whether t_{AVK_CPU} or t_{DELAY} is supplied either one of the following two equations must be satisfied:

$$(n + 1) t_K \geq t_{ACC} - t_{AVK_CPU} + t_{QVK_CPU}$$

$$(n + 2) t_K \geq t_{ACC} + t_{DELAY} + t_{QVK_CPU}$$

2. and also

$$t_K > t_{KQV} + t_{QVK_CPU}$$

where:

- n is the chosen X-Latency configuration code
- t_K is the clock period
- t_{AVK_CPU} is clock to address valid, \bar{L} Low, or \bar{E} Low, whichever occurs last
- t_{DELAY} is address valid, \bar{L} Low, or \bar{E} Low to clock, whichever occurs last
- t_{QVK_CPU} is the data setup time required by the system CPU,
- t_{KQV} is the clock to data valid time
- t_{ACC} is the random access time of the device.

Refer to [Figure 6: X-Latency and data output configuration example](#).

8.3 Wait Polarity Bit (CR10)

In synchronous burst mode the Wait signal indicates whether the output data are valid or a WAIT state must be inserted. The Wait Polarity bit is used to set the polarity of the Wait signal. When the Wait Polarity bit is set to '0' the Wait signal is active Low. When the Wait Polarity bit is set to '1' the Wait signal is active High (default).

8.4 Data Output Configuration Bit (CR9)

The Data Output Configuration bit determines whether the output remains valid for one or two clock cycles. When the Data Output Configuration Bit is '0' the output data is valid for one clock cycle, when the Data Output Configuration Bit is '1' the output data is valid for two clock cycles.

The Data Output Configuration depends on the condition:

- $t_K > t_{KQV} + t_{QVK_CPU}$

where t_K is the clock period, t_{QVK_CPU} is the data setup time required by the system CPU and t_{KQV} is the clock to data valid time. If this condition is not satisfied, the Data Output Configuration bit should be set to '1' (two clock cycles). Refer to [Figure 6: X-Latency and data output configuration example](#).

8.5 Wait Configuration Bit (CR8)

In burst mode the Wait bit controls the timing of the Wait output pin, WAIT. When WAIT is asserted, Data is Not Valid and when WAIT is deasserted, Data is Valid. When the Wait bit is '0' the Wait output pin is asserted during the wait state. When the Wait bit is '1' (default) the Wait output pin is asserted one clock cycle before the wait state.

8.6 Burst Type Bit (CR7)

The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' (default) the memory outputs from sequential addresses. See [Table 11: Burst type definition](#), for the sequence of addresses output from a given starting address in each mode.

8.7 Valid Clock Edge Bit (CR6)

The Valid Clock Edge bit, CR6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

8.8 Wrap Burst Bit (CR3)

The burst reads can be confined inside the 4 or 8 Word boundary (wrap) or overcome the boundary (no wrap). The Wrap Burst bit is used to select between wrap and no wrap. When

the Wrap Burst bit is set to '0' the burst read wraps; when it is set to '1' the burst read does not wrap.

8.9 Burst length Bits (CR2-CR0)

The Burst Length bits set the number of Words to be output during a Synchronous Burst Read operation as result of a single address latch cycle. They can be set for 4 Words, 8 Words, 16 Words or continuous burst, where all the words are read sequentially.

In continuous burst mode the burst sequence can cross bank boundaries.

In continuous burst mode or in 4, 8, 16 Words no-wrap, depending on the starting address, the device asserts the WAIT output to indicate that a delay is necessary before the data is output.

If the starting address is aligned to a 4 Word boundary no wait states are needed and the WAIT output is not asserted.

If the starting address is shifted by 1,2 or 3 positions from the four word boundary, WAIT will be asserted for 1, 2 or 3 clock cycles when the burst sequence crosses the first 16 Word boundary, to indicate that the device needs an internal delay to read the successive words in the array. WAIT will be asserted only once during a continuous burst access. See also [Table 11: Burst type definition](#).

CR14, CR5 and **CR4** are reserved for future use.

Table 10. Configuration Register bits

Bit	Description	Value	Description
CR15	Read Select	0	Synchronous Read
		1	Asynchronous Read (Default at power-on)
CR14	Reserved		
CR13-CR11	X-Latency	010	2 clock latency
		011	3 clock latency
		100	4 clock latency
		101	5 clock latency
		111	Reserved (default)
		Other configurations reserved	
CR10	Wait Polarity	0	WAIT is active Low
		1	WAIT is active high (default)
CR9	Data Output Configuration	0	Data held for one clock cycle
		1	Data held for two clock cycles (default)
CR8	Wait Configuration	0	WAIT is active during wait state
		1	WAIT is active one data cycle before wait state (default)
CR7	Burst Type	0	Interleaved
		1	Sequential (default)
CR6	Valid Clock Edge	0	Falling Clock edge
		1	Rising Clock edge (default)
CR5-CR4	Reserved		
CR3	Wrap Burst	0	Wrap
		1	No Wrap (default)
CR2-CR0	Burst Length	001	4 Words
		010	8 Words
		011	16 Words
		111	Continuous (CR7 must be set to '1') (default)

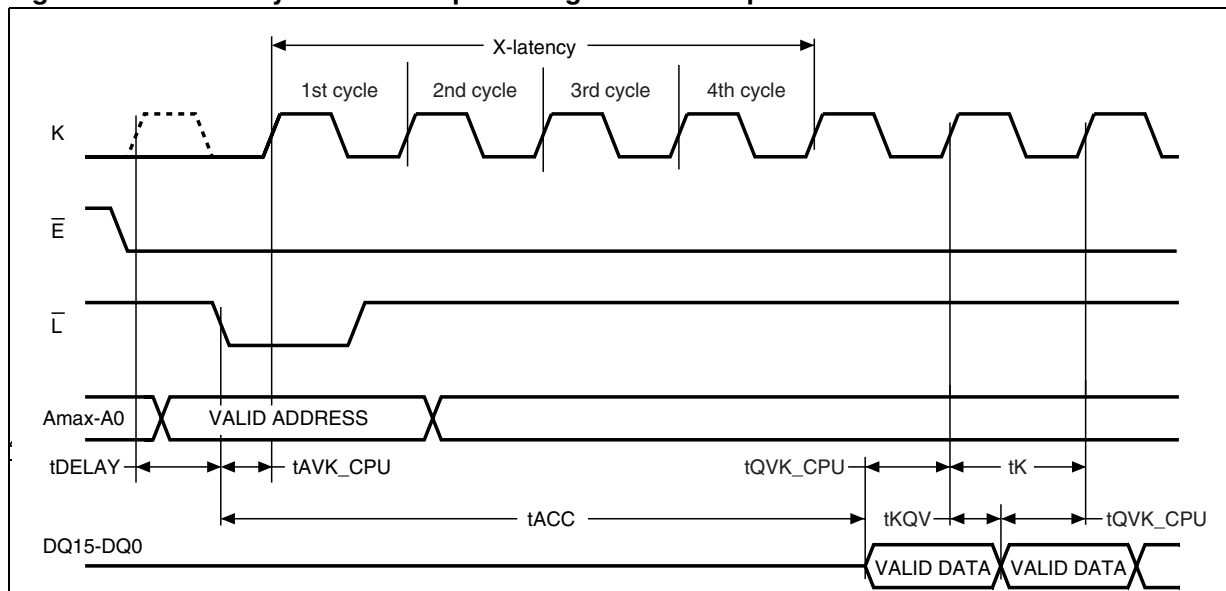
Table 11. Burst type definition

Mode	Start Add	4 Words		8 Words		16 Words		Continuous Burst
		Sequential	Interleaved	Sequential	Interleaved	Sequential	Interleaved	
Wrap	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6...
	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14	1-2-3-4-5-6-7-...15-WAIT-16-17-18...
	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13	2-3-4-5-6-7...15-WAIT-WAIT-16-17-18...
	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12	3-4-5-6-7...15-WAIT-WAIT-WAIT-16-17-18...
	...							
	7	7-4-5-6	7-6-5-4	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8	7-8-9-10-11-12-13-14-15-WAIT-WAIT-WAIT-16-17...
	...							
	12							12-13-14-15-16-17-18...
	13							13-14-15-WAIT-16-17-18...
	14							14-15-WAIT-WAIT-16-17-18....
15							15-WAIT-WAIT-WAIT-16-17-18...	

Table 11. Burst type definition (continued)

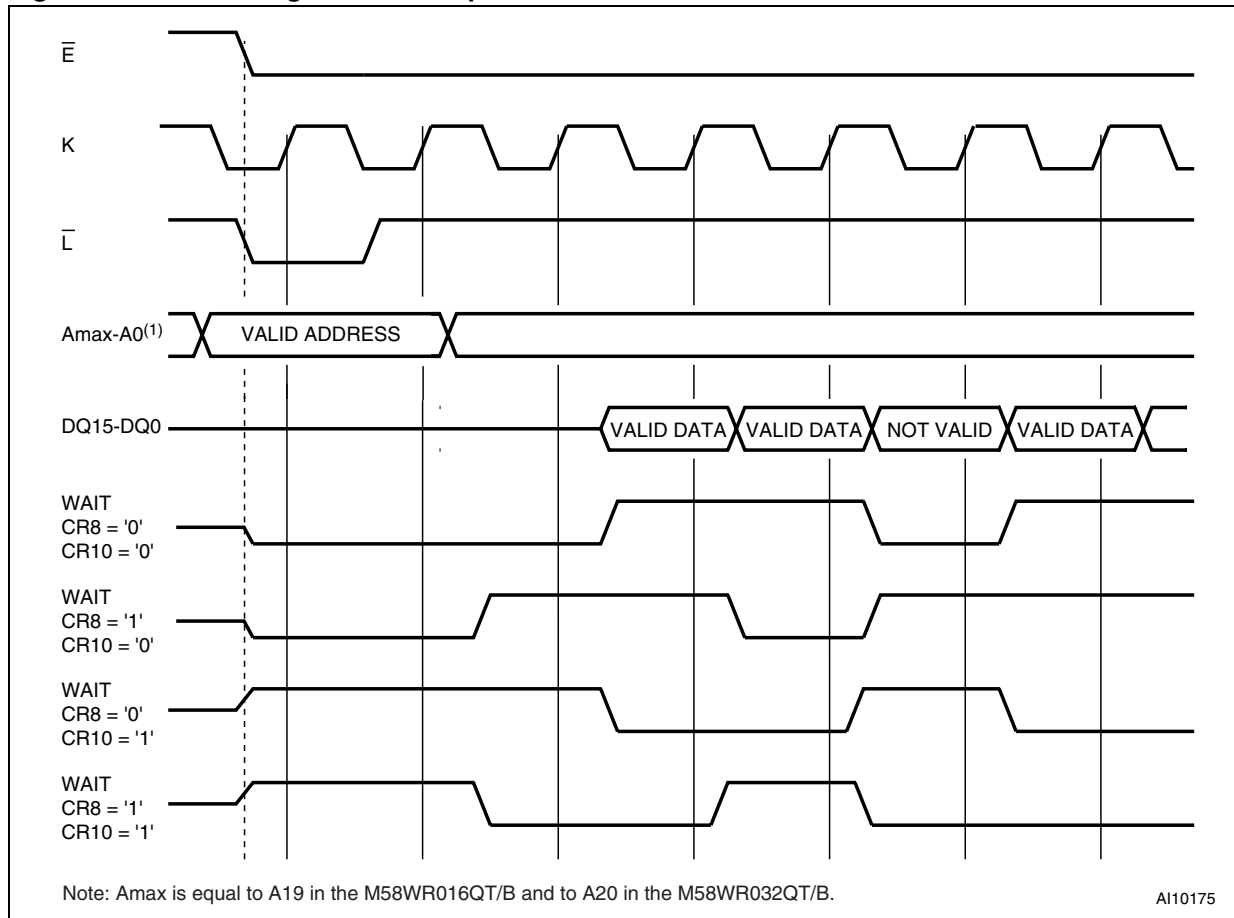
Mode	Start Add	4 Words		8 Words		16 Words		Continuous Burst
		Sequential	Interleaved	Sequential	Interleaved	Sequential	Interleaved	
No-wrap	0	0-1-2-3		0-1-2-3-4-5-6-7		0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15		Same as for Wrap (Wrap /No Wrap has no effect on Continuous Burst)
	1	1-2-3-4		1-2-3-4-5-6-7-8		1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-WAIT-16		
	2	2-3-4-5		2-3-4-5-6-7-8-9...		2-3-4-5-6-7-8-9-10-11-12-13-14-15-WAIT-WAIT-16-17		
	3	3-4-5-6		3-4-5-6-7-8-9-10		3-4-5-6-7-8-9-10-11-12-13-14-15-WAIT-WAIT-WAIT-16-17-18		
	...							
	7	7-8-9-10		7-8-9-10-11-12-13-14		7-8-9-10-11-12-13-14-15-WAIT-WAIT-WAIT-16-17-18-19-20-21-22		
	...							
	12	12-13-14-15		12-13-14-15-16-17-18-19		12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27		
	13	13-14-15-WAIT-16		13-14-15-WAIT-16-17-18-19-20		13-14-15-WAIT-16-17-18-19-20-21-22-23-24-25-26-27-28		
	14	14-15-WAIT-WAIT-16-17		14-15-WAIT-WAIT-16-17-18-19-20-21		14-15-WAIT-WAIT-16-17-18-19-20-21-22-23-24-25-26-27-28-29		
15	15-WAIT-WAIT-WAIT-16-17-18		15-WAIT-WAIT-WAIT-16-17-18-19-20-21-22		15-WAIT-WAIT-WAIT-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30			

Figure 6. X-Latency and data output configuration example



Notes: 1. Settings shown: X-latency = 4, Data Output held for one clock cycle.
 2. Amax is equal to A19 in the M58WR016QT/B and to A20 in the M58WR032QT/B.

Figure 7. Wait configuration example



9 Read modes

Read operations can be performed in two different ways depending on the settings in the Configuration Register. If the clock signal is 'don't care' for the data output, the read operation is Asynchronous; if the data output is synchronized with clock, the read operation is Synchronous.

The Read mode and data output format are determined by the Configuration Register. (See Configuration Register section for details). All banks supports both asynchronous and synchronous read operations. The Multiple Bank architecture allows read operations in one bank, while write operations are being executed in another (see Tables 12 and 13).

9.1 Asynchronous Read mode

In Asynchronous Read operations the clock signal is 'don't care'. The device outputs the data corresponding to the address latched, that is the memory array, Status Register, Common Flash Interface or Electronic Signature depending on the command issued. CR15 in the Configuration Register must be set to '1' for Asynchronous operations.

In Asynchronous Read mode a Page of data is internally read and stored in a Page Buffer. The Page has a size of 4 Words and is addressed by A0 and A1 address inputs. The address inputs A0 and A1 are not gated by Latch Enable in Asynchronous Read mode.

The first read operation within the Page has a longer access time (T_{acc} , Random access time), subsequent reads within the same Page have much shorter access times. If the Page changes then the normal, longer timings apply again.

Asynchronous Read operations can be performed in two different ways, Asynchronous Random Access Read and Asynchronous Page Read. Only Asynchronous Page Read takes full advantage of the internal page storage so different timings are applied.

During Asynchronous Read operations, after a bus inactivity of 150ns, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value and the outputs are still driven.

In Asynchronous Read mode, the WAIT signal is always asserted.

See [Table 21: Asynchronous Read AC characteristics](#), [Figure 10: Asynchronous Random Access Read AC waveforms](#), and [Figure 11: Asynchronous Page Read AC waveforms](#) for details.

9.2 Synchronous Burst Read mode

In Synchronous Burst Read mode the data is output in bursts synchronized with the clock. It is possible to perform burst reads across bank boundaries.

Synchronous Burst Read mode can only be used to read the memory array. For other read operations, such as Read Status Register, Read CFI and Read Electronic Signature, Single Synchronous Read or Asynchronous Random Access Read must be used.

In Synchronous Burst Read mode the flow of the data output depends on parameters that are configured in the Configuration Register.

A burst sequence is started at the first clock edge (rising or falling depending on Valid Clock Edge bit CR6 in the Configuration Register) after the falling edge of Latch Enable or Chip Enable, whichever occurs last. Addresses are internally incremented and after a delay of 2 to 5 clock cycles (X latency bits CR13-CR11) the corresponding data are output on each clock cycle.

The number of Words to be output during a Synchronous Burst Read operation can be configured as 4, 8, 16 Words, or Continuous (Burst Length bits CR2-CR0). The data can be configured to remain valid for one or two clock cycles (Data Output Configuration bit CR9).

The order of the data output can be modified through the Burst Type and the Wrap Burst bits in the Configuration Register. The burst sequence may be configured to be sequential or interleaved (CR7). The burst reads can be confined inside the 4, 8 or 16 Word boundary (Wrap) or overcome the boundary (No Wrap). If the starting address is aligned to the Burst Length (4, 8 or 16 Words) the wrapped configuration has no impact on the output sequence. Interleaved mode is not allowed in Continuous Burst Read mode or with No Wrap sequences.

A WAIT signal may be asserted to indicate to the system that an output delay will occur. This delay will depend on the starting address of the burst sequence; the worst case delay will occur when the sequence is crossing a 16 Word boundary and the starting address was at the end of a four word boundary.

WAIT is asserted during X latency, the Wait state and at the end of 4-, 8- or 16-Word burst. It is only deasserted when output data are valid. In Continuous Burst Read mode a Wait state will occur when crossing the first 16 Word boundary. If the burst starting address is aligned to a 4 Word Page, the Wait state will not occur.

The WAIT signal can be configured to be active Low or active High (default) by setting CR10 in the Configuration Register. The WAIT signal is meaningful only in Synchronous Burst Read mode, in other modes, WAIT is always asserted (except for Read Array mode).

See [Table 22: Synchronous Read AC characteristics](#), and [Figure 12: Synchronous Burst Read AC waveforms](#), for details.

9.2.1 Synchronous Burst Read Suspend

A Synchronous Burst Read operation can be suspended, freeing the data bus for other higher priority devices. It can be suspended during the initial access latency time (before data is output) in which case the initial latency time can be reduced to zero, or after the device has output data. When the Synchronous Burst Read operation is suspended, internal array sensing continues and any previously latched internal data is retained. A burst sequence can be suspended and resumed as often as required as long as the operating conditions of the device are met.

A Synchronous Burst Read operation is suspended when \bar{E} is low and the current address has been latched (on a Latch Enable rising edge or on a valid clock edge). The clock signal is then halted at V_{IH} or at V_{IL} , and \bar{G} goes high.

When \bar{G} becomes low again and the clock signal restarts, the Synchronous Burst Read operation is resumed exactly where it stopped.

WAIT being gated by \bar{E} remains active and will not revert to high-impedance when \bar{G} goes high. So if two or more devices are connected to the system's READY signal, to prevent bus contention the WAIT signal of the Flash memory should not be directly connected to the system's READY signal.

See [Table 22: Synchronous Read AC characteristics](#) and [Figure 14: Synchronous Burst Read Suspend AC waveforms](#), for details.

9.3 Single Synchronous Read mode

Single Synchronous Read operations are similar to Synchronous Burst Read operations except that only the first data output after the X latency is valid. Synchronous Single Reads are used to read the Electronic Signature, Status Register, CFI, Block Protection Status, Configuration Register Status or Protection Register. When the addressed bank is in Read CFI, Read Status Register or Read Electronic Signature mode, the WAIT signal is always asserted.

See [Table 22: Synchronous Read AC characteristics](#) and [Figure 13: Single Synchronous Read AC waveforms](#), for details.

10 Dual operations and Multiple Bank architecture

The Multiple Bank Architecture of the M58WRxxxQT/B provides flexibility for software developers by allowing code and data to be split with 4Mbit granularity. The Dual Operations feature simplifies the software management of the device and allows code to be executed from one bank while another bank is being programmed or erased.

The Dual operations feature means that while programming or erasing in one bank, Read operations are possible in another bank with zero latency (only one bank at a time is allowed to be in Program or Erase mode). If a Read operation is required in a bank which is programming or erasing, the Program or Erase operation can be suspended. Also if the suspended operation was Erase then a Program command can be issued to another block, so the device can have one block in Erase Suspend mode, one programming and other banks in Read mode. Bus Read operations are allowed in another bank between setup and confirm cycles of program or erase operations. The combination of these features means that read operations are possible at any moment.

Tables 12 and 13 show the dual operations possible in other banks and in the same bank. For a complete list of possible commands refer to [Appendix D: Command interface state tables](#).

Table 12. Dual operations allowed in other banks

Status of bank	Commands allowed in another bank							
	Read Array	Read Status Register	Read CFI Query	Read Electronic Signature	Program	Block Erase	Program/ Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programming	Yes	Yes	Yes	Yes	–	–	Yes	–
Erasing	Yes	Yes	Yes	Yes	–	–	Yes	–
Program Suspended	Yes	Yes	Yes	Yes	–	–	–	Yes
Erase Suspended	Yes	Yes	Yes	Yes	Yes	–	–	Yes

Table 13. Dual operations allowed in same bank

Status of bank	Commands allowed in same bank							
	Read Array	Read Status Register	Read CFI Query	Read Electronic Signature	Program	Block Erase	Program/ Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programming	_(1)	Yes	Yes	Yes	-	-	Yes	-
Erasing	_(1)	Yes	Yes	Yes	-	-	Yes	-
Program Suspended	Yes(2)	Yes	Yes	Yes	-	-	-	Yes
Erase Suspended	Yes(2)	Yes	Yes	Yes	Yes(2)	-	-	Yes

1. The Read Array command is accepted but the data output is not guaranteed until the Program or Erase has completed.
2. Not allowed in the Block or Word that is being erased or programmed.

11 Block locking

The M58WRxxxQT/B features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has three levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.
- $V_{PP} \leq V_{PPLK}$ - the third level offers a complete hardware protection against program and erase on all blocks.

The protection status of each block can be set to Locked, Unlocked, and Lock-Down. [Table 14](#), defines all of the possible protection states (\overline{WP} , DQ1, DQ0), and [Appendix C](#), [Figure 26](#), shows a flowchart for the locking operations.

11.1 Reading a Block's lock status

The lock status of every block can be read in the Read Electronic Signature mode of the device. To enter this mode write 90h to the device. Subsequent reads at the address specified in [Table 7](#), will output the protection status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the locking system.

11.2 Locked state

The default status of all blocks on power-up or after a hardware reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will return an error in the Status Register. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

11.3 Unlocked state

Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state after a hardware reset or when the device is powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

11.4 Lock-Down state

Blocks that are Locked-Down (state (0,1,x)) are protected from program and erase operations (as for Locked blocks) but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the \overline{WP} input pin. When $\overline{WP}=0$ (V_{IL}), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WP}=1$ (V_{IH}) the Lock-Down function is disabled (1,1,x) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-locked (1,1,1) and unlocked (1,1,0) as desired while \overline{WP} remains high. When \overline{WP} is Low, blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while \overline{WP} was high. Device reset or power-down resets all blocks, including those in Lock-Down, to the Locked state.

11.5 Locking operations during Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete. Locking operations cannot be performed during a program suspend. Refer to [Appendix D: Command interface state tables](#), for detailed information on which commands are valid during erase suspend.

Table 14. Lock status

Current Protection Status ⁽¹⁾ (\overline{WP} , DQ1, DQ0)		Next Protection Status ⁽¹⁾ (\overline{WP} , DQ1, DQ0)			
Current State	Program/Erase Allowed	After Block Lock Command	After Block Unlock Command	After Block Lock-Down Command	After \overline{WP} transition
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1 ⁽²⁾	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1 ⁽²⁾	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 ⁽³⁾

1. The lock status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a locked block) as read in the Read Electronic Signature command with A1 = V_{IH} and A0 = V_{IL}.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to \overline{WP} status.
3. A \overline{WP} transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

12 Program and erase times and endurance cycles

The Program and Erase times and the number of Program/ Erase cycles per block are shown in [Table 15](#). Exact erase times may change depending on the memory array condition. The best case is when all the bits in the block or bank are at '0' (preprogrammed). The worst case is when all the bits in the block or bank are at '1' (not preprogrammed). Usually, the system overhead is negligible with respect to the erase time.

In the M58WRxxxQT/B the maximum number of Program/ Erase cycles depends on the V_{PP} voltage supply used.

Table 15. Program/Erase times and endurance cycles⁽¹⁾

Parameter		Condition	Min	Typ	Typical after 100k W/E Cycles	Max	Unit	
$V_{PP} = V_{DD}$	Erase	Parameter Block (4 KWord) ⁽²⁾		0.3	1	2.5	s	
		Main Block (32 KWord)	Preprogrammed		0.8	3	4	s
			Not Preprogrammed		1.1		4	s
		Bank (4Mbit)	Preprogrammed		3			s
			Not Preprogrammed		4.5			s
	Program ⁽³⁾	Word			10	10	100	μ s
		Parameter Block (4 KWord)			32			ms
		Main Block (32 KWord)			256			ms
	Suspend Latency	Program			5		10	μ s
		Erase			5		20	μ s
	Program/Erase Cycles (per Block)	Main Blocks		100,000				cycles
		Parameter Blocks		100,000				cycles

Table 15. Program/Erase times and endurance cycles⁽¹⁾ (continued)

Parameter		Condition	Min	Typ	Typical after 100k W/E Cycles	Max	Unit	
V_{PP} = V_{PPH}	Erase	Parameter Block (4 KWord)			0.25		2.5 s	
		Main Block (32 KWord)			0.8		4 s	
		Bank (4Mbit)			3.5		s	
	Program ⁽³⁾	Word/ Double Word/ Quadruple Word ⁽⁴⁾			8		100 μs	
		Parameter Block (4 KWord)	Quad-Enhanced Factory		10		ms	
			Enhanced Factory		25		ms	
			Quadruple Word ⁽⁴⁾		8		ms	
			Word		32		ms	
		Main Block (32 KWord)	Quad-Enhanced Factory		80		ms	
			Enhanced Factory		200		ms	
			Quadruple Word ⁽⁴⁾		64		ms	
			Word		256		ms	
		Bank (4Mbit)	Quad-Enhanced Factory ⁽⁴⁾		520		s	
	Quadruple Word ⁽⁴⁾			510		ms		
	Program/Erase Cycles (per Block)	Main Blocks					1000	cycles
		Parameter Blocks					2500	cycles

1. T_A = -40 to 85°C; V_{DD} = 1.7V to 2.2V; V_{DDQ} = 2.2V to 3.3V.
2. The difference between Preprogrammed and not preprogrammed is not significant (<30ms).
3. Values are liable to change with the external system-level overhead (command sequence and Status Register polling execution).
4. Measurements performed at 25°C. T_A = 25°C ±5°C for Quadruple Word, Double Word and Quadruple Enhanced Factory Program.

13 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 16. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	-40	85	°C
T_{BIAS}	Temperature Under Bias	-40	125	°C
T_{STG}	Storage Temperature	-65	155	°C
V_{IO}	Input or Output Voltage	-0.5	$V_{DDQ}+0.6$	V
V_{DD}	Supply Voltage	-0.2	2.45	V
V_{DDQ}	Input/Output Supply Voltage	-0.2	2.45	V
V_{PP}	Program Voltage	-0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

14 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in [Table 17: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 17. Operating and AC measurement conditions

Parameter	M58WRxxxQT/B						Unit
	60		70		80		
	Min	Max	Min	Max	Min	Max	
V _{DD} Supply Voltage	1.7	2	1.7	2	1.7	2	V
V _{DDQ} Supply Voltage	1.7	2.24	1.7	2.24	1.7	2.24	V
V _{PP} Supply Voltage (Factory environment)	11.4	12.6	11.4	12.6	11.4	12.6	V
V _{PP} Supply Voltage (Application environment)	-0.4	V _{DDQ} +0.4	-0.4	V _{DDQ} +0.4	-0.4	V _{DDQ} +0.4	V
Ambient Operating Temperature	-40	85	-40	85	-40	85	°C
Load Capacitance (C _L)	30		30		30		pF
Input Rise and Fall Times		5		5		5	ns
Input Pulse Voltages	0 to V _{DDQ}		0 to V _{DDQ}		0 to V _{DDQ}		V
Input and Output Timing Ref. Voltages	V _{DDQ} /2		V _{DDQ} /2		V _{DDQ} /2		V

Figure 8. AC measurement I/O waveform

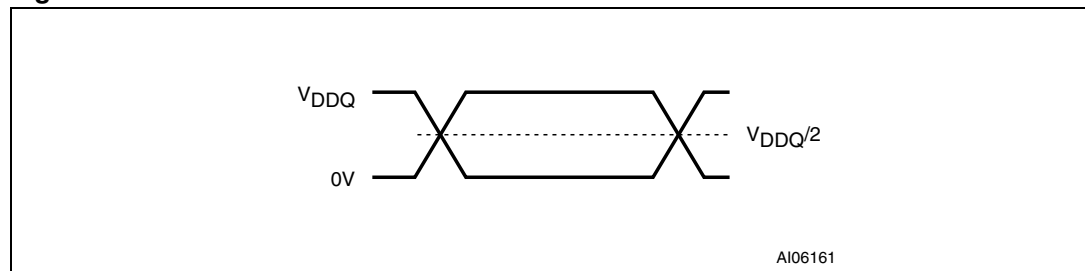


Figure 9. AC measurement load circuit

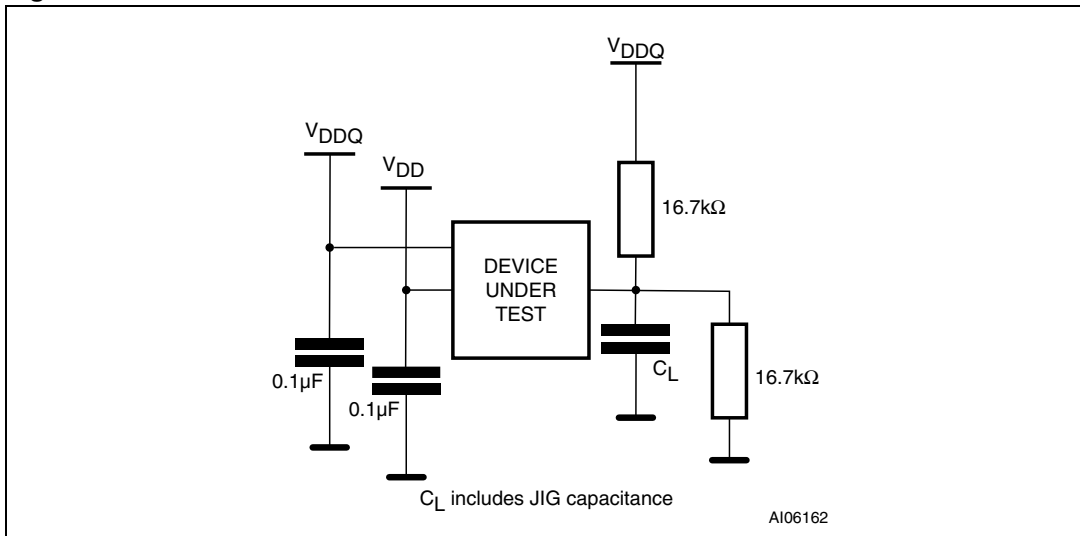


Table 18. Capacitance⁽¹⁾

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

1. Sampled only, not 100% tested.

Table 19. DC characteristics - currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{DDQ}$			± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{DDQ}$			± 1	μA
I_{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\bar{E} = V_{IL}, \bar{G} = V_{IH}$		3	6	mA
		4 Word		7	16	mA
	Supply Current Synchronous Read (f=54MHz)	8 Word		10	18	mA
		16 Word		12	22	mA
		Continuous		13	25	mA
	Supply Current Synchronous Read (f=66MHz)	4 Word		8	17	mA
		8 Word		11	20	mA
		16 Word		14	25	mA
Continuous			16	30	mA	
I_{DD2}	Supply Current (Reset)	$\bar{RP} = V_{SS} \pm 0.2V$		10	50	μA
I_{DD3}	Supply Current (Standby)	$\bar{E} = V_{DDQ} \pm 0.2V$ $K = V_{SS}$		10	50	μA
I_{DD4}	Supply Current (Automatic Standby)	$\bar{E} = V_{IL}, \bar{G} = V_{IH}$		10	50	μA
$I_{DD5}^{(1)}$	Supply Current (Program)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
	Supply Current (Erase)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
$I_{DD6}^{(1)(2)}$	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		13	26	mA
		Program/Erase in one Bank, Synchronous Read in another Bank		23	45	mA
$I_{DD7}^{(1)}$	Supply Current Program/Erase Suspended (Standby)	$\bar{E} = V_{DDQ} \pm 0.2V$ $K = V_{SS}$		10	50	μA
$I_{PP1}^{(1)}$	V_{PP} Supply Current (Program)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	μA
	V_{PP} Supply Current (Erase)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	μA
I_{PP2}	V_{PP} Supply Current (Read)	$V_{PP} \leq V_{DD}$		0.2	5	μA
$I_{PP3}^{(1)}$	V_{PP} Supply Current (Standby)	$V_{PP} \leq V_{DD}$		0.2	5	μA

1. Sampled only, not 100% tested.

2. V_{DD} Dual Operation current is the sum of read and program or erase currents.

Table 20. DC characteristics - voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		-0.5		0.4	V
V_{IH}	Input High Voltage		$V_{DDQ} - 0.4$		$V_{DDQ} + 0.4$	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu A$			0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$	$V_{DDQ} - 0.1$			V
V_{PP1}	V_{PP} Program Voltage-Logic	Program, Erase	1.3	1.8	3.3	V
V_{PPH}	V_{PP} Program Voltage Factory	Program, Erase	11.4	12	12.6	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	V_{DD} Lock Voltage				1	V
V_{RPH}	\overline{RP} pin Extended High Voltage				3.3	V

Figure 10. Asynchronous Random Access Read AC waveforms

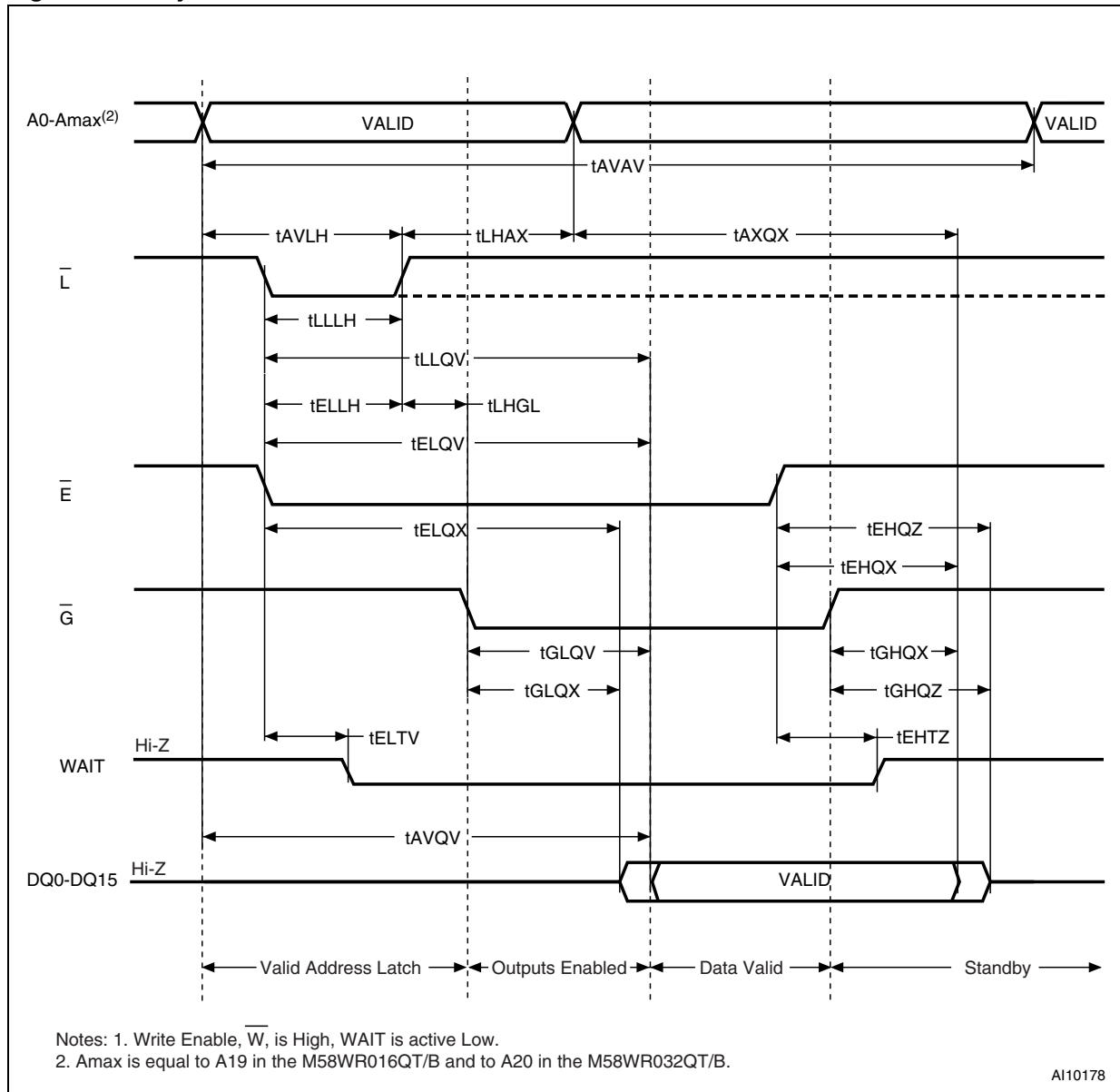


Figure 11. Asynchronous Page Read AC waveforms

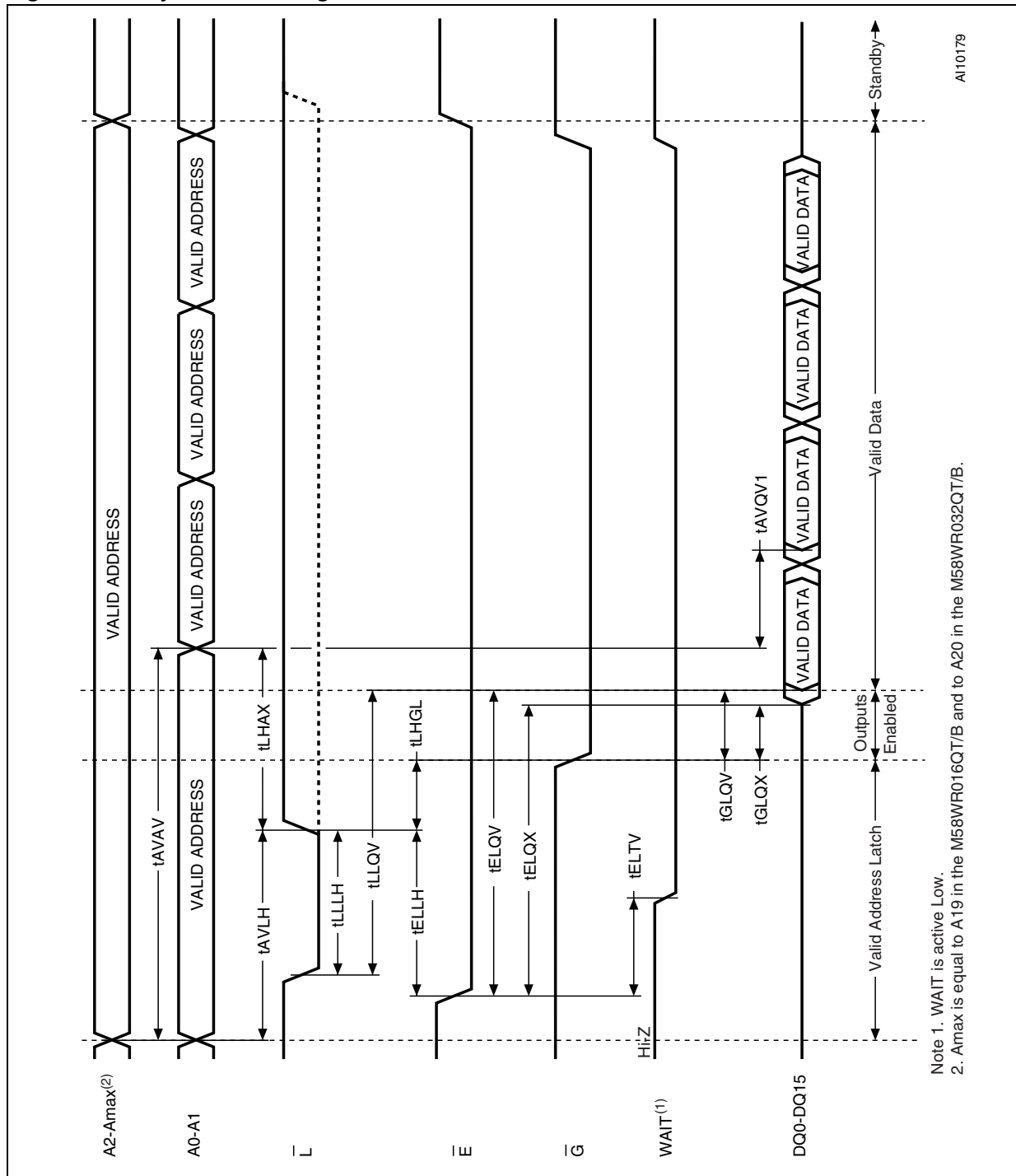


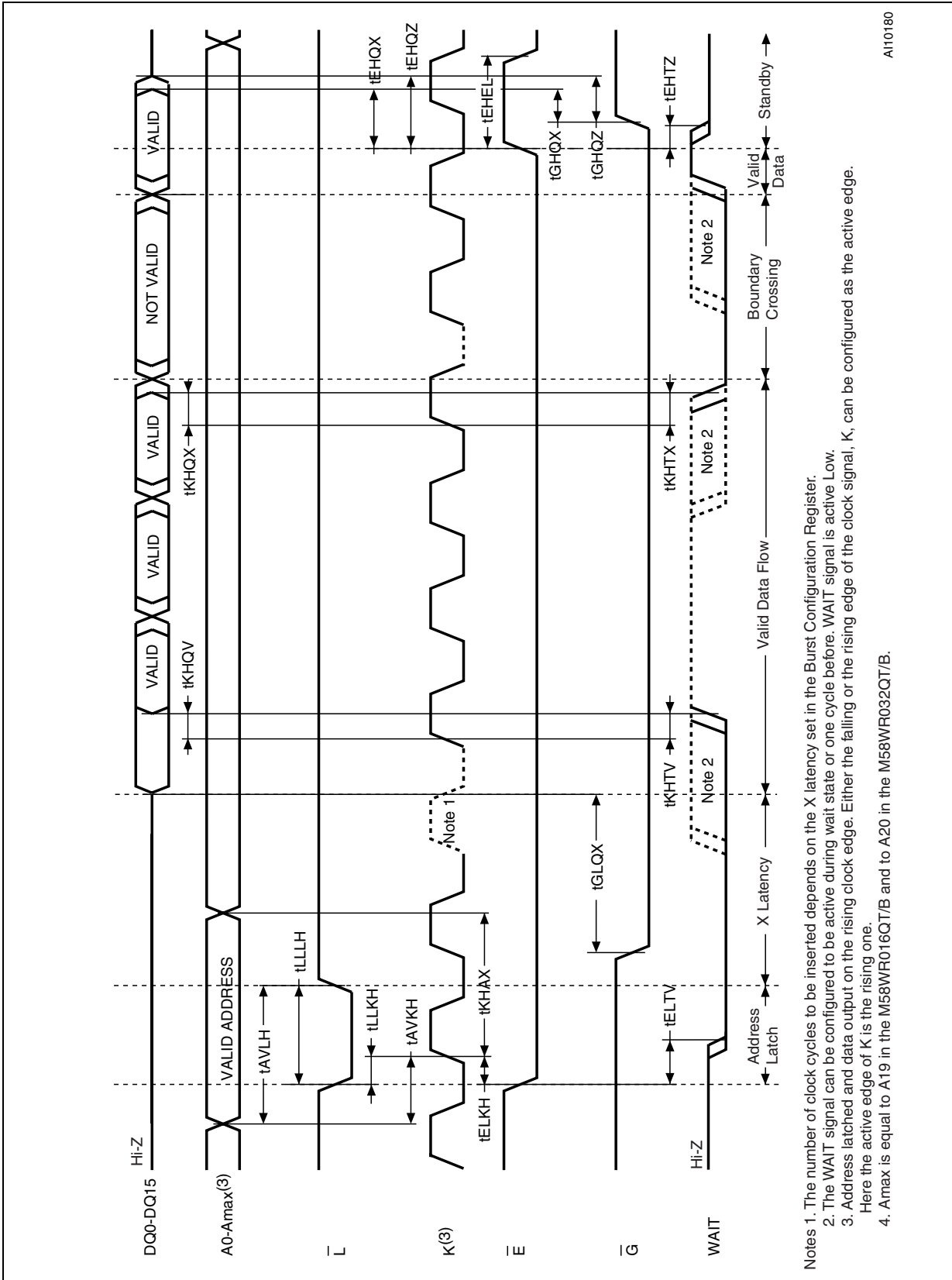
Table 21. Asynchronous Read AC characteristics

Symbol	Alt	Parameter	Min	M58WRxxxQT/B			Unit	
				60	70	80		
Read Timings	t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	60	70	80	ns
	t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	Max	60	70	80	ns
	t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	Max	20	20	25	ns
	$t_{AXQX}^{(1)}$	t_{OH}	Address Transition to Output Transition	Min	0	0	0	ns
	t_{ELTV}		Chip Enable Low to Wait Valid	Max	11	14	14	ns
	$t_{ELQV}^{(2)}$	t_{CE}	Chip Enable Low to Output Valid	Max	60	70	80	ns
	$t_{ELQX}^{(1)}$	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	0	ns
	t_{EHTZ}		Chip Enable High to Wait Hi-Z	Max	14	17	17	ns
	$t_{EHQX}^{(1)}$	t_{OH}	Chip Enable High to Output Transition	Min	0	0	0	ns
	$t_{EHQZ}^{(1)}$	t_{HZ}	Chip Enable High to Output Hi-Z	Max	14	17	17	ns
	$t_{GLQV}^{(2)}$	t_{OE}	Output Enable Low to Output Valid	Max	20	20	25	ns
	$t_{GLQX}^{(1)}$	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	0	ns
	$t_{GHQX}^{(1)}$	t_{OH}	Output Enable High to Output Transition	Min	0	0	0	ns
	$t_{GHQZ}^{(1)}$	t_{DF}	Output Enable High to Output Hi-Z	Max	14	14	14	ns
Latch Timings	t_{AVLH}	t_{AVADVH}	Address Valid to Latch Enable High	Min	7	9	9	ns
	t_{ELLH}	t_{ELADVH}	Chip Enable Low to Latch Enable High	Min	10	10	10	ns
	t_{LHAX}	t_{ADVHAX}	Latch Enable High to Address Transition	Min	7	9	9	ns
	t_{LLLH}	$t_{ADVLADVH}$	Latch Enable Pulse Width	Min	7	9	9	ns
	t_{LLQV}	t_{ADVLQV}	Latch Enable Low to Output Valid (Random)	Max	60	70	80	ns
	t_{LHGL}	t_{ADVHGL}	Latch Enable High to Output Enable Low	Min	0	0	0	ns

1. Sampled only, not 100% tested.

2. \bar{Q} may be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of \bar{E} without increasing t_{ELQV} .

Figure 12. Synchronous Burst Read AC waveforms



AI10180

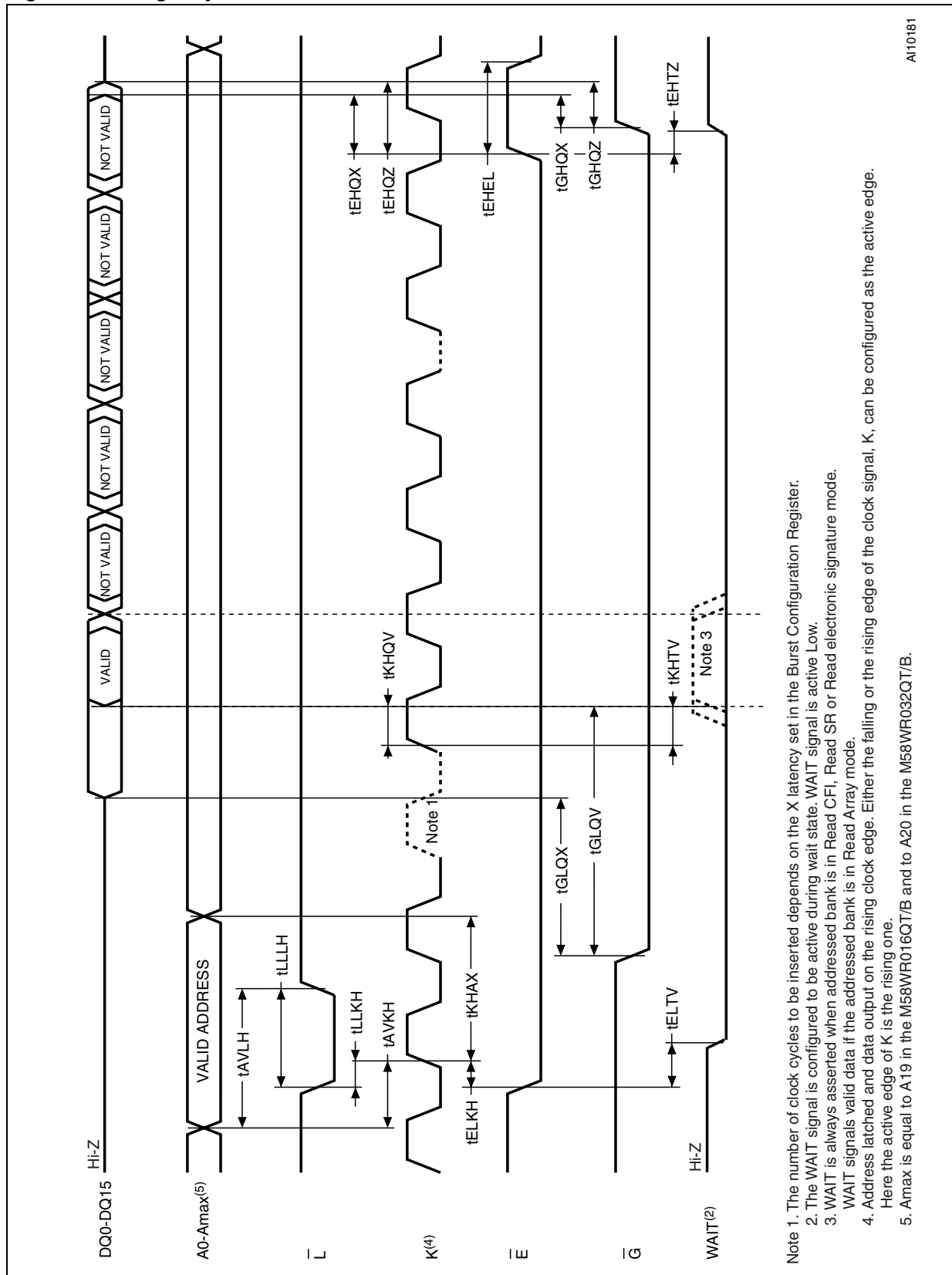
Notes 1. The number of clock cycles to be inserted depends on the X latency set in the Burst Configuration Register.

2. The WAIT signal can be configured to be active during wait state or one cycle before. WAIT signal is active Low.

3. Address latched and data output on the rising clock edge. Either the falling or the rising edge of the clock signal, K, can be configured as the active edge. Here the active edge of K is the rising one.

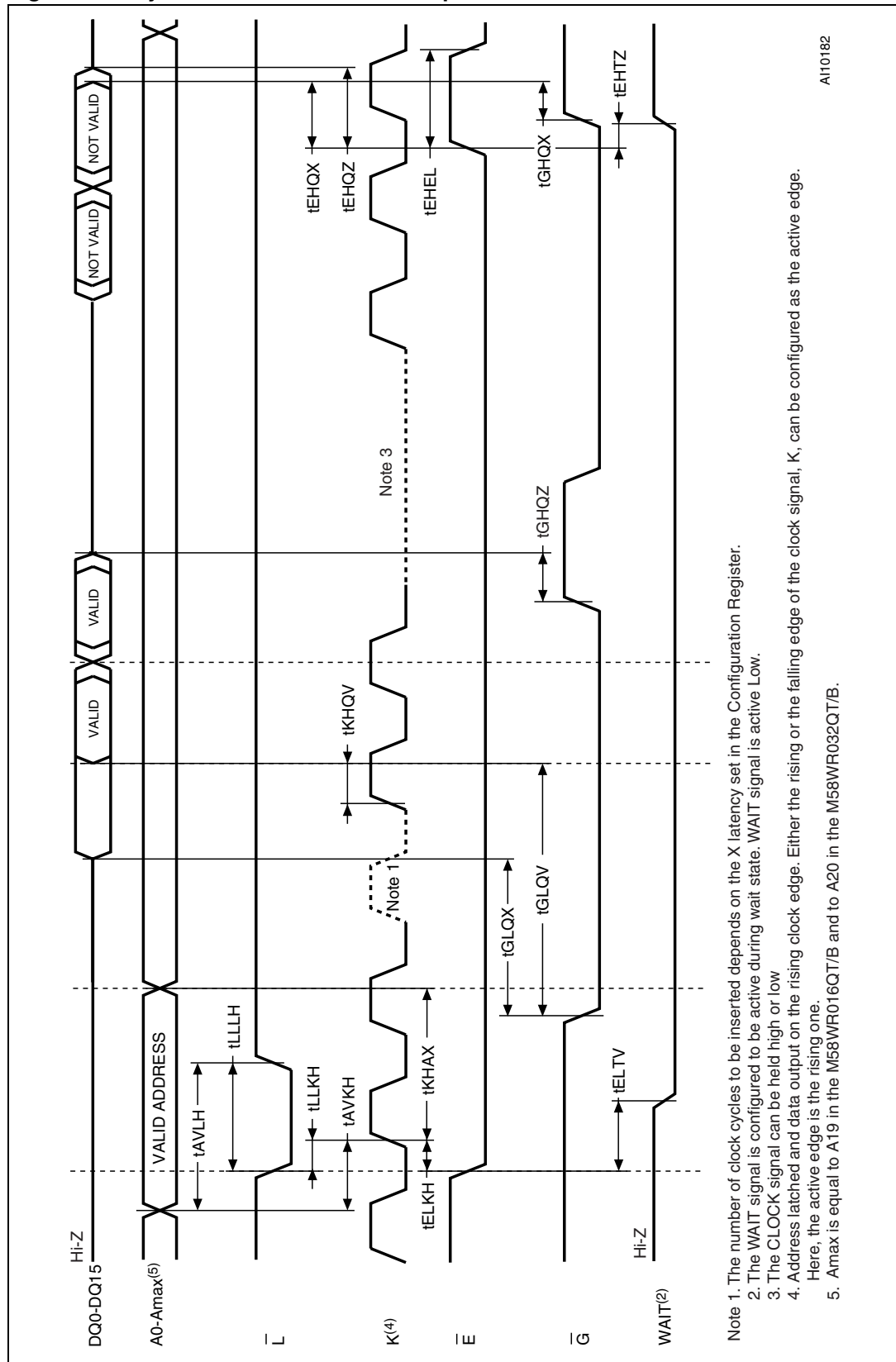
4. Amax is equal to A19 in the M58WR016QT/B and to A20 in the M58WR032QT/B.

Figure 13. Single Synchronous Read AC waveforms



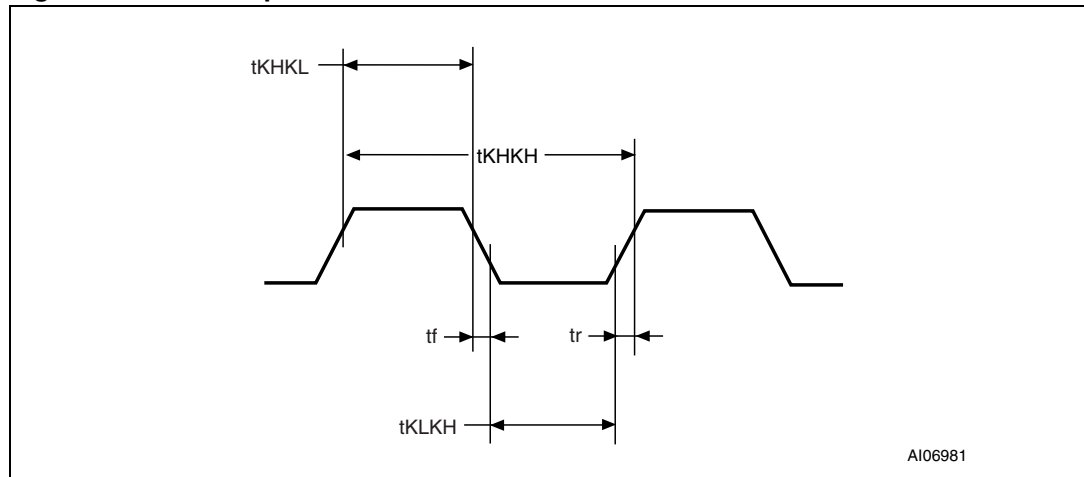
A10181

Figure 14. Synchronous Burst Read Suspend AC waveforms



A10182

Figure 15. Clock input AC waveform



AI06981

Table 22. Synchronous Read AC characteristics^{(1) (2)}

Symbol	Alt	Parameter		M58WRxxxQT/B			Unit	
				60	70	80		
Synchronous Read Timings	t_{AVKH}	t_{AVCLKH}	Address Valid to Clock High	Min	7	9	9	ns
	t_{ELKH}	t_{ELCLKH}	Chip Enable Low to Clock High	Min	7	9	9	ns
	t_{ELTV}		Chip Enable Low to Wait Valid	Max	11	14	14	ns
	t_{EHEL}		Chip Enable Pulse Width (subsequent synchronous reads)	Min	14	14	14	ns
	t_{EHTZ}		Chip Enable High to Wait Hi-Z	Max	11	14	14	ns
	t_{KHAX}	t_{CLKHAX}	Clock High to Address Transition	Min	7	9	9	ns
	t_{KHQV} t_{KHTV}	t_{CLKHQV}	Clock High to Output Valid Clock High to WAIT Valid	Max	11	14	14	ns
	t_{KHQX} t_{KHTX}	t_{CLKHQX}	Clock High to Output Transition Clock High to WAIT Transition	Min	3	4	4	ns
	t_{LLKH}	$t_{ADVLCLKH}$	Latch Enable Low to Clock High	Min	7	9	9	ns
Clock Specifications	t_{KHKH}	t_{CLK}	Clock Period (f=54MHz)	Min		18.5	18.5	ns
			Clock Period (f=66MHz)	Min	15			ns
	t_{KHKL} t_{KLKH}		Clock High to Clock Low Clock Low to Clock High	Min	3.5	4.5	4.5	ns
	t_f t_r		Clock Fall or Rise Time	Max	3	3	3	ns

1. Sampled only, not 100% tested.

2. For other timings please refer to [Table 21: Asynchronous Read AC characteristics](#).

Table 23. Write AC characteristics, Write Enable controlled⁽¹⁾

Symbol	Alt	Parameter		M58WRxxQT/B			Unit	
				60	70	80		
Write Enable Controlled Timings	t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	60	70	80	ns
	t_{AVLH}		Address Valid to Latch Enable High	Min	7	9	9	ns
	$t_{AVWH}^{(2)}$		Address Valid to Write Enable High	Min	40	45	50	ns
	t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Min	40	45	50	ns
	t_{ELLH}		Chip Enable Low to Latch Enable High	Min	10	10	10	ns
	t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	ns
	t_{ELQV}		Chip Enable Low to Output Valid	Min	60	70	80	ns
	t_{ELKV}		Chip Enable Low to Clock Valid	Min	7	9	9	ns
	t_{GHWL}		Output Enable High to Write Enable Low	Min	14	17	17	ns
	t_{LHAX}		Latch Enable High to Address Transition	Min	7	9	9	ns
	t_{LLLH}		Latch Enable Pulse Width	Min	7	9	9	ns
	$t_{WHAV}^{(2)}$		Write Enable High to Address Valid	Min	0	0	0	ns
	$t_{WHAX}^{(2)}$	t_{AH}	Write Enable High to Address Transition	Min	0	0	0	ns
	t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	0	ns
	t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	ns
	$t_{WHEL}^{(3)}$		Write Enable High to Chip Enable Low	Min	20	25	25	ns
	t_{WHGL}		Write Enable High to Output Enable Low	Min	0	0	0	ns
	t_{WHLL}		Write Enable High to Latch Enable Low	Min	0	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20	25	25	ns	
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	40	45	50	ns	
Protection Timings	t_{QVPL}		Output (Status Register) Valid to V_{PP} Low	Min	0	0	0	ns
	t_{QVWPL}		Output (Status Register) Valid to Write Protect Low	Min	0	0	0	ns
	t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	Min	200	200	200	ns
	t_{WHVPL}		Write Enable High to V_{PP} Low	Min	200	200	200	ns
	t_{WHWPL}		Write Enable High to Write Protect Low	Min	200	200	200	ns
	t_{WPHWH}		Write Protect High to Write Enable High	Min	200	200	200	ns

1. Sampled only, not 100% tested.

2. Meaningful only if \bar{L} is always kept low.

3. t_{WHEL} has this value when reading from the targeted bank or when reading from any address after a Set Configuration Register command has been issued. System designers should take this into account and may insert a software No-Op instruction to delay the first read in the same bank after issuing any command, or to delay the first read to any address after issuing a Set Configuration Register command. If the first read after the command is a Read Array operation in a different bank and no changes to the Configuration Register have been issued, t_{WHEL} is 0ns.

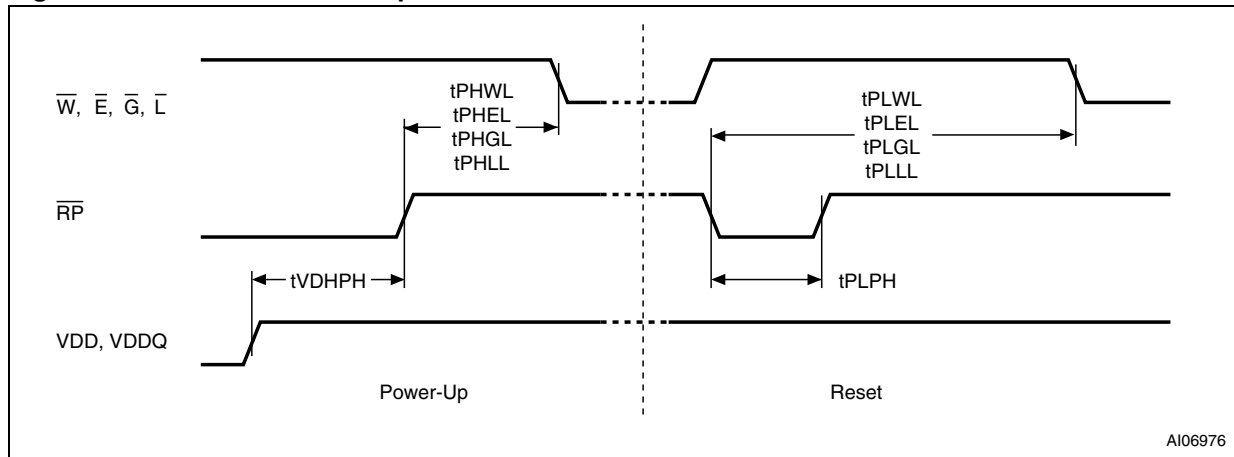
Table 24. Write AC characteristics, Chip Enable controlled⁽¹⁾

Symbol	Alt	Parameter		M58WRxxxQT/B			Unit	
				60	70	80		
Chip Enable Controlled Timings	t _{AVAV}	t _{WC}	Address Valid to Next Address Valid	Min	60	70	80	ns
	t _{AVEH}		Address Valid to Chip Enable High	Min	40	45	50	ns
	t _{AVLH}		Address Valid to Latch Enable High	Min	7	9	9	ns
	t _{DVEH}	t _{DS}	Data Valid to Chip Enable High	Min	40	45	50	ns
	t _{EHAX}	t _{AH}	Chip Enable High to Address Transition	Min	0	0	0	ns
	t _{EHDx}	t _{DH}	Chip Enable High to Input Transition	Min	0	0	0	ns
	t _{EHEL}	t _{CPH}	Chip Enable High to Chip Enable Low	Min	20	25	25	ns
	t _{EHGL}		Chip Enable High to Output Enable Low	Min	0	0	0	ns
	t _{EHWH}	t _{CH}	Chip Enable High to Write Enable High	Min	0	0	0	ns
	t _{ELKV}		Chip Enable Low to Clock Valid	Min	7	9	9	ns
	t _{ELEH}	t _{CP}	Chip Enable Low to Chip Enable High	Min	40	45	50	ns
	t _{ELLH}		Chip Enable Low to Latch Enable High	Min	10	10	10	ns
	t _{ELQV}		Chip Enable Low to Output Valid	Min	60	70	80	ns
	t _{GHEL}		Output Enable High to Chip Enable Low	Min	14	17	17	ns
	t _{LHAX}		Latch Enable High to Address Transition	Min	7	9	9	ns
	t _{LLLH}		Latch Enable Pulse Width	Min	7	9	9	ns
Protection Timings	t _{WHEL} ⁽²⁾		Write Enable High to Chip Enable Low	Min	20	25	25	ns
	t _{WLEL}	t _{CS}	Write Enable Low to Chip Enable Low	Min	0	0	0	ns
	t _{EHVPL}		Chip Enable High to V _{PP} Low	Min	200	200	200	ns
	t _{EHWPL}		Chip Enable High to Write Protect Low	Min	200	200	200	ns
	t _{QVVPL}		Output (Status Register) Valid to V _{PP} Low	Min	0	0	0	ns
	t _{QVWPL}		Output (Status Register) Valid to Write Protect Low	Min	0	0	0	ns
t _{VPHEH}	t _{VPS}	V _{PP} High to Chip Enable High	Min	200	200	200	ns	
t _{WPHEH}		Write Protect High to Chip Enable High	Min	200	200	200	ns	

1. Sampled only, not 100% tested.

2. t_{WHEL} has this value when reading from the targeted bank or when reading from any address after a Set Configuration Register command has been issued. System designers should take this into account and may insert a software No-Op instruction to delay the first read in the same bank after issuing any command, or to delay the first read to any address after issuing a Set Configuration Register command. If the first read after the command is a Read Array operation in a different bank and no changes to the Configuration Register have been issued, t_{WHEL} is 0ns.

Figure 18. Reset and Power-up AC waveforms



A106976

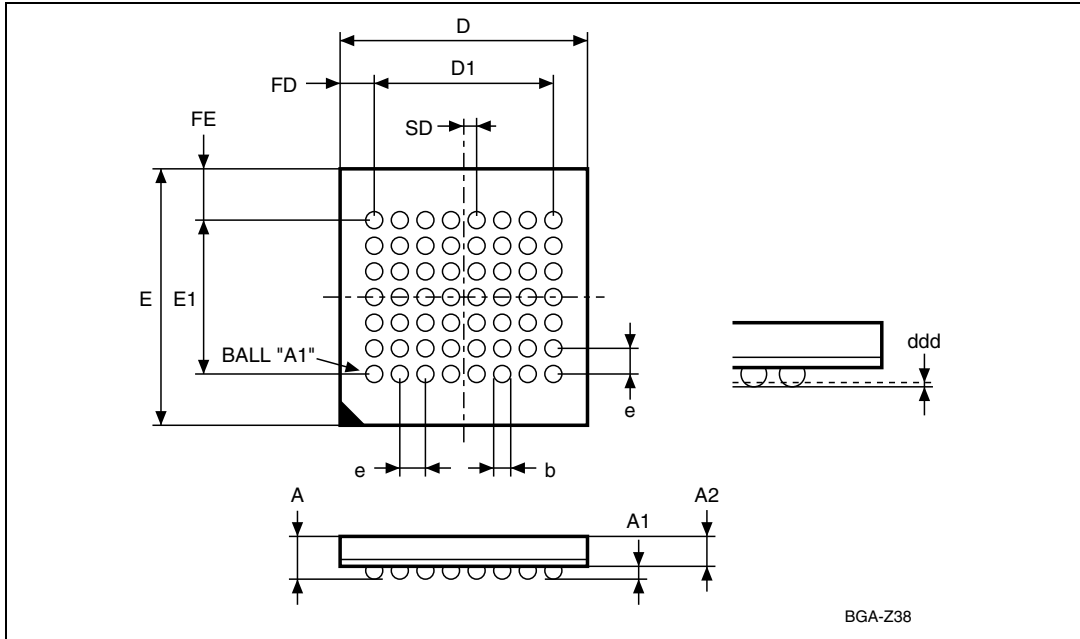
Table 25. Reset and Power-up AC characteristics

Symbol	Parameter	Test Condition		60	70	80	Unit
t_{PLWL} t_{PLEL} t_{PLGL} t_{PLLL}	Reset Low to Write Enable Low, Chip Enable Low, Output Enable Low, Latch Enable Low	During Program	Min	10	10	10	μs
		During Erase	Min	20	20	20	μs
		Other Conditions	Min	80	80	80	ns
t_{PHWL} t_{PHEL} t_{PHGL} t_{PHLL}	Reset High to Write Enable Low, Chip Enable Low, Output Enable Low, Latch Enable Low		Min	30	30	30	ns
$t_{PLPH}^{(1),(2)}$	\overline{RP} Pulse Width		Min	50	50	50	ns
$t_{VDHPH}^{(3)}$	Supply Voltages High to Reset High		Min	50	50	50	μs

1. The device Reset is possible but not guaranteed if $t_{PLPH} < 50ns$.
2. Sampled only, not 100% tested.
3. It is important to assert \overline{RP} in order to allow proper CPU initialization during Power-Up or Reset.

15 Package mechanical

Figure 19. VFPGA56 - 7.7x9mm, 8x7 ball array, 0.75mm pitch, Bottom View Package Outline



1. Drawing is not to scale.

Table 26. VFPGA56 - 7.7x9mm, 8x7 ball array, 0.75mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.000			0.0394
A1		0.200			0.0079	
A2	0.660			0.0260		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	7.700	7.600	7.800	0.3031	0.2992	0.3071
D1	5.250	-	-	0.2067	-	-
ddd			0.080			0.0031
e	0.750	-	-	0.0295	-	-
E	9.000	8.900	9.100	0.3543	0.3504	0.3583
E1	4.500	-	-	0.1772	-	-
FD	1.225	-	-	0.0482	-	-
FE	2.250	-	-	0.0886	-	-
SD	0.375	-	-	0.0148	-	-

16 Part numbering

Table 27. Ordering information scheme

Example:	M58WR016QT	70	ZB	6	T
Device Type M58					
Architecture W = Multiple Bank, Burst Mode					
Operating Voltage R = $V_{DD} = 1.7V$ to $2V$, $V_{DDQ} = 1.7V$ to $2.24V$					
Density 016 = 16 Mbit (x16) 032 = 32 Mbit (x16)					
Technology Q = $0.11\mu m$ technology					
Parameter Location T = Top Boot B = Bottom Boot					
Speed 60 = 60ns 70 = 70ns 80 = 80ns					
Package ZB = VFPGA56, 7.7x9mm, 0.75mm pitch					
Temperature Range 6 = -40 to $85^{\circ}C$					
Option Blank = Standard Packing T = Tape & Reel Packing E = ECOPACK® Package, Standard Packing F = ECOPACK® Package, Tape & Reel Packing					

Table 28. Daisy chain ordering scheme

Example: M58WR016QT ZB T

Device Type

M58WR016Q

Daisy Chain

ZB = VFPGA56, 7.7x9mm, 0.75mm pitch

Option

Blank = Standard Packing

T = Tape & Reel Packing

E = ECOPACK® Package, Standard Packing

F = ECOPACK®, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.

Appendix A Block address tables

Table 29. Top boot block addresses, M58WR016QT

Bank ⁽¹⁾	#	Size (KWord)	Address Range
Parameter Bank	0	4	FF000-FFFFF
	1	4	FE000-FEFFF
	2	4	FD000-FDFFF
	3	4	FC000-FCFFF
	4	4	FB000-FBFFF
	5	4	FA000-FAFFF
	6	4	F9000-F9FFF
	7	4	F8000-F8FFF
	8	32	F0000-F7FFF
	9	32	E8000-EFFFF
	10	32	E0000-E7FFF
	11	32	D8000-DFFFF
	12	32	D0000-D7FFF
	13	32	C8000-CFFFF
14	32	C0000-C7FFF	
Bank 1	15	32	B8000-BFFFF
	16	32	B0000-B7FFF
	17	32	A8000-AFFFF
	18	32	A0000-A7FFF
	19	32	98000-9FFFF
	20	32	90000-97FFF
	21	32	88000-8FFFF
	22	32	80000-87FFF
Bank 2	23	32	78000-7FFFF
	24	32	70000-77FFF
	25	32	68000-6FFFF
	26	32	60000-67FFF
	27	32	58000-5FFFF
	28	32	50000-57FFF
	29	32	48000-4FFFF
	30	32	40000-47FFF

Table 29. Top boot block addresses, M58WR016QT (continued)

Bank 3	31	32	38000-3FFFF
	32	32	30000-37FFF
	33	32	28000-2FFFF
	34	32	20000-27FFF
	35	32	18000-1FFFF
	36	32	10000-17FFF
	37	32	08000-0FFFF
	38	32	00000-07FFF

1. There are two Bank Regions: Bank Region 1 contains all the banks that are made up of main blocks only; Bank Region 2 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Table 30. Bottom boot block addresses, M58WR016QB

Bank ⁽¹⁾	#	Size (KWord)	Address Range
Bank 3	38	32	F8000-FFFFFF
	37	32	F0000-F7FFF
	36	32	E8000-EFFFF
	35	32	E0000-E7FFF
	34	32	D8000-DFFFF
	33	32	D0000-D7FFF
	32	32	C8000-CFFFF
	31	32	C0000-C7FFF
Bank 2	30	32	B8000-BFFFF
	29	32	B0000-B7FFF
	28	32	A8000-AFFFF
	27	32	A0000-A7FFF
	26	32	98000-9FFFF
	25	32	90000-97FFF
	24	32	88000-8FFFF
	23	32	80000-87FFF
Bank 1	22	32	78000-7FFFF
	21	32	70000-77FFF
	20	32	68000-6FFFF
	19	32	60000-67FFF
	18	32	58000-5FFFF
	17	32	50000-57FFF
	16	32	48000-4FFFF
	15	32	40000-47FFF

Table 30. Bottom boot block addresses, M58WR016QB (continued)

Parameter Bank	14	32	38000-3FFFF
	13	32	30000-37FFF
	12	32	28000-2FFFF
	11	32	20000-27FFF
	10	32	18000-1FFFF
	9	32	10000-17FFF
	8	32	08000-0FFFF
	7	4	07000-07FFF
	6	4	06000-06FFF
	5	4	05000-05FFF
	4	4	04000-04FFF
	3	4	03000-03FFF
	2	4	02000-02FFF
	1	4	01000-01FFF
	0	4	00000-00FFF

1. There are two Bank Regions: Bank Region 2 contains all the banks that are made up of main blocks only; Bank Region 1 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Table 31. Top boot block addresses, M58WR032QT

Bank ⁽¹⁾	#	Size (KWord)	Address Range
Parameter Bank	0	4	1FF000-1FFFFFF
	1	4	1FE000-1FEFFF
	2	4	1FD000-1FDFFF
	3	4	1FC000-1FCFFF
	4	4	1FB000-1FBFFF
	5	4	1FA000-1FAFFF
	6	4	1F9000-1F9FFF
	7	4	1F8000-1F8FFF
	8	32	1F0000-1F7FFF
	9	32	1E8000-1EFFFF
	10	32	1E0000-1E7FFF
	11	32	1D8000-1DFFFF
	12	32	1D0000-1D7FFF
	13	32	1C8000-1CFFFF
	14	32	1C0000-1C7FFF

Table 31. Top boot block addresses, M58WR032QT (continued)

Bank 1	15	32	1B8000-1BFFFF
	16	32	1B0000-1B7FFF
	17	32	1A8000-1AFFFF
	18	32	1A0000-1A7FFF
	19	32	198000-19FFFF
	20	32	190000-197FFF
	21	32	188000-18FFFF
	22	32	180000-187FFF
Bank 2	23	32	178000-17FFFF
	24	32	170000-177FFF
	25	32	168000-16FFFF
	26	32	160000-167FFF
	27	32	158000-15FFFF
	28	32	150000-157FFF
	29	32	148000-14FFFF
	30	32	140000-147FFF
Bank 3	31	32	138000-13FFFF
	32	32	130000-137FFF
	33	32	128000-12FFFF
	34	32	120000-127FFF
	35	32	118000-11FFFF
	36	32	110000-117FFF
	37	32	108000-10FFFF
	38	32	100000-107FFF
Bank 4	39	32	0F8000-0FFFFF
	40	32	0F0000-0F7FFF
	41	32	0E8000-0EFFFF
	42	32	0E0000-0E7FFF
	43	32	0D8000-0DFFFF
	44	32	0D0000-0D7FFF
	45	32	0C8000-0CFFFF
	46	32	0C0000-0C7FFF

Table 31. Top boot block addresses, M58WR032QT (continued)

Bank 5	47	32	0B8000-0BFFFF
	48	32	0B0000-0B7FFF
	49	32	0A8000-0AFFFF
	50	32	0A0000-0A7FFF
	51	32	098000-09FFFF
	52	32	090000-097FFF
	53	32	088000-08FFFF
	54	32	080000-087FFF
Bank 6	55	32	078000-07FFFF
	56	32	070000-077FFF
	57	32	068000-06FFFF
	58	32	060000-067FFF
	59	32	058000-05FFFF
	60	32	050000-057FFF
	61	32	048000-04FFFF
	62	32	040000-047FFF
Bank 7	63	32	038000-03FFFF
	64	32	030000-037FFF
	65	32	028000-02FFFF
	66	32	020000-027FFF
	67	32	018000-01FFFF
	68	32	010000-017FFF
	69	32	008000-00FFFF
	70	32	000000-007FFF

1. There are two Bank Regions: Bank Region 1 contains all the banks that are made up of main blocks only; Bank Region 2 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Table 32. Bottom boot block addresses, M58WR032QB

Bank ⁽¹⁾	#	Size (KWord)	Address Range
Bank 7	70	32	1F8000-1FFFFFFF
	69	32	1F0000-1F7FFF
	68	32	1E8000-1EFFFF
	67	32	1E0000-1E7FFF
	66	32	1D8000-1DFFFF
	65	32	1D0000-1D7FFF
	64	32	1C8000-1CFFFF
	63	32	1C0000-1C7FFF

Table 32. Bottom boot block addresses, M58WR032QB (continued)

Bank 6	62	32	1B8000-1BFFFF
	61	32	1B0000-1B7FFF
	60	32	1A8000-1AFFFF
	59	32	1A0000-1A7FFF
	58	32	198000-19FFFF
	57	32	190000-197FFF
	56	32	188000-18FFFF
	55	32	180000-187FFF
Bank 5	54	32	178000-17FFFF
	53	32	170000-177FFF
	52	32	168000-16FFFF
	51	32	160000-167FFF
	50	32	158000-15FFFF
	49	32	150000-157FFF
	48	32	148000-14FFFF
	47	32	140000-147FFF
Bank 4	46	32	138000-13FFFF
	45	32	130000-137FFF
	44	32	128000-12FFFF
	43	32	120000-127FFF
	42	32	118000-11FFFF
	41	32	110000-117FFF
	40	32	108000-10FFFF
	39	32	100000-107FFF
Bank 3	38	32	0F8000-0FFFFF
	37	32	0F0000-0F7FFF
	36	32	0E8000-0EFFFF
	35	32	0E0000-0E7FFF
	34	32	0D8000-0DFFFF
	33	32	0D0000-0D7FFF
	32	32	0C8000-0CFFFF
	31	32	0C0000-0C7FFF

Table 32. Bottom boot block addresses, M58WR032QB (continued)

Bank 2	30	32	0B8000-0BFFFF
	29	32	0B0000-0B7FFF
	28	32	0A8000-0AFFFF
	27	32	0A0000-0A7FFF
	26	32	098000-09FFFF
	25	32	090000-097FFF
	24	32	088000-08FFFF
	23	32	080000-087FFF
Bank 1	22	32	078000-07FFFF
	21	32	070000-077FFF
	20	32	068000-06FFFF
	19	32	060000-067FFF
	18	32	058000-05FFFF
	17	32	050000-057FFF
	16	32	048000-04FFFF
	15	32	040000-047FFF
Parameter Bank	14	32	038000-03FFFF
	13	32	030000-037FFF
	12	32	028000-02FFFF
	11	32	020000-027FFF
	10	32	018000-01FFFF
	9	32	010000-017FFF
	8	32	008000-00FFFF
	7	4	007000-007FFF
	6	4	006000-006FFF
	5	4	005000-005FFF
	4	4	004000-004FFF
	3	4	003000-003FFF
	2	4	002000-002FFF
	1	4	001000-001FFF
	0	4	000000-000FFF

1. There are two Bank Regions: Bank Region 2 contains all the banks that are made up of main blocks only; Bank Region 1 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Appendix B Common Flash Interface

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables [33](#), [34](#), [35](#), [36](#), [37](#), [38](#), [39](#), [40](#), [41](#) and [42](#) show the addresses used to retrieve the data. The Query data is always presented on the lowest order data outputs (DQ0-DQ7), the other outputs (DQ8-DQ15) are set to 0.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see [Figure 5: Protection Register Memory Map](#)). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by Numonyx. Issue a Read Array command to return to Read mode.

Table 33. Query structure overview⁽¹⁾

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
80h	Security Code Area	Lock Protection Register Unique device Number and User Programmable OTP

1. The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables [34](#), [35](#), [36](#) and [37](#). Query data is always presented on the lowest order data outputs.

Table 34. CFI Query identification string

Offset	Sub-section Name	Description	Value
00h	0020h	Manufacturer Code	Numonyx
01h	8812h 8813h 8814h 8815h	Device Code	Top (M58WR016QT) Bottom (M58WR016QB) Top (M58WR032QT) Bottom (M58WR032QB)
02h	reserved	Reserved	
03h	reserved	reserved	
04h-0Fh	reserved	Reserved	
10h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	0052h		"R"
12h	0059h		"Y"
13h 14h	0003h 0000h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	
15h 16h	offset = P = 0039h 0000h	Address for Primary Algorithm extended Query table (see Table 36)	p = 39h
17h 18h	0000h 0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
19h 1Ah	value = A = 0000h 0000h	Address for Alternate Algorithm extended Query table	NA

Table 35. CFI query system interface information

Offset	Data	Description	Value
1Bh	0017h	V _{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 millivolts	1.7V
1Ch	0020h	V _{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 millivolts	2V
1Dh	00B4h	V _{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 millivolts	11.4V
1Eh	00C6h	V _{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 millivolts	12.6V
1Fh	0004h	Typical time-out per single byte/word program = 2 ⁿ μs	16μs
20h	0000h	Typical time-out for multi-Byte program = 2 ⁿ μs	NA
21h	000Ah	Typical time-out per individual block erase = 2 ⁿ ms	1s
22h	0000h	Typical time-out for full chip erase = 2 ⁿ ms	NA
23h	0003h	Maximum time-out for word program = 2 ⁿ times typical	128μs
24h	0000h	Maximum time-out for multi-Byte program = 2 ⁿ times typical	NA
25h	0002h	Maximum time-out per individual block erase = 2 ⁿ times typical	4s
26h	0000h	Maximum time-out for chip erase = 2 ⁿ times typical	NA

Table 36. Device geometry definition

Offset Word Mode	Data	Description	Value	
27h	0015h ⁽¹⁾	Device Size = 2 ⁿ in number of bytes	2 MBytes	
	0016h ⁽²⁾		4 MBytes	
28h 29h	0001h 0000h	Flash Device Interface Code description	x16 Async.	
2Ah 2Bh	0000h 0000h	Maximum number of bytes in multi-byte program or page = 2 ⁿ	NA	
2Ch	0002h	Number of identical sized erase block regions within the device bit 7 to 0 = x = number of Erase Block Regions	2	
TOP DEVICES	2Dh 2Eh	001Eh 0000h	M58WR016QT/B Erase Block Region 1 Information Number of identical-size erase blocks = 001Eh+1	31
		003Eh 0000h	M58WR032QT/B Erase Block Region 1 Information Number of identical-size erase blocks = 003Eh+1	63
	2Fh 30h	0000h 0001h	Erase Block Region 1 Information Block size in Region 1 = 0100h * 256 byte	64 KByte
		0007h 0000h	Erase Block Region 2 Information Number of identical-size erase blocks = 0007h+1	8
	33h 34h	0020h 0000h	Erase Block Region 2 Information Block size in Region 2 = 0020h * 256 byte	8 KByte
		35h 38h	Reserved for future erase block region information	
BOTTOM DEVICES	2Dh 2Eh	0007h 0000h	Erase Block Region 1 Information Number of identical-size erase block = 0007h+1	8
		0020h 0000h	Erase Block Region 1 Information Block size in Region 1 = 0020h * 256 byte	8 KByte
	31h 32h	001Eh 0000h	M58WR016QT/B Erase Block Region 2 Information Number of identical-size erase block = 001Eh+1	31
		003Eh 0000h	M58WR032QT/B Erase Block Region 2 Information Number of identical-size erase block = 003Eh+1	63
	33h 34h	0000h 0001h	Erase Block Region 2 Information Block size in Region 2 = 0100h * 256 byte	64 KByte
35h 38h	Reserved for future erase block region information		NA	

1. Applies to M58WR016QT/B only.

2. Applies to M58WR032QT/B only.

Table 37. Primary algorithm-specific extended query table

Offset	Data	Description	Value
(P)h = 39h	0050h 0052h 0049h	Primary Algorithm extended Query table unique ASCII string "PRI"	"P" "R" "I"
(P+3)h = 3Ch	0031h	Major version number, ASCII	"1"
(P+4)h = 3Dh	0033h	Minor version number, ASCII	"3"
(P+5)h = 3Eh (P+7)h = 40h (P+8)h = 41h	00E6h 0003h 0000h 0000h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte. bit 0Chip Erase supported (1 = Yes, 0 = No) bit 1Erase Suspend supported (1 = Yes, 0 = No) bit 2Program Suspend supported (1 = Yes, 0 = No) bit 3Legacy Lock/Unlock supported (1 = Yes, 0 = No) bit 4Queued Erase supported (1 = Yes, 0 = No) bit 5Instant individual block locking supported (1 = Yes, 0 = No) bit 6Protection bits supported (1 = Yes, 0 = No) bit 7Page mode read supported (1 = Yes, 0 = No) bit 8Synchronous read supported (1 = Yes, 0 = No) bit 9Simultaneous operation supported (1 = Yes, 0 = No) bit 10 to 31Reserved; undefined bits are '0'. If bit 31 is '1' then another 31 bit field of optional features follows at the end of the bit-30 field.	No Yes Yes No No Yes Yes Yes Yes Yes
(P+9)h = 42h	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query bit 0Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1Reserved; undefined bits are '0'	Yes
(P+A)h = 43h (P+B)h = 44h	0003h 0000h	Block Protect Status Defines which bits in the Block Status Register section of the Query are implemented. bit 0Block protect Status Register Lock/Unlock bit active(1 = Yes, 0 = No) bit 1Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No) bit 15 to 2Reserved for future use; undefined bits are '0'	Yes Yes
(P+C)h = 45h	0018h	V _{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	1.8V
(P+D)h = 46h	00C0h	V _{PP} Supply Optimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	12V

Table 38. Protection Register Information

Offset	Data	Description	Value
(P+E)h = 47h	0001h	Number of protection register fields in JEDEC ID space. 0000h indicates that 256 fields are available.	1
(P+F)h = 48h	0080h	Protection Field 1: Protection Description	0080h
(P+10)h = 49h	0000h	Bits 0-7 Lower byte of protection register address	
(P+11)h = 4Ah	0003h	Bits 8-15 Upper byte of protection register address	8 Bytes
(P+12)h = 4Bh	0004h	Bits 16-23 2 ⁿ bytes in factory pre-programmed region	16 Bytes
		Bits 24-31 2 ⁿ bytes in user programmable region	

Table 39. Burst Read information

Offset	Data	Description	Value
(P+13)h = 4Ch	0003h	Page-mode read capability bits 0-7'n' such that 2 ⁿ HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width.	8 Bytes
(P+14)h = 4Dh	0004h	Number of synchronous mode read configuration fields that follow.	4
(P+15)h = 4Eh	0001h	Synchronous mode read capability configuration 1 bit 3-7Reserved bit 0-2'n' such that 2 ⁿ⁺¹ HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bit 0-2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	4
(P+16)h = 4Fh	0002h	Synchronous mode read capability configuration 2	8
(P+17)h = 50h	0003h	Synchronous mode read capability configuration 3	16
(P+18)h = 51h	0007h	Synchronous mode read capability configuration 4	Cont.

Table 40. Bank and erase block region information^{(1) (2)}

TOP DEVICES		BOTTOM DEVICES		Description
Offset	Data	Offset	Data	
(P+19)h = 52h	02h	(P+19)h = 52h	02h	Number of Bank Regions within the device

1. The variable P is a pointer which is defined at CFI offset 15h.
2. Bank Regions. There are two Bank Regions, see [Table 29](#) and [Table 30](#) for the M58WR016QT/B and see [Table 31](#) and [Table 32](#) for the M58WR032QT/B.

Table 41. Bank and erase block region 1 information⁽¹⁾

TOP DEVICES		BOTTOM DEVICES		Description
Offset	Data	Offset	Data	
(P+1A)h = 53h	03h ⁽²⁾	(P+1A)h = 53h	01h	Number of identical banks within Bank Region 1
	07h ⁽³⁾			
(P+1B)h = 54h	00h	(P+1B)h = 54h	00h	
(P+1C)h = 55h	11h	(P+1C)h = 55h	11h	Number of program or erase operations allowed in Bank region 1: Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+1D)h = 56h	00h	(P+1D)h = 56h	00h	Number of program or erase operations allowed in other banks while a bank in same region is programming Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+1E)h = 57h	00h	(P+1E)h = 57h	00h	Number of program or erase operations allowed in other banks while a bank in this region is erasing Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+1F)h = 58h	01h	(P+1F)h = 58h	02h	Types of erase block regions in Bank region 1 n = number of erase block regions with contiguous same-size erase blocks. Symmetrically blocked banks have one blocking region. ⁽⁴⁾
(P+20)h = 59h	07h	(P+20)h = 59h	07h	Bank Region 1 Erase Block Type 1 Information Bits 0-15: n+1 = number of identical-sized erase blocks in each bank Bits 16-31: nx256 = number of bytes in erase block region
(P+21)h = 5Ah	00h	(P+21)h = 5Ah	00h	
(P+22)h = 5Bh	00h	(P+22)h = 5Bh	20h	
(P+23)h = 5Ch	01h	(P+23)h = 5Ch	00h	
(P+24)h = 5Dh	64h	(P+24)h = 5Dh	64h	Bank Region 1 (Erase Block Type 1) Minimum block erase cycles × 1000
(P+25)h = 5Eh	00h	(P+25)h = 5Eh	00h	
(P+26)h = 5Fh	01h	(P+26)h = 5Fh	01h	Bank Region 1 (Erase Block Type 1): Blts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for "internal ECC used" Blts 5-7: reserved 5Eh 01 5Eh 01
(P+27)h = 60h	03h	(P+27)h = 60h	03h	Bank Region 1 (Erase Block Type 1): Page mode and synchronous mode capabilities Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved

Table 41. Bank and erase block region 1 information⁽¹⁾ (continued)

TOP DEVICES		BOTTOM DEVICES		Description
Offset	Data	Offset	Data	
		(P+28)h = 61h	06h	Bank Region 1 Erase Block Type 2 Information
		(P+29)h = 62h	00h	Bits 0-15: n+1 = number of identical-sized erase blocks
		(P+2A)h = 63h	00h	Bits 16-31: n×256 = number of bytes in erase block region
		(P+2B)h = 64h	01h	
		(P+2C)h = 65h	64h	Bank Region 1 (Erase Block Type 2)
		(P+2D)h = 66h	00h	Minimum block erase cycles × 1000
		(P+2E)h = 67h	01h	Bank Region 1 (Erase Block Type 2): Blts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” Blts 5-7: reserved
		(P+2F)h = 68h	03h	Bank Region 1 (Erase Block Type 2): Page mode and synchronous mode capabilities Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved

1. The variable P is a pointer which is defined at CFI offset 15h.
2. Applies to the M58WR016QT/B only.
3. Applies to the M58WR032QT/B only.
4. Bank Regions. There are two Bank Regions, see [Table 29](#) and [Table 30](#) for the M58WR016QT/B and see [Table 31](#) and [Table 32](#) for the M58WR032QT/B.

Table 42. Bank and erase block region 2 information⁽¹⁾

TOP DEVICES		BOTTOM DEVICES		Description
Offset	Data	Offset	Data	
(P+28)h = 61h	01h	(P+30)h = 69h	03h ⁽²⁾	Number of identical banks within bank region 2
			07h ⁽³⁾	
(P+29)h = 62h	00h	(P+31)h = 6Ah	00h	
(P+2A)h = 63h	11h	(P+32)h = 6Bh	11h	Number of program or erase operations allowed in bank region 2: Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+2B)h = 64h	00h	(P+33)h = 6Ch	00h	Number of program or erase operations allowed in other banks while a bank in this region is programming Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+2C)h = 65h	00h	(P+34)h = 6Dh	00h	Number of program or erase operations allowed in other banks while a bank in this region is erasing Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+2D)h = 66h	02h	(P+35)h = 6Eh	01h	Types of erase block regions in Bank region 2 n = number of erase block regions with contiguous same-size erase blocks. Symmetrically blocked banks have one blocking region. ⁽⁴⁾
(P+2E)h = 67h	06h	(P+36)h = 6Fh	07h	Bank Region 2 Erase Block Type 1 Information Bits 0-15: n+1 = number of identical-sized erase blocks in each bank Bits 16-31: nx256 = number of bytes in erase block region
(P+2F)h = 68h	00h	(P+37)h = 70h	00h	
(P+30)h = 69h	00h	(P+38)h = 71h	00h	
(P+31)h = 6Ah	01h	(P+39)h = 72h	01h	
(P+32)h = 6Bh	64h	(P+3A)h = 73h	64h	Bank Region 2 (Erase Block Type 1) Minimum block erase cycles × 1000
(P+33)h = 6Ch	00h	(P+3B)h = 74h	00h	
(P+34)h = 6Dh	01h	(P+3C)h = 75h	01h	Bank Region 2 (Erase Block Type 1): Blts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for "internal ECC used" Blts 5-7: reserved

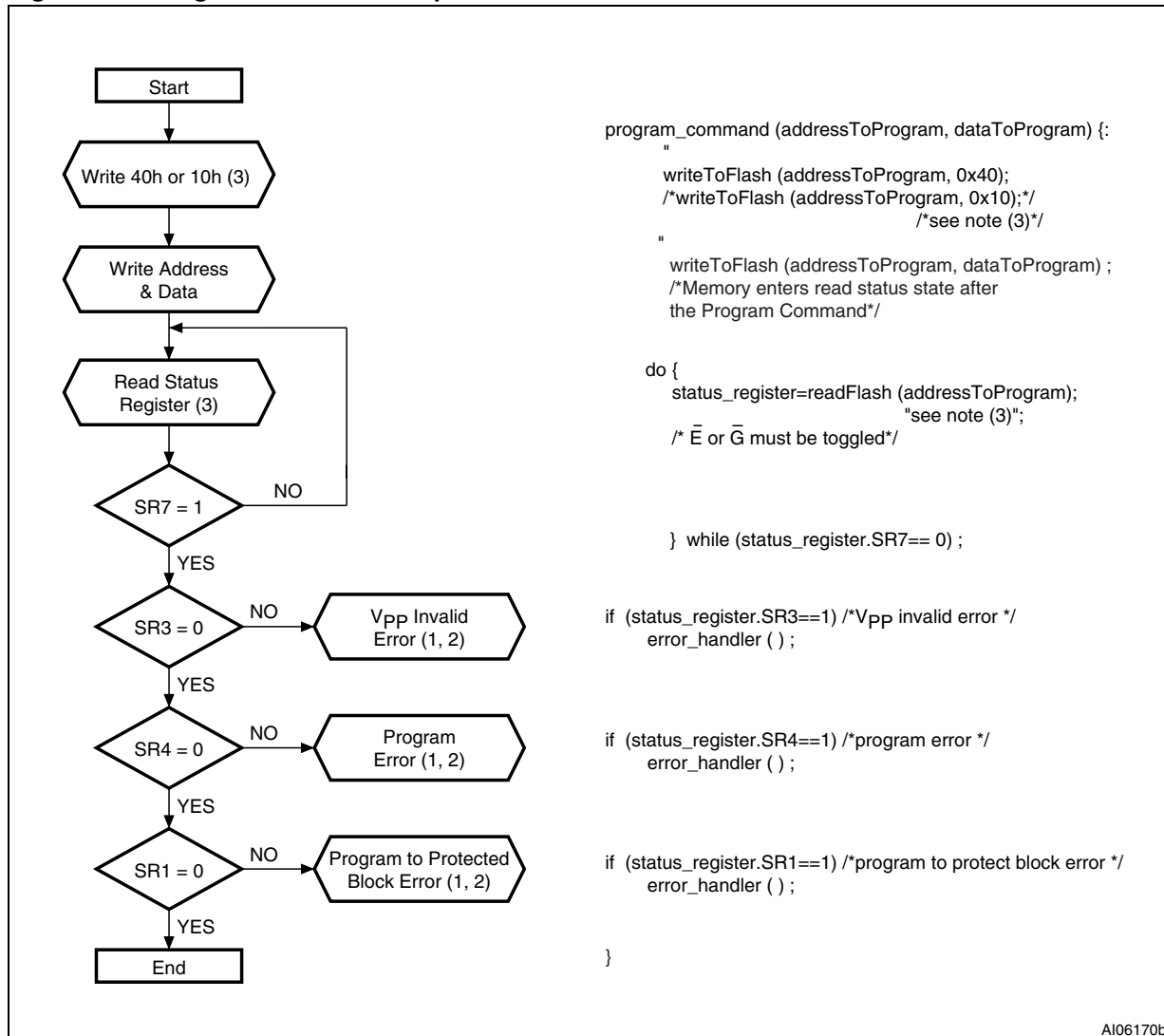
Table 42. Bank and erase block region 2 information⁽¹⁾ (continued)

TOP DEVICES		BOTTOM DEVICES		Description
Offset	Data	Offset	Data	
(P+35)h = 6Eh	03h	(P+3D)h = 76h	03h	Bank Region 2 (Erase Block Type 1): Page mode and synchronous mode capabilities (defined in Table 39) Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved
(P+36)h = 6Fh	07h			Bank Region 2 Erase Block Type 2 Information Bits 0-15: n+1 = number of identical-sized erase blocks Bits 16-31: nx256 = number of bytes in erase block region
(P+37)h = 70h	00h			
(P+38)h = 71h	20h			
(P+39)h = 72h	00h			
(P+3A)h = 73h	64h			Bank Region 2 (Erase Block Type 2) Minimum block erase cycles × 1000
(P+3B)h = 74h	00h			
(P+3C)h = 75h	01h			Bank Region 2 (Erase Block Type 2): Bits per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” Bits 5-7: reserved
(P+3D)h = 76h	03h			Bank Region 2 (Erase Block Type 2): Page mode and synchronous mode capabilities (defined in Table 39) Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved
(P+3E)h = 77h		(P+3E)h = 77h		Feature Space definitions
(P+3F)h = 78h		(P+3F)h = 78h		Reserved

1. The variable P is a pointer which is defined at CFI offset 15h.
2. Applies to the M58WR016QT/B only.
3. Applies to the M58WR032QT/B only.
4. Bank Regions. There are two Bank Regions, see [Table 29](#) and [Table 30](#) for the M58WR016QT/B and see [Table 31](#) and [Table 32](#) for the M58WR032QT/B.

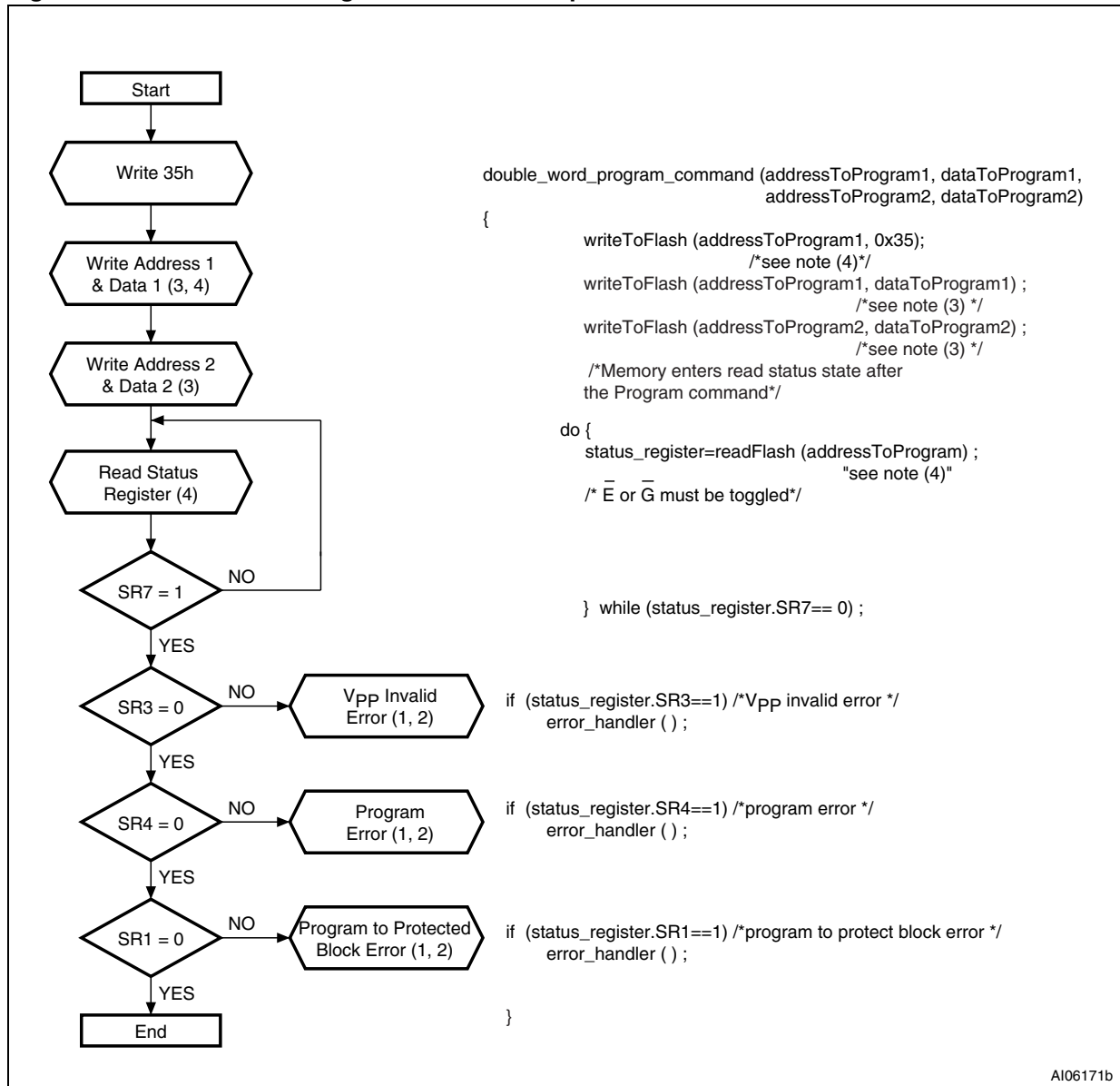
Appendix C Flowcharts and pseudo codes

Figure 20. Program flowchart and pseudo code



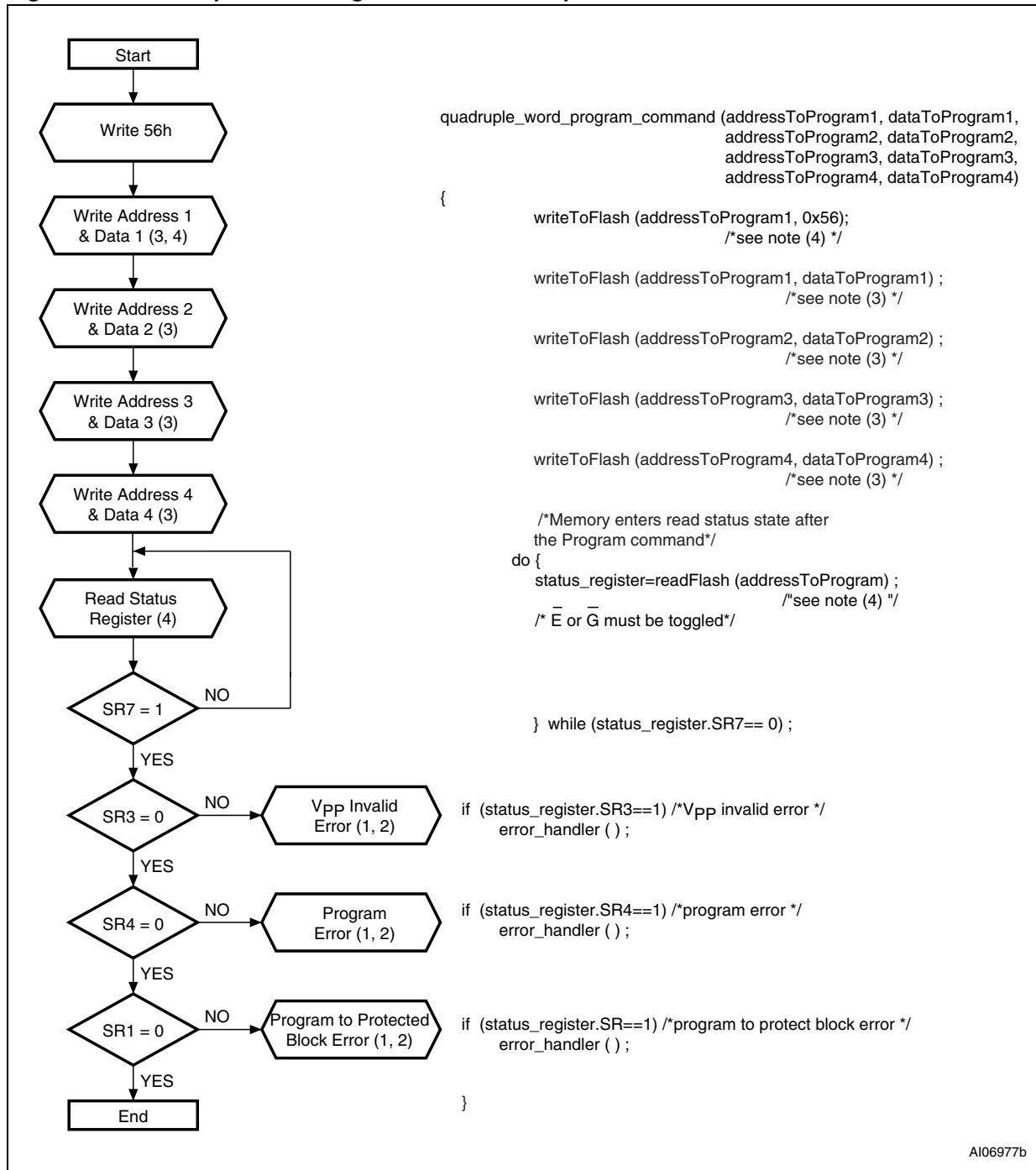
1. Status check of SR1 (Protected Block), SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Any address within the bank can equally be used.

Figure 21. Double Word Program flowchart and pseudo code



1. Status check of SR1 (Protected Block), SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.
4. Any address within the bank can equally be used.

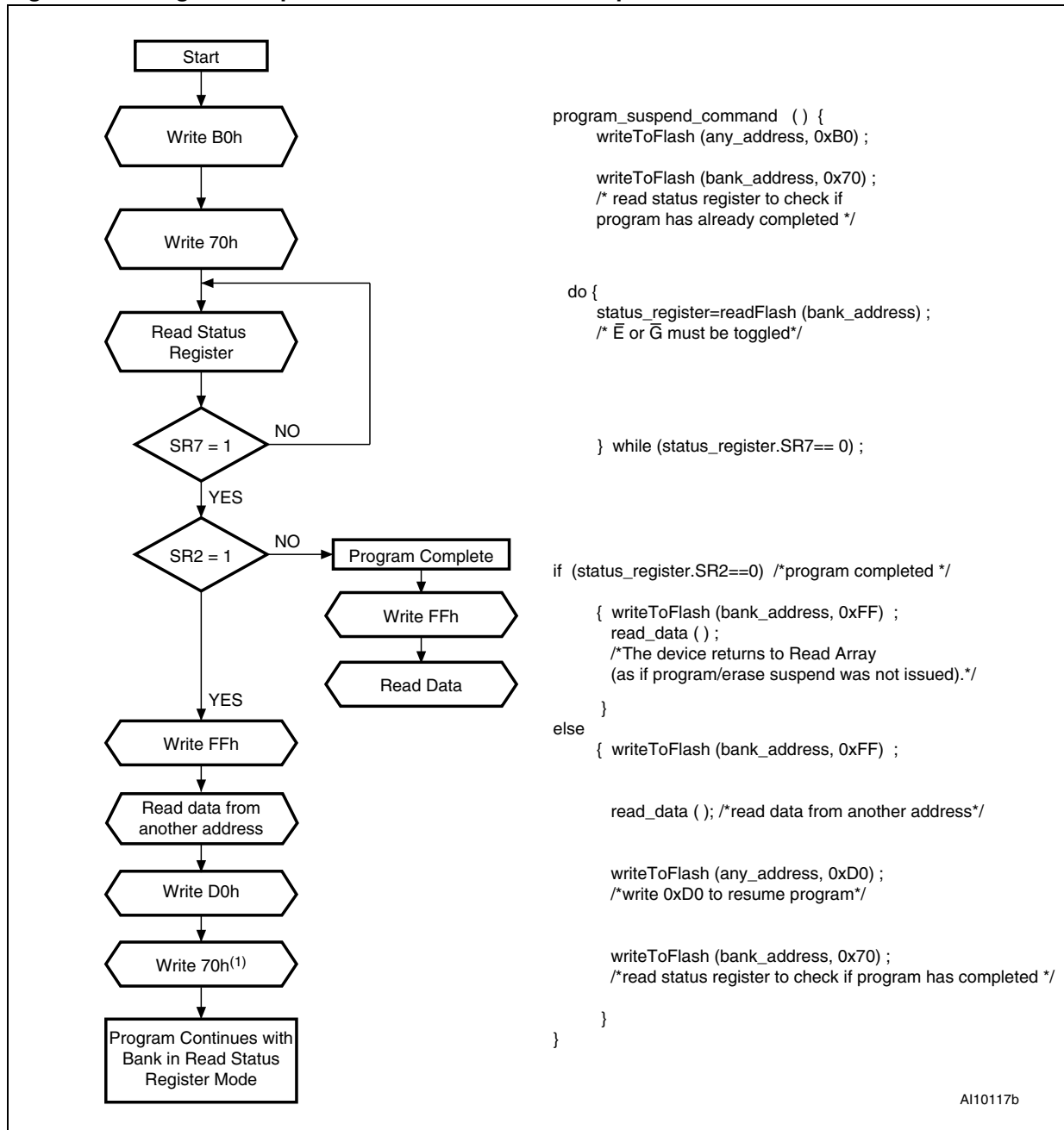
Figure 22. Quadruple Word Program flowchart and pseudo code



AI06977b

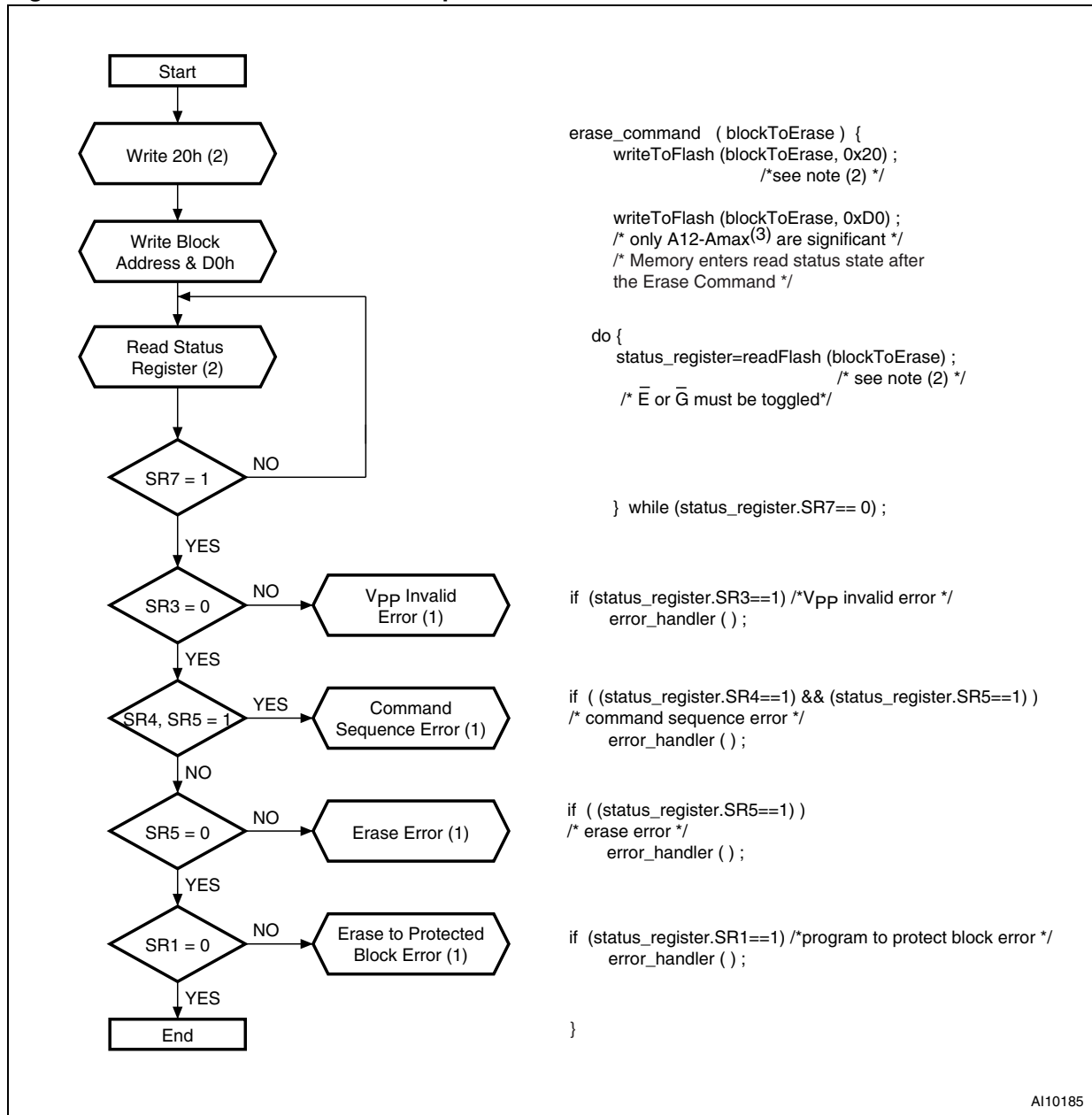
1. Status check of SR1 (Protected Block), SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 to Address 4 must be consecutive addresses differing only for bits A0 and A1.
4. Any address within the bank can equally be used.

Figure 23. Program Suspend & Resume flowchart and pseudo code



1. The Read Status Register command (Write 70h) can be issued just before or just after the Program Resume command.

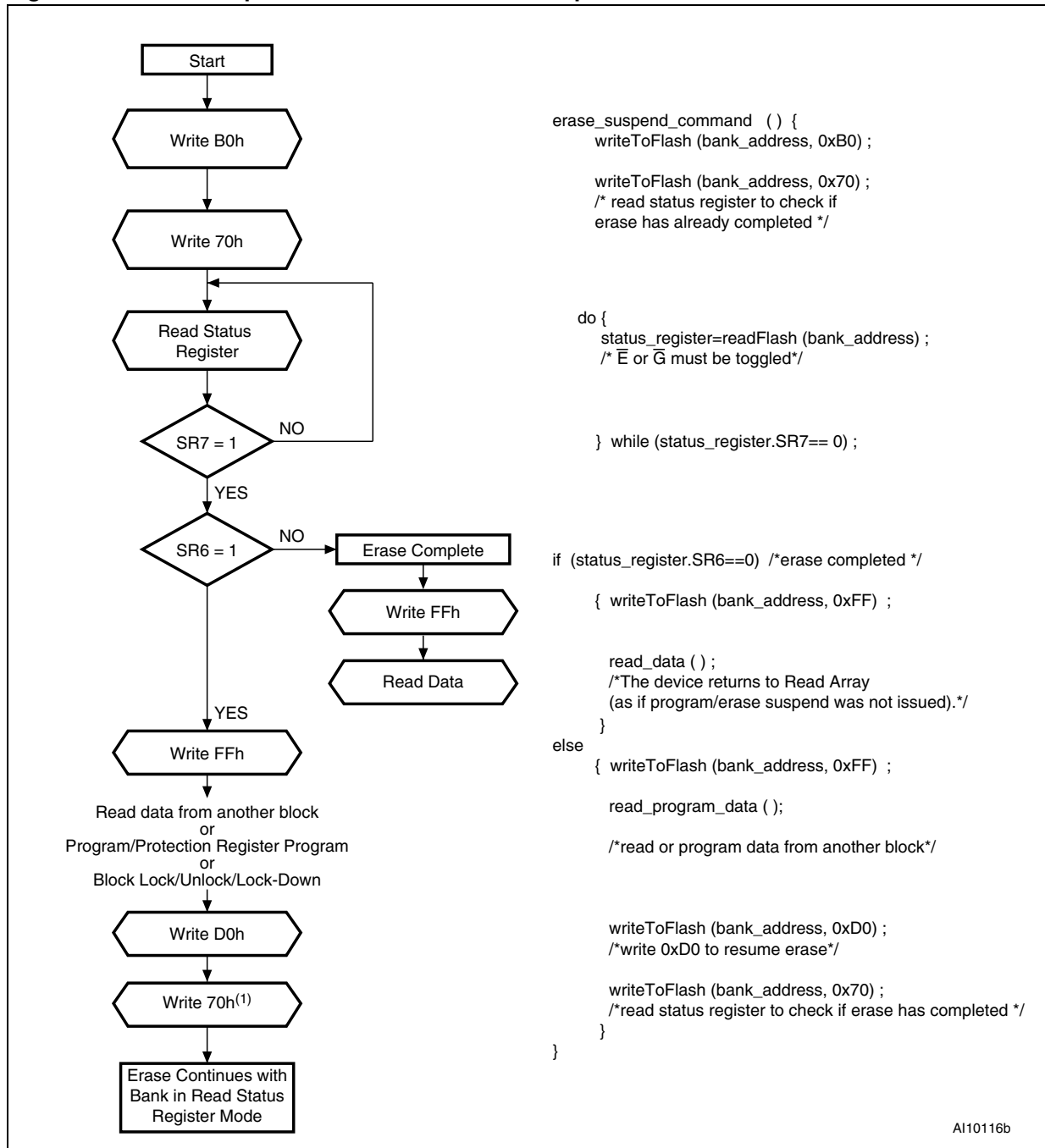
Figure 24. Block Erase flowchart and pseudo code



A110185

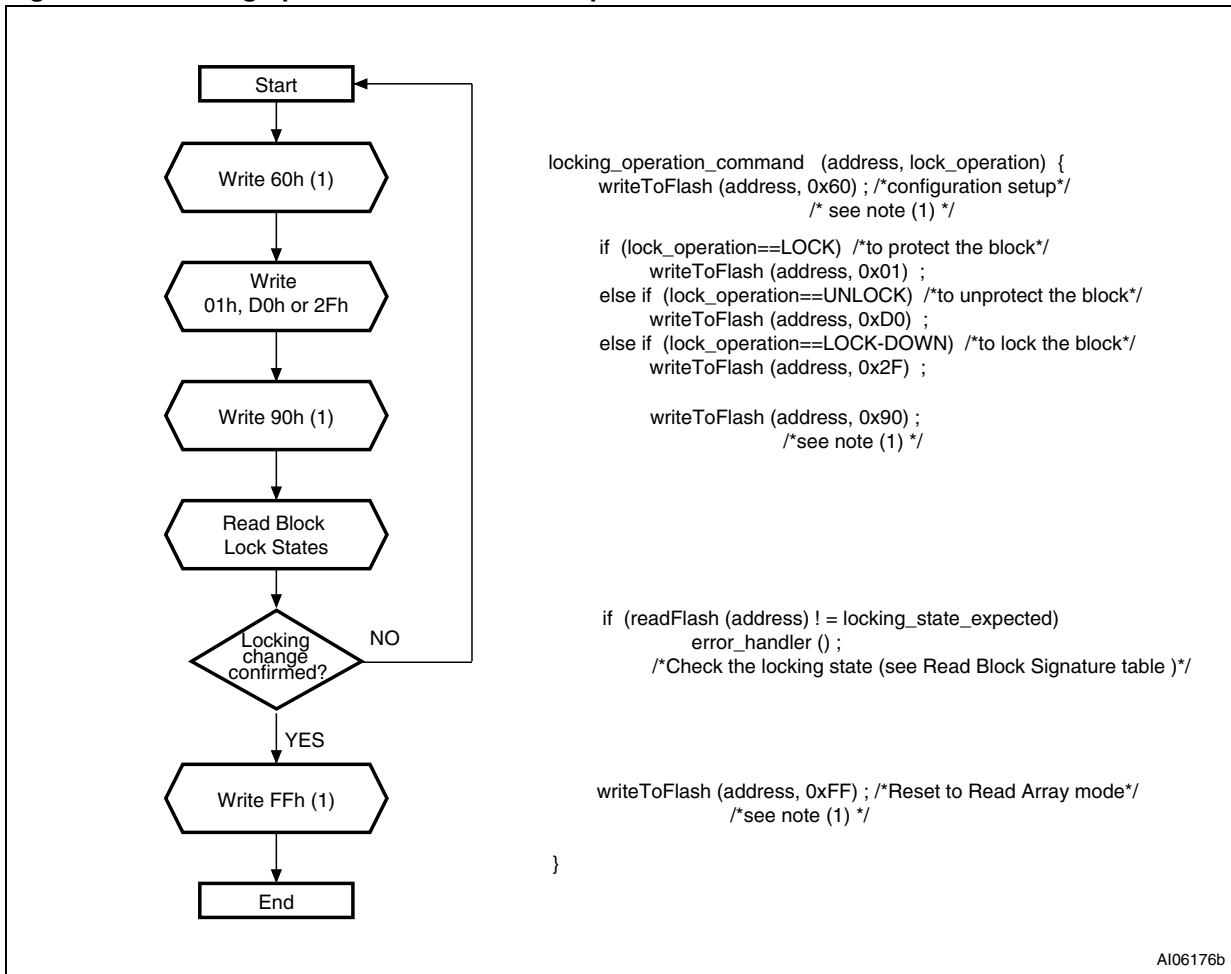
1. If an error is found, the Status Register must be cleared before further Program/Erase operations.
2. Any address within the bank can be used also.
3. Amax is equal to A19 in the M58WR016QT/B and to A20 in the M58WR032QT/B.

Figure 25. Erase Suspend & Resume flowchart and pseudo code



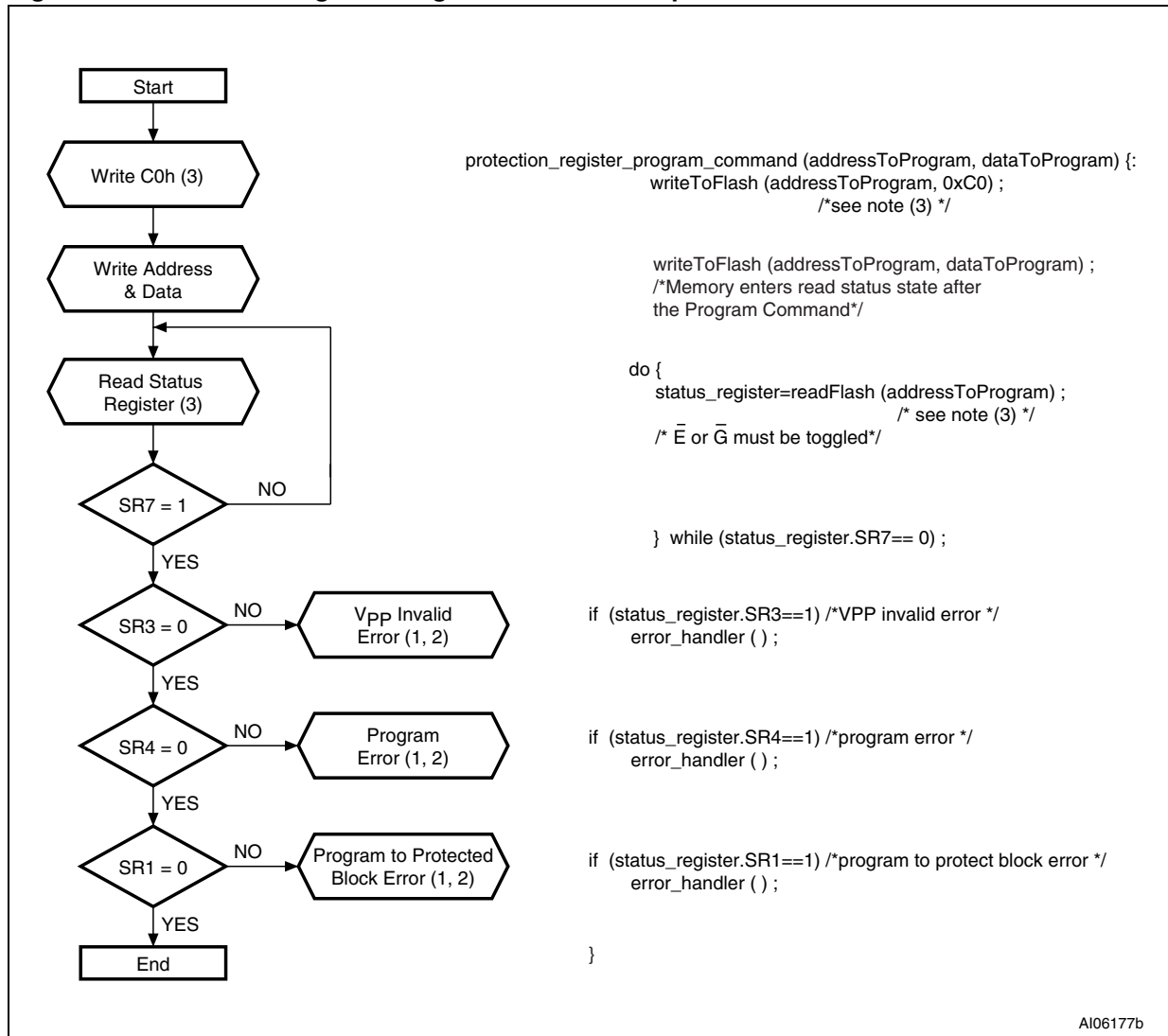
1. The Read Status Register command (Write 70h) can be issued just before or just after the Erase Resume command.

Figure 26. Locking operations flowchart and pseudo code



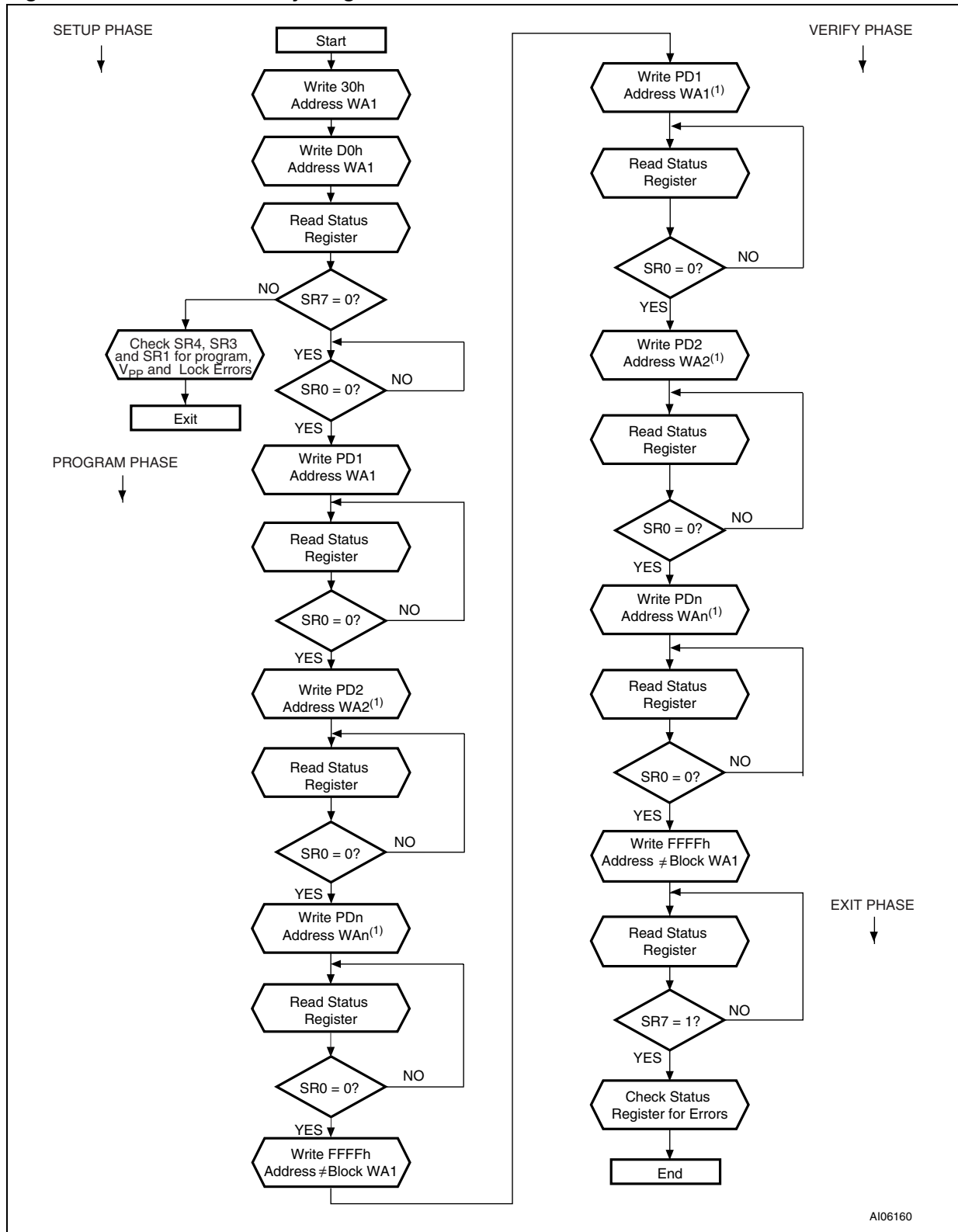
1. Any address within the bank can equally be used.

Figure 27. Protection Register Program flowchart and pseudo code



1. Status check of SR1 (Protected Block), SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Any address within the bank can equally be used.

Figure 28. Enhanced Factory Program flowchart



1. Address can remain Starting Address WA1 or be incremented.

C.1 Enhanced Factory Program pseudo code

```

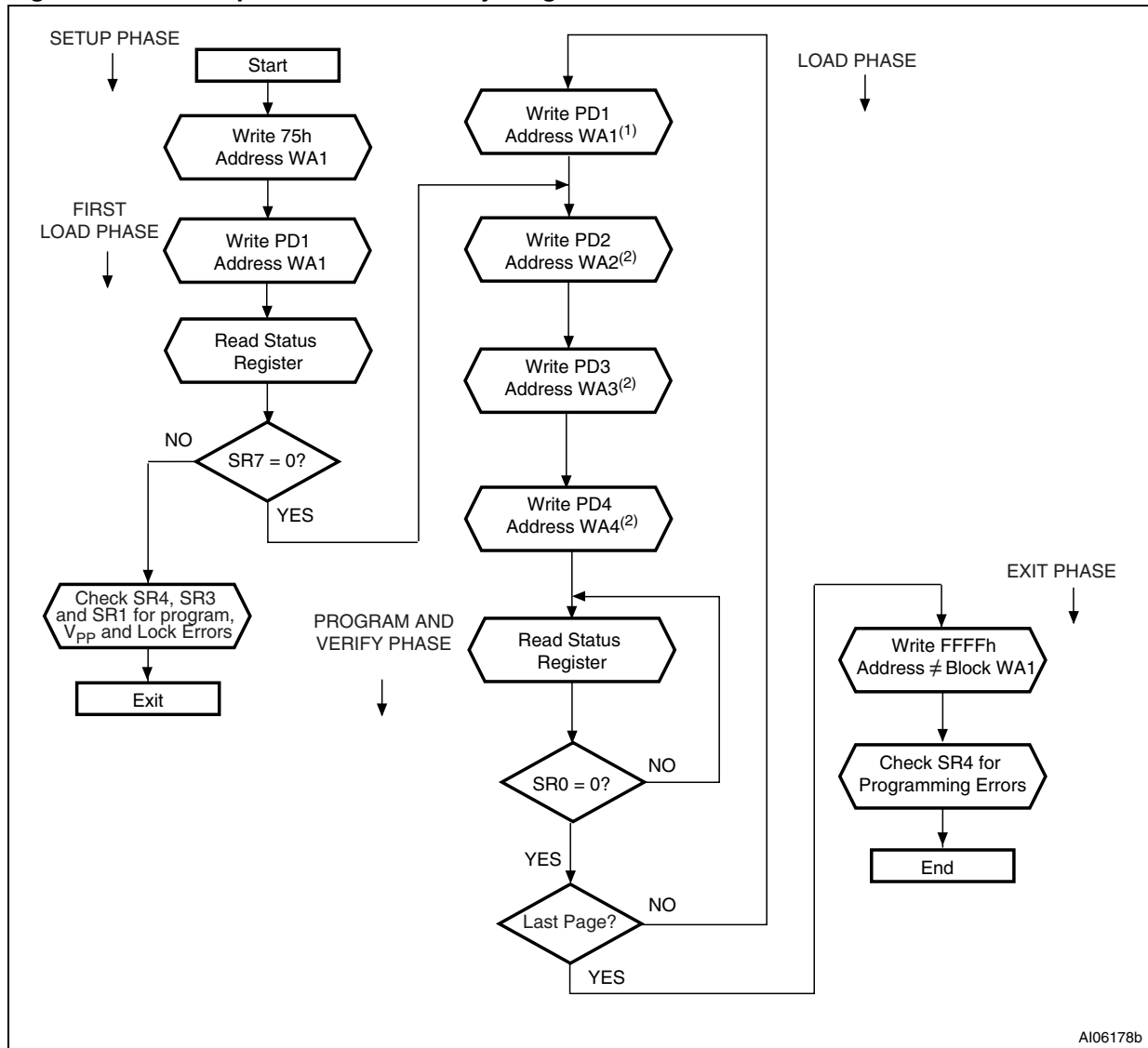
efp_command(addressFlow,dataFlow,n)
/* n is the number of data to be programmed */
{
    /* setup phase */
    writeToFlash(addressFlow[0],0x30);
    writeToFlash(addressFlow[0],0xD0);
    status_register=readFlash(any_address);
    if (status_register.SR7==1){
        /*EFP aborted for an error*/
        if (status_register.SR4==1) /*program error*/
            error_handler();
        if (status_register.SR3==1) /*VPP invalid error*/
            error_handler();
        if (status_register.SR1==1) /*program to protect block error*/
            error_handler();
    }
    else{
        /*Program Phase*/
        do{
            status_register=readFlash(any_address);
            /* E or G must be toggled*/
        } while (status_register.SR0==1)
        /*Ready for first data*/
        for (i=0; i++; i< n){
            writeToFlash(addressFlow[i],dataFlow[i]);
            /* status register polling*/
            do{
                status_register=readFlash(any_address);
                /* E or G must be toggled*/
            } while (status_register.SR0==1);
            /* Ready for a new data */
        }
        writeToFlash(another_block_address,FFFFh);

        /* Verify Phase */
        for (i=0; i++; i< n){
            writeToFlash(addressFlow[i],dataFlow[i]);
            /* status register polling*/
            do{
                status_register=readFlash(any_address);
                /* E or G must be toggled*/
            } while (status_register.SR0==1);
            /* Ready for a new data */
        }
        writeToFlash(another_block_address,FFFFh);
        /* exit program phase */

        /* Exit Phase */
        /* status register polling */
        do{
            status_register=readFlash(any_address);
            /* E or G must be toggled */
        } while (status_register.SR7==0);
        if (status_register.SR4==1) /*program failure error*/
            error_handler();
        if (status_register.SR3==1) /*VPP invalid error*/
            error_handler();
        if (status_register.SR1==1) /*program to protect block error*/
            error_handler();
    }
}

```

Figure 29. Quadruple Enhanced Factory Program flowchart



1. Address can remain Starting Address WA1 (in which case the next Page is programmed) or can be any address in the same block.
2. The address is only checked for the first Word of each Page as the order to program the Words is fixed, so subsequent Words in each Page can be written to any address.

C.2 Quadruple Enhanced Factory Program Pseudo Code

```

quad_efp_command(addressFlow,dataFlow,n)
/* n is the number of pages to be programmed.*/
{
    /* Setup phase */
    writeToFlash(addressFlow[0],0x75);
    for (i=0; i++; i< n){
        /*Data Load Phase*/

        /*First Data*/
        writeToFlash(addressFlow[i],dataFlow[i,0]);
        /*at the first data of the first page, Quad-EFP may be aborted*/
        if (First_Page) {
            status_register=readFlash(any_address);
            if (status_register.SR7==1){
                /*EFP aborted for an error*/
                if (status_register.SR4==1) /*program error*/
                    error_handler();
                if (status_register.SR3==1) /*VPP invalid error*/
                    error_handler();
                if (status_register.SR1==1) /*program to protect block
error*/
                    error_handler();
            }
        }
        /*2nd data*/
        writeToFlash(addressFlow[i],dataFlow[i,1]);

        /*3rd data*/
        writeToFlash(addressFlow[i],dataFlow[i,2]);

        /*4th data*/
        writeToFlash(addressFlow[i],dataFlow[i,3]);

        /* Program&Verify Phase */
        do{
            status_register=readFlash(any_address);
            /* E or G must be toggled*/
        }while (status_register.SR0==1)
    }
    /* Exit Phase */
    writeToFlash(another_block_address,FFFFh);
    /* status register polling */
    do{
        status_register=readFlash(any_address);
        /* E or G must be toggled */
    } while (status_register.SR7==0);
        if (status_register.SR1==1) /*program to protected block error*/
            error_handler();
        if (status_register.SR3==1) /*VPP invalid error*/
            error_handler();
        if (status_register.SR4==1) /*program failure error*/
            error_handler();
    }
}

```


Appendix D Command interface state tables

Table 43. Command interface states - modify table, next state⁽¹⁾

Current CI State	Command Input											
	Read Array ⁽²⁾ (FFh)	WP setup ⁽³⁾⁽⁴⁾ (10/40h)	DWP, QWP Setup ⁽³⁾⁽⁴⁾ (35h, 56h)	Block Erase, Bank Erase Setup ⁽³⁾⁽⁴⁾ (20h, 80h)	EFP Setup (30h)	Quad-EFP Setup (75h)	Erase Confirm P/E Resume, Block Unlock confirm, EFP Confirm (D0h)	Program/Erase Suspend (B0h)	Read Status Register (70h)	Clear Status Register ⁽⁵⁾ (50h)	Read Electronic signature, Read CFI Query (90h, 98h)	
Ready	Ready	Program Setup	Program Setup	Erase Setup	EFP Setup	Quad-EFP Setup	Ready					
Lock/CR Setup	Ready (Lock Error)					Ready	Ready (Lock Error)					
OTP	Setup	OTP Busy										
	Busy	OTP Busy										
Program	Setup	Program Busy										
	Busy	Program Busy						Program Suspended	Program Busy			
	Suspend	Program Suspended				Program Busy		Program Suspended				
Erase	Setup	Ready (error)				Erase Busy		Ready (error)				
	Busy	Erase Busy						Erase Suspended	Erase Busy			
	Suspend	Erase Suspended	Program in Erase Suspend	Erase Suspended			Erase Busy		Erase Suspended			
Program in Erase Suspend	Setup	Program Busy in Erase Suspend										
	Busy	Program Busy in Erase Suspend						Program Suspend in Erase Suspend	Program Busy in Erase Suspend			
	Suspend	Program Suspend in Erase Suspend				Program Busy in Erase Suspend		Program Suspend in Erase Suspend				
Lock/CR Setup in Erase Suspend	Erase Suspend (Lock Error)					Erase Suspend		Erase Suspend (Lock Error)				
EFP	Setup	Ready (error)				EFP Busy		Ready (error)				
	Busy	EFP Busy ⁽⁶⁾										
	Verify	EFP Verify ⁽⁶⁾										
Quad EFP	Setup	Quad EFP Busy ⁽⁶⁾										
	Busy	Quad EFP Busy ⁽⁶⁾										

1. CI = Command Interface, CR = Configuration Register, EFP = Enhanced Factory Program, Quad EFP = Quadruple Enhanced Factory Program, DWP = Double Word Program, QWP = Quadruple Word Program, P/E. C. = Program/Erase Controller.
2. At Power-Up, all banks are in Read Array mode. A Read Array command issued to a busy bank, results in undetermined data output.
3. The two cycle command should be issued to the same bank address.
4. If the P/E.C. is active, both cycles are ignored.
5. The Clear Status Register command clears the Status Register error bits except when the P/E.C. is busy or suspended.
6. EFP and Quad EFP are allowed only when Status Register bit SR0 is set to '0'.EFP and Quad EFP are busy if Block Address is first EFP Address. Any other commands are treated as data.

Table 44. Command interface states - modify table, next output state

Current CI State	Command Input ⁽¹⁾ ⁽²⁾										
	Read Array ⁽³⁾ (FFh)	WP Setup ⁽⁴⁾ ⁽⁵⁾ (10/40h)	DWP, QWP Setup ⁽⁴⁾ ⁽⁵⁾ (35h, 56h)	Block Erase, Bank Erase Setup ⁽⁴⁾ ⁽⁵⁾ (20h, 80h)	EFP Setup (30h)	Quad-EFP Setup (75h)	Erase Confirm P/E Resume, Block Unlock confirm, EFP Confirm (D0h)	Program/ Erase Suspend (B0h)	Read Status Register (70h)	Clear status Register ⁽⁶⁾ (50h)	Read Electronic signature, Read CFI Query (90h, 98h)
Program Setup	Status Register										
Erase Setup											
OTP Setup											
Program in Erase Suspend											
EFP Setup											
EFP Busy											
EFP Verify											
Quad EFP Setup											
Quad EFP Busy											
Lock/CR Setup											
Lock/CR Setup in Erase Suspend											
OTP Busy											
Ready										Electronic Signature/CFI	
Program Busy											
Erase Busy											
Program/Eraser											
Program Busy in Erase Suspend											
Program Suspend in Erase Suspend											

1. CI = Command Interface, CR = Configuration Register, EFP = Enhanced Factory Program, Quad EFP = Quadruple Enhanced Factory Program, DWP = Double Word Program, QWP = Quadruple Word Program, P/E. C. = Program/Eraser Controller.
2. The output state shows the type of data that appears at the outputs if the bank address is the same as the command address. A bank can be placed in Read Array, Read Status Register, Read Electronic Signature or Read CFI Query mode, depending on the command issued. Each bank remains in its last output state until a new command is issued. The next state does not depend on the bank's output state.
3. At Power-Up, all banks are in Read Array mode. A Read Array command issued to a busy bank, results in undetermined data output.
4. The two cycle command should be issued to the same bank address.
5. If the P/E.C. is active, both cycles are ignored.
6. The Clear Status Register command clears the Status Register error bits except when the P/E.C. is busy or suspended.

Table 45. Command interface states - lock table, next state

Current CI State		Command Input ⁽¹⁾							P/E. C. Operation Completed
		Lock/CR Setup ⁽²⁾ (60h)	OTP Setup ⁽²⁾ (C0h)	Block Lock Confirm (01h)	Block Lock-Down Confirm (2Fh)	Set CR Confirm (03h)	EFP Exit, Quad EFP Exit ⁽³⁾	Illegal Command ⁽⁴⁾	
Ready		Lock/CR Setup	OTP Setup	Ready					N/A
Lock/CR Setup		Ready (Lock error)		Ready			Ready (Lock error)		N/A
OTP	Setup	OTP Busy							N/A
	Busy								Ready
Program	Setup	Program Busy							N/A
	Busy	Program Busy							Ready
	Suspend	Program Suspended							N/A
Erase	Setup	Ready (error)							N/A
	Busy	Erase Busy							Ready
	Suspend	Lock/CR Setup in Erase Suspend	Erase Suspended						N/A
Program in Erase Suspend	Setup	Program Busy in Erase Suspend							N/A
	Busy	Program Busy in Erase Suspend							Erase Suspended
	Suspend	Program Suspend in Erase Suspend							N/A
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock error)		Erase Suspend			Erase Suspend (Lock error)		N/A
EFP	Setup	Ready (error)							N/A
	Busy	EFP Busy ⁽⁵⁾				EFP Verify		EFP Busy ⁽⁵⁾	N/A
	Verify	EFP Verify ⁽⁵⁾				Ready		EFP Verify ⁽⁵⁾	Ready
QuadEFP	Setup	Quad EFP Busy ⁽⁵⁾							N/A
	Busy	Quad EFP Busy ⁽⁵⁾				Ready		Quad EFP Busy ⁽⁵⁾	Ready

1. CI = Command Interface, CR = Configuration Register, EFP = Enhanced Factory Program, Quad EFP = Quadruple Enhanced Factory Program, P/E. C. = Program/Erase Controller.
2. If the P/E.C. is active, both cycles are ignored.
3. EFP and Quad EFP exit when Block Address is different from first Block Address and data is FFFFh.
4. Illegal commands are those not defined in the command set.
5. EFP and Quad EFP are allowed only when Status Register bit SR0 is set to '0'. EFP and Quad EFP are busy if Block Address is first EFP Address. Any other commands are treated as data.

Table 46. Command interface states - lock table, next output state

Current CI State	Command Input ⁽¹⁾							
	Lock/CR Setup ⁽²⁾ (60h)	OTP Setup ⁽²⁾ (C0h)	Block Lock Confirm (01h)	Block Lock-Down Confirm (2Fh)	Set CR Confirm (03h)	EFP Exit, Quad EFP Exit ⁽³⁾	Illegal Command ⁽⁴⁾	P/E. C. Operation Completed
Program Setup	Status Register							Output Unchanged
Erase Setup								
OTP Setup								
Program in Erase Suspend								
EFP Setup								
EFP Busy								
EFP Verify								
Quad EFP Setup								
Quad EFP Busy								
Lock/CR Setup	Status Register			Array	Status Register		Output Unchanged	
Lock/CR Setup in Erase Suspend								
OTP Busy	Status Register	Output Unchanged			Array	Output Unchanged	Output Unchanged	
Ready	Status Register							Output Unchanged
Program Busy								
EraseBusy								
Program/Erase								
Program Busy in Erase Suspend								
Program Suspend in Erase Suspend								

1. CI = Command Interface, CR = Configuration Register, EFP = Enhanced Factory Program, Quad EFP = Quadruple Enhanced Factory Program, P/E. C. = Program/Erase Controller.
2. If the P/E.C. is active, both cycles are ignored.
3. EFP and Quad EFP exit when Block Address is different from first Block Address and data is FFFFh.
4. Illegal commands are those not defined in the command set.

17 Revision history

Table 47. Document revision history

Date	Revision	Changes
15-Sep-2004	0.1	First Issue
14-Apr-2006	1	<p>Document status promoted from Target Specification to full Datasheet.</p> <p>Small text changes. Address modified for Clear Status Register command in Table 6: Standard commands.</p> <p>Test condition modified for I_{DD3} and I_{DD7} in Table 19: DC characteristics - currents. V_{PP1} min modified and V_{LKO} value moved from Min to Max in Table 20: DC characteristics - voltages.</p> <p>t_{WHQV} removed from Figure 16, Table 23, Figure 17 and Table 24. Note 3 modified. Data modified at address offset 31h in Table 36. Figure 23: Program Suspend & Resume flowchart and pseudo code and Figure 25: Erase Suspend & Resume flowchart and pseudo code modified.</p>
12-Nov-2007	2	Applied Numonyx branding.

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