Ordering number : EN8214

SANYO

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA5683T — 4ch Switching Regulator Control IC

Overview

The LA5683T is 4ch switching regulator control IC.

Functions

- Low-voltage operation (minimum 1.8V).
- OUT1 and OUT2 can drive external PNP transistors.
- OUT3 and OUT4 can drive external NPN transistors.
- 4-independent-channel standby circuit built-in.
- ±1% accuracy reference voltage.
- Supports MOS transistor drive.
- Channel 2 dead time internally set fixed, duty cycle = 100%. (The dead time for channels 1, 3, and 4 are set externally.)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max		9	V
Allowable power dissipation	Pd max	Independent IC	0.4	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}		1.8 to 8	V
Supply voltage 2	V_{BIAS}		1.8 to 8	V
Output sync current	I_{SINK} max		0 to 30	mA
Reference voltage output current	I_{REF}		0 to 1	mA
Timing resistor	RT		3 to 30	kΩ
Timing capacity	CT		100 to 1000	pF
Triangular wave frequency	f_{OSC}		0.1 to 1	MHz

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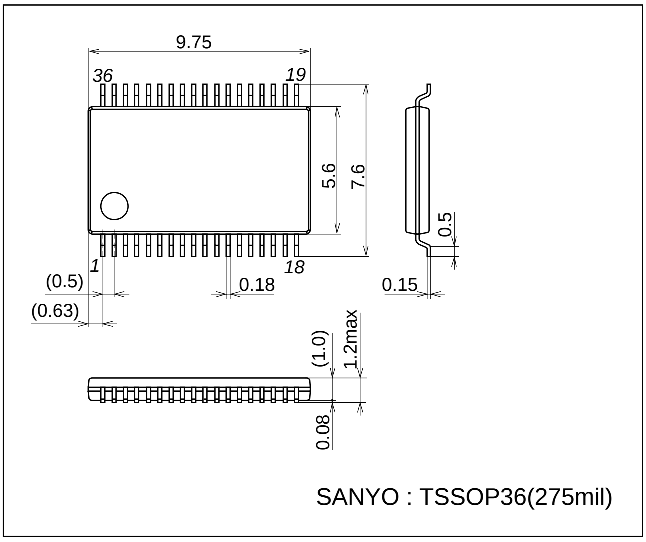
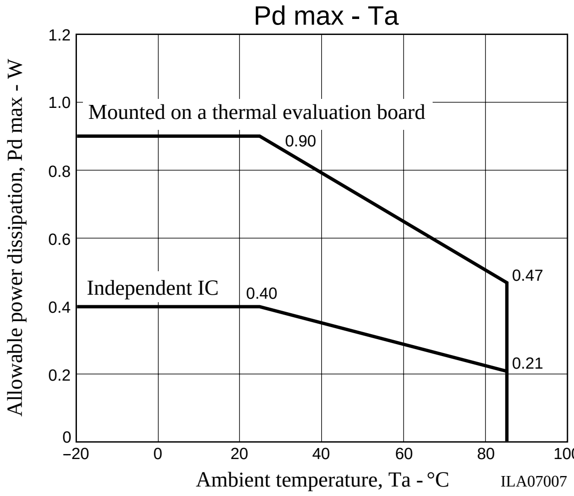
Electrical Characteristics at Ta = 25°C, V_{CC} = VSTBY1 to 4 = 3V, SCP = 0V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
[Error amplifier]							
IN+ pin internal bias voltage		VB	Pins IN1+, IN2+, IN3+, and IN4+	0.500	0.506	0.512	V
Output L level voltage	CH1 to CH4	V_{Low}_FB1	IN1– = 2.0 IFB1 = 20μA			1	V
Output H level voltage	CH1 to CH4	V_{Hi} _FB1	IN1– = 0V IFB1 = -20μA	2.25			V
[Protection circuit]							
Threshold voltage		V_{SCP}		1.1	1.25	1.4	V
SCP pin current		I_{SCP}			3.9		μA
[Idle period adjustment block]							
Input bias current		I_B_DTC		-15	-3		μA
Threshold voltage 1	CH1	VTH1_DTC	IN1– = 0V, duty cycle = 100%	0.67	0.77	0.87	V
Threshold voltage 2	CH1	VTH2_DTC	IN1– = 0V, duty cycle = 0%	0.35	0.4	0.45	V
Threshold voltage 3	CH3 to CH4	VTH3_DTC	IN3, IN4– = 0V, duty cycle = 100%	0.72	0.8	0.88	V
Threshold voltage 4	CH3 to CH4	VTH4_DTC	IN3, IN4– = 0V, duty cycle = 0%	0.4	0.45	0.5	V
[Software start block (CH1 to CH4)]							
Software start current	CH1 to CH4	I_{SF}	CSOFT = 0V	3.16	3.95	4.74	μA
Software start resistance	CH1 to CH4	R_{SF}		160	200	240	kΩ
[Output blocks 1 and 2 (CH1 and CH2)]							
OUT pin source current		I_{OUT}12_SOUR	IN1, 2– = 0V DTC1 = 0V V_{OUT}1, 2 = 2.7V ICAPH = 0.5mA	10			mA
OUT pin sink current		I_{OUT}12_SINK	IN1, 2– = 0V DTC1 = 1.0V V_{OUT}1, 2 = 2.3V	35	45	55	mA
[Output blocks and 4 (CH3 and CH4)]							
OUT pin source current		I_{OUT}34_SOUR	V_{OUT}3, 4 = 0.9V DTC3, 4 = 1.0V IN3, 4 = 0V	20	30	40	mA
OUT pin sink current		I_{OUT}34_SINK	V_{OUT}3, 4 = 0.3V DTC3, 4 = 1.0V IN3, 4 = 1.0V	30			mA
OUT pin high level voltage		V_{OUT}34_Hi	I_{OUT}3, 4 = -10mA DTC3, 4 = 1.0V IN3, 4 = 0V	2			V
OUT pin low level voltage		V_{OUT}34_Low	I_{OUT}3, 4 = 10mA DTC3, 4 = 0V IN3, 4 = 1.0V			0.2	V
[Triangular wave form generator block]							
Current setting pin voltage		VT_RT	RT = 5.6kΩ	1.190	1.260	1.330	V
Output current		I_{OH}_CT	VCT = 0.5V, RT = 5.6kΩ		230		μA
Output current ratio		ΔI_O_CT		0.8	1.0	1.2	
Oscillation frequency		f_{OSC}1		380	440	500	kHz
[Reference voltage block]							
Reference voltage		VREF	I_{REF} = -1mA	1.244	1.257	1.270	V
Line regulation		V_{LN}_REF	V_{CC} = 1.8V to 8V			10	mV
Load regulation		V_{LD}_REF	I_{REF} = -0.1mA to -1mA			10	mV
[STBY circuit]							
On voltage		V_{ON}_STBY		1.15			V
Off voltage		V_{OFF}_STBY				0.2	V
Pin input current		I_{IN}_STBY	VSTBY1 to 4 = 3V			70	μA
[All circuits]							
Operating-time current drain		I_{CC}1	FB1, 2, 3, 4 = 1.5V DTC1, 3, 4 = 1.5V		15	18	mA
Standby-time current drain		I_{CC}2	VSTBY1 to 3 = 0V			1	μA

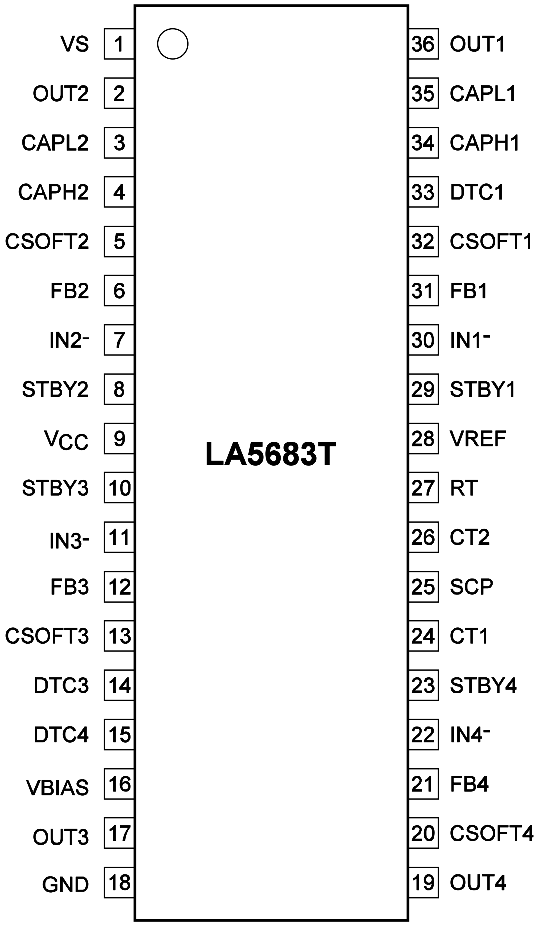
Package Dimensions

unit : mm
3253B





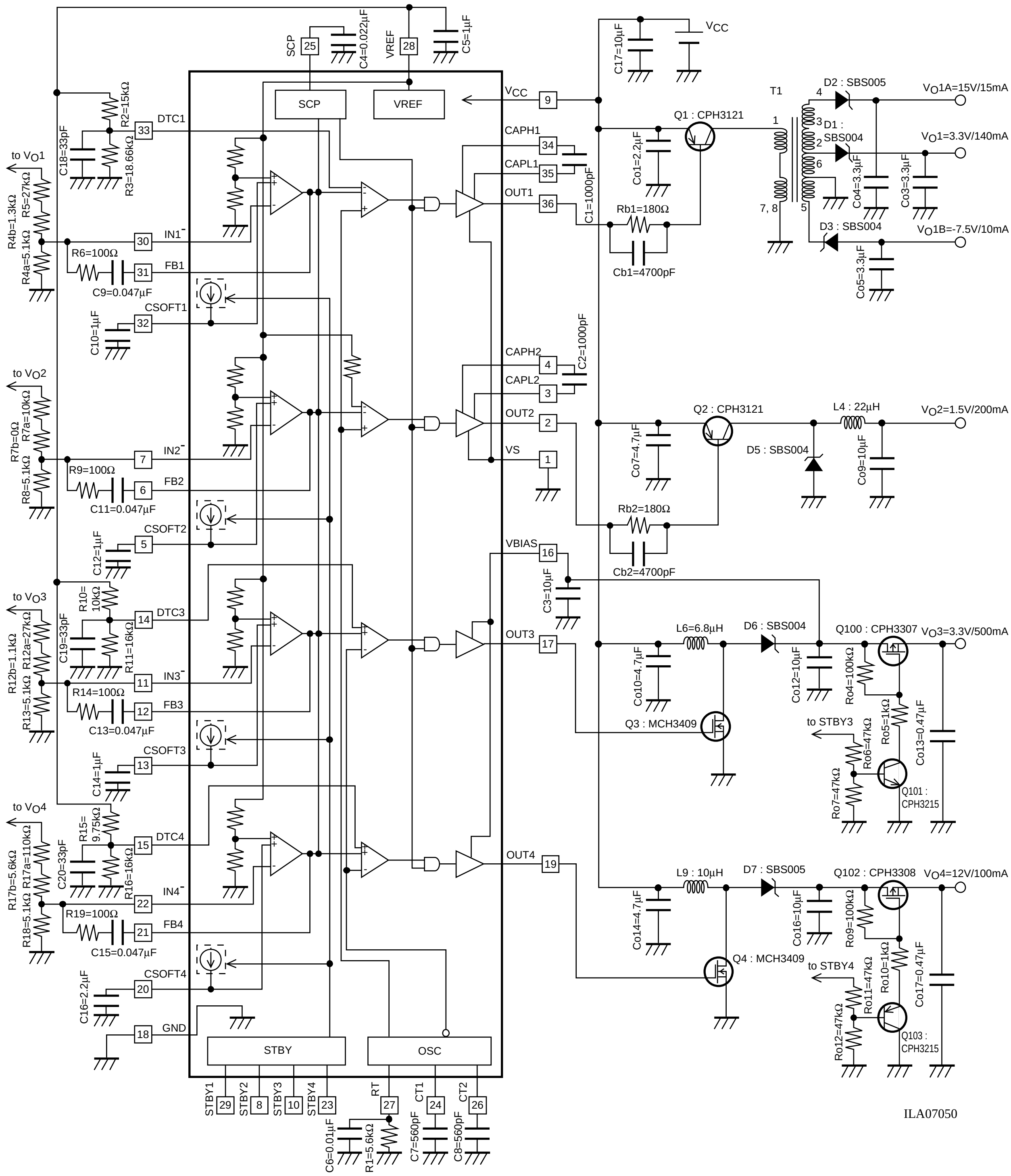
Pin Assignment



Top view

Block Diagram and Application Circuit Examples 1

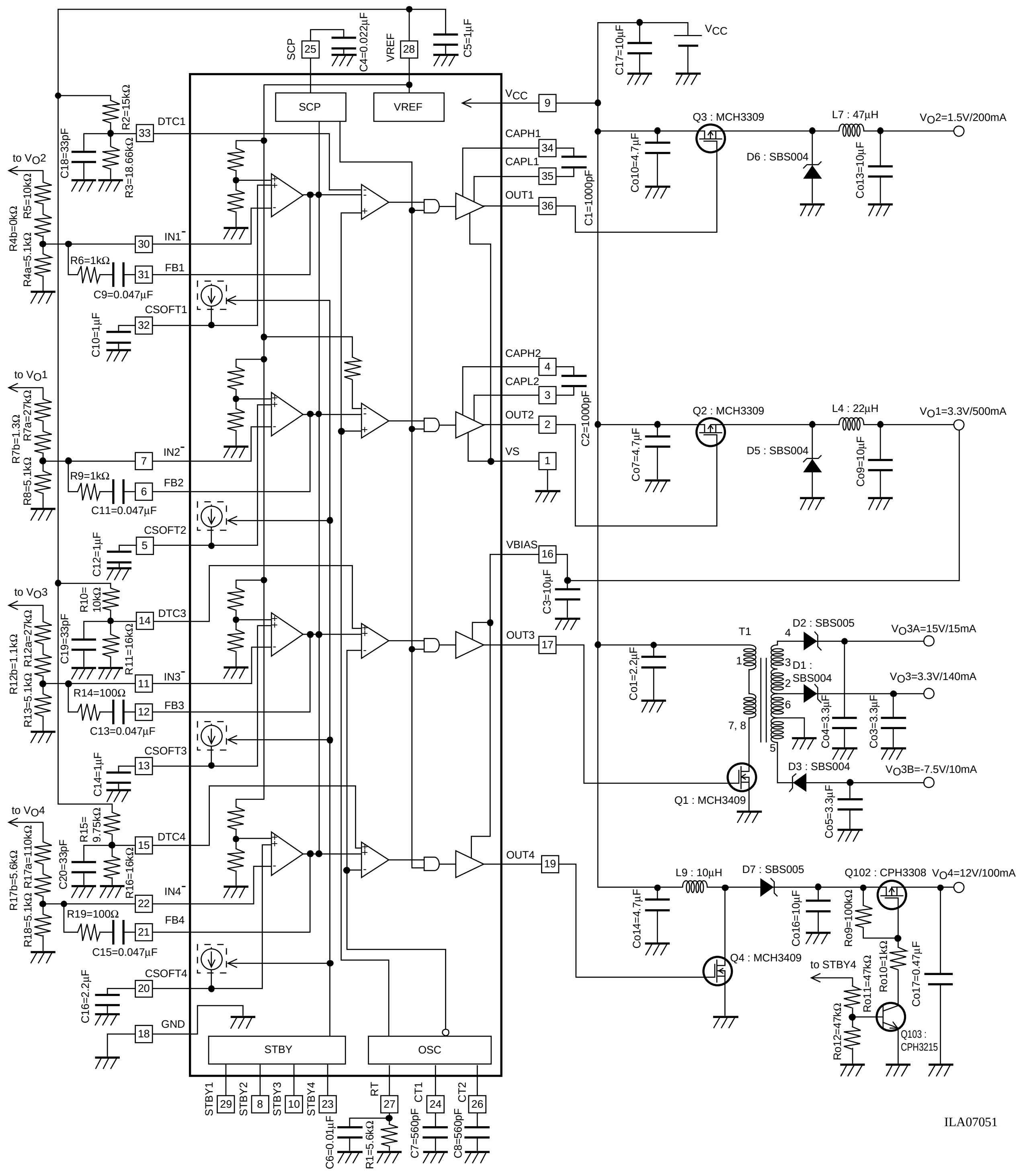
2-dry-battery (1.8V to 3.2V) configuration



T1 = Sumida product
L4 = TDK product: RLF5018-220MR63
L6 = TDK product: SLF6028-6R8M1R5
L9 = Toko product: 636CY-100M

Application Circuit Examples 2

4-dry battery (3.5V to 6.5V) configuration



T1 = Sumida product

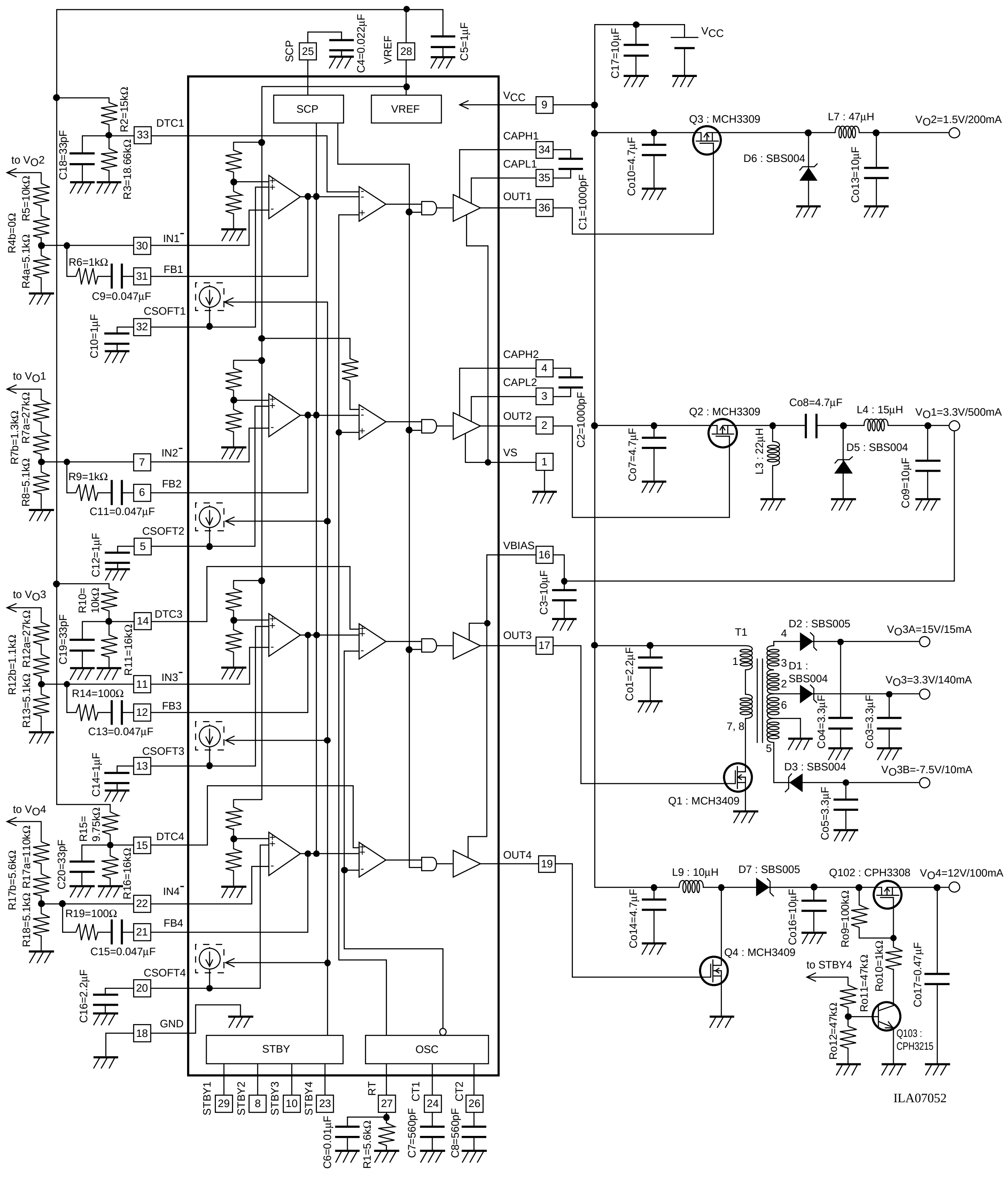
L4 = TDK product: RLF5018-220MR63

L7 = Toko product: 636CY-470M

L9 = Toko product: 636CY-100M

Application Circuit Examples 3

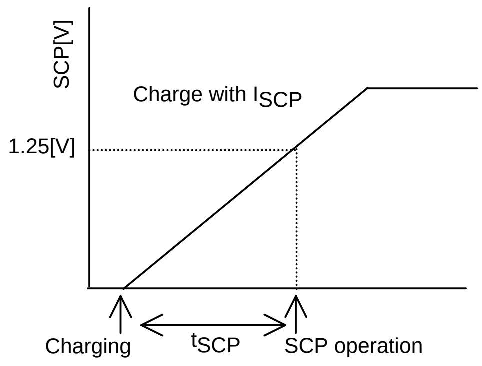
1-lithium ion battery (2.5V to 4.2V) configuration



T1 = Sumida product
L3 = TDK product: RLF5018-220MR63
L4 = TDK product: RLF5018-150MR63
L7 = Toko product: 636CY-470M
L9 = Toko product: 636CY-100M

SCP Pin

Charging of the SCP block starts when FB1 to FB4 are set to a low level due to a load shorting and the protection circuit is activated if the block does not reset itself within the preset time t_{SCP} (the protection circuit then turns off the whole OUT channels).

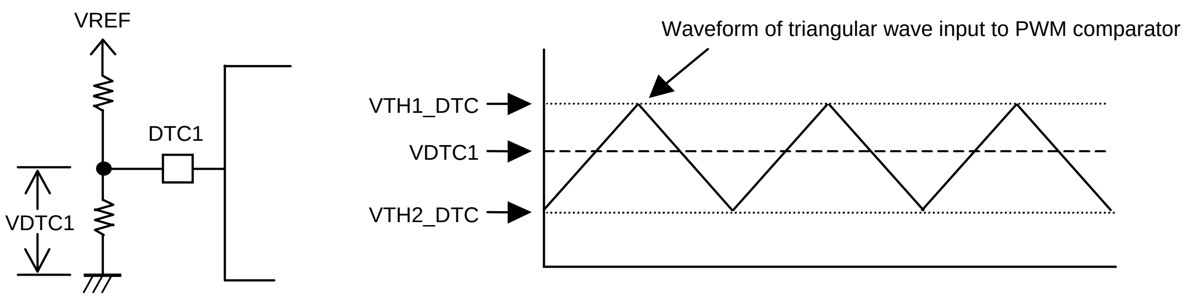


SCP Charging

$$t_{SCP} = \frac{C_{SCP} \times V_{SCP}}{I_{SCP}} \quad [S]$$

Dead Time Setup

• The dead time of channel 1 can be set by the voltage at DTC1.



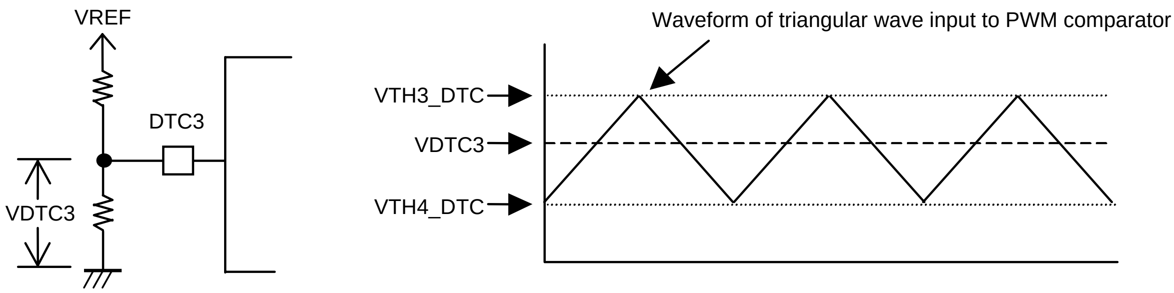
The duty cycle D1 is calculated as follows:

$$D1 = \frac{VDTC1 - VTH2\_DTC}{VTH1\_DTC - VTH2\_DTC} \times 100[\%]$$

• Channel 2

The dead time of channe 2 is fixed internally and the setting duty is 100%.

• Channel 3
The dead time of channel 3 can be set by the voltage at DTC3.



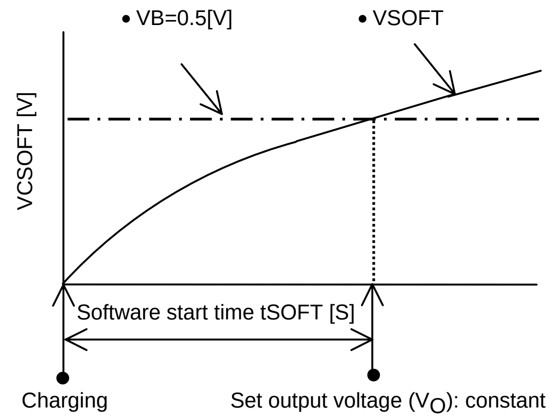
The duty cycle D3 is calculated as follows:

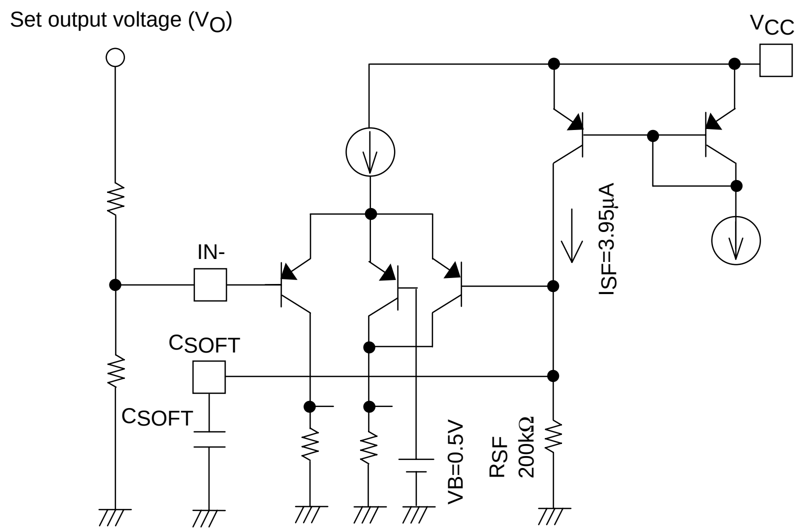
$$D3 = \frac{VDTC3 - VTH4\_DTC}{VTH3\_DTC - VTH4\_DTC} \times 100[\%]$$

• Channel 4
The dead time of channel 4 can be set in the same manner as that of channel 3.

Procedure for Setting the Software Start Time

- Channel 1 (the procedure is the same for channels 2, 3, and 4.)
  The software start time of channel 1 is set by the capacitance of the capacitor connected between pin CSOFT1 to CSOFT4 and GND.





$$t_{SOFT} = -C_{SOFT} \times R_{SF} 1n(1 - \frac{VB}{R_{SF} \times I_{SF}}) [S]$$

* The formula is for channel 1.
The software start time for channels 2 to 4 can be calculated in the same manner.

CT1 and CT2

The waveform of CT1 is 180 degrees out of phase with that of CT2. Their frequency cannot be set independently.
The capacitance of the capacitors to be connected to pins CT1 and CT2 must be the same.

- Setting the oscillation frequency
  (1) The oscillation frequency of the oscillator can be set by selecting the capacitance of the capacitors connected to pins CT1 and CT2 (see Figure 1).
  (2) The oscillation frequency can also be determined by the resistance of the resistor connected to the RT pin (see Figure 2).

Figure 1 Oscillation Frequency vs. Timing Capacitance Characteristics

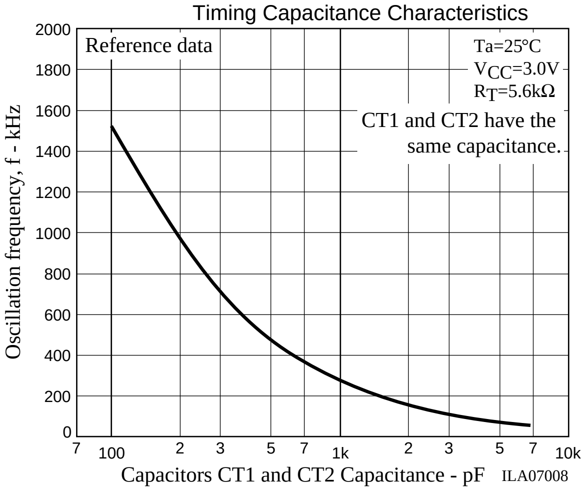
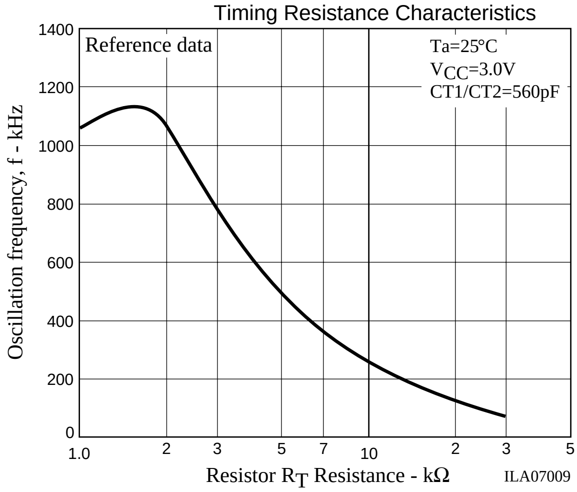
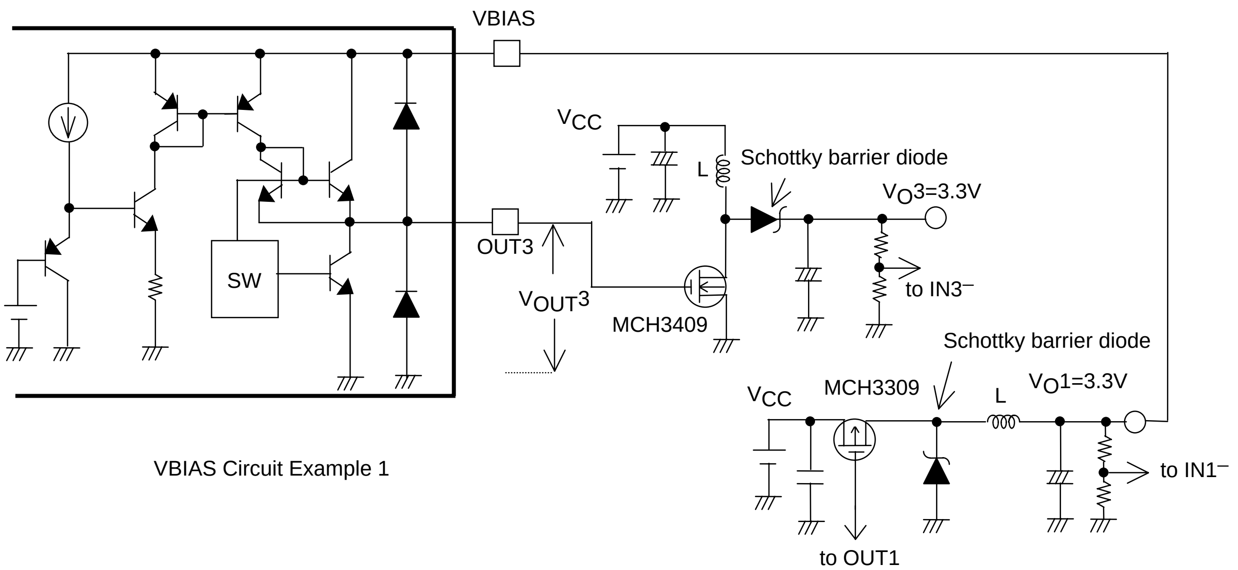


Figure 2 Oscillation Frequency vs. Timing Resistance Characteristics



Sample Circuits

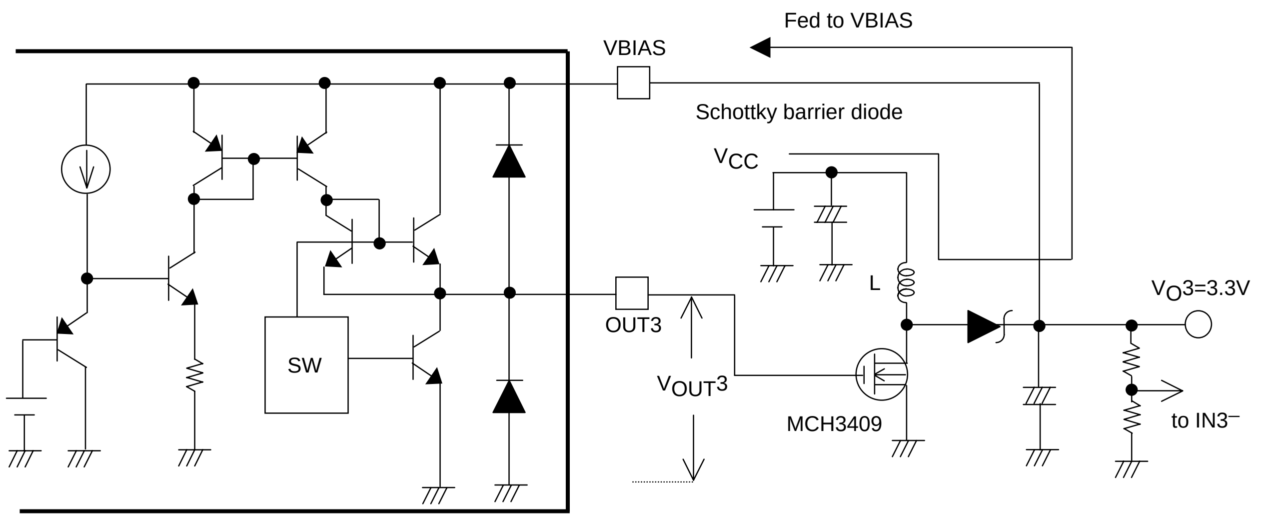
Sample Circuit That Makes Use of VBIAS (1)
This IC can be used to implement the circuit that is shown below since the power to the channels 3 and 4 output stages is supplied via VBIAS.
Apply V_O1 that is dropped to 3.3V in channel 1 to VBIAS. A voltage of approx. VBIAS3-1 volt develops at $V_{OUT}3$, so that the IC can drive MOS transistors in a low-voltage environment like this sample circuit.



VBIAS Circuit Example 1

Sample Circuit That Makes Use of VBIAS (2)

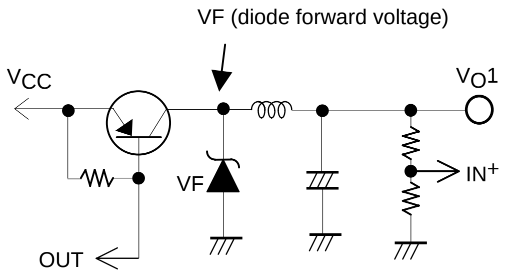
This IC can be used to implement the circuit that is shown below since the power to the channels 3 and 4 output stages is supplied via VBIAS.
Apply the power voltage to VBIAS through the path that is made up of V_{CC}, L to Schottky diode (through path formation).
Then feed the stabilized voltage V_O3 that is raised to 3.3V in channel 3 to VBIAS.
A voltage of approx. VBIAS3-1 volt develops at $V_{OUT}3$, so that the IC can drive MOS transistors in a low-voltage environment like this sample circuit.

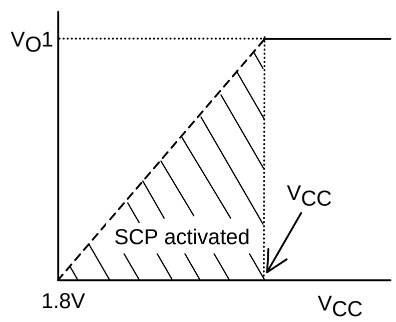


VBIAS Circuit Example 2

Using the IC in a Step-down Circuit (CH1 and CH2)

The IC detects a short-circuit condition and activates the SCP when V_{CC} falls below the preset voltage V_O+VF in such a step-down application as the one shown below.





When stepping down V_{CC}<V0+VF

Using the IC in a Step-up Circuit (CH3 and CH4)

In a step-up application like the one shown below, a through path consisting of V_{CC}, L, and D is formed when STBY is set off and a voltage normally remains present at V_O.

* Although the STBY off-time through path in the application circuit example is cut by a MOSFET, a voltage remains present at V_O after an SCP operation performed with STBY set on.

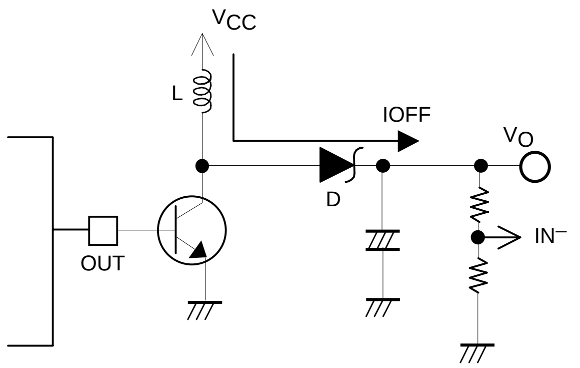


Figure Used with a Chopper Type Step-up Circuit