



## 1.8V CONFIGURABLE BUFFER WITH ADDRESS- PARITY TEST

**IDT74SSTUA32866**

### FEATURES:

- 1.8V Operation
- SSTL\_18 style clock and data inputs
- Differential CLK input
- Configurable as 25-bit 1:1 or 14-bit 1:2 registered buffer
- Control inputs compatible with LVCMOS levels
- Flow-through architecture for optimum PCB design
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Checks parity on data inputs
- Maximum operating frequency: 410MHz
- Optimized for DDR2 - 400 / 533 / 667 (PC2 - 3200 / 4300 / 5300) JEDEC R/C E, F, G, H, and J
- Available in 96-pin LFBGA package

### APPLICATIONS:

- Along with CSPUA877 DDR2 PLL, provides complete solution for DDR2 DIMMs

### DESCRIPTION:

This 25-bit 1:1 / 14-bit 1:2 configurable registered buffer is designed for 1.7V to 1.9V  $V_{DD}$  operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive eighteen SDRAM loads. All inputs are SSTL\_18, except reset ( $\overline{RESET}$ ) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL\_18 specifications, except the open-drain error ( $\overline{QERR}$ ) output.

The SSTUA32866 operates from a differential clock (CLK and  $\overline{CLK}$ ). Data are registered at the crossing of CLK going high and  $\overline{CLK}$  going low. Parity is checked on the parity bit (PAR\_IN) input which arrives one cycle after the input data to which it applies. The  $\overline{QERR}$  output is open drain.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, the partial-parity-out (PPO) and  $\overline{QERR}$  signals are produced two clock cycles after the corresponding data output.

When used in pairs, the C0 input of the first register is tied low and the C0 input of the second register is tied high. The C1 input of both registers are tied high. The  $\overline{QERR}$  output of the first SSTUA32866 is left floating and the valid error information is latched on the  $\overline{QERR}$  output of the second SSTUA32866.

If an error occurs and the  $\overline{QERR}$  output is driven low, it stays latched low for two clock cycles or until  $\overline{RESET}$  is driven low. The DIMM-dependent signals (DODT, DCKE,  $\overline{DCS}$ , and  $\overline{CSR}$ ) are not included in the parity check.

The C0 input controls the pinout configuration of the 1:2 pinout from register A configuration (when low) to register B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

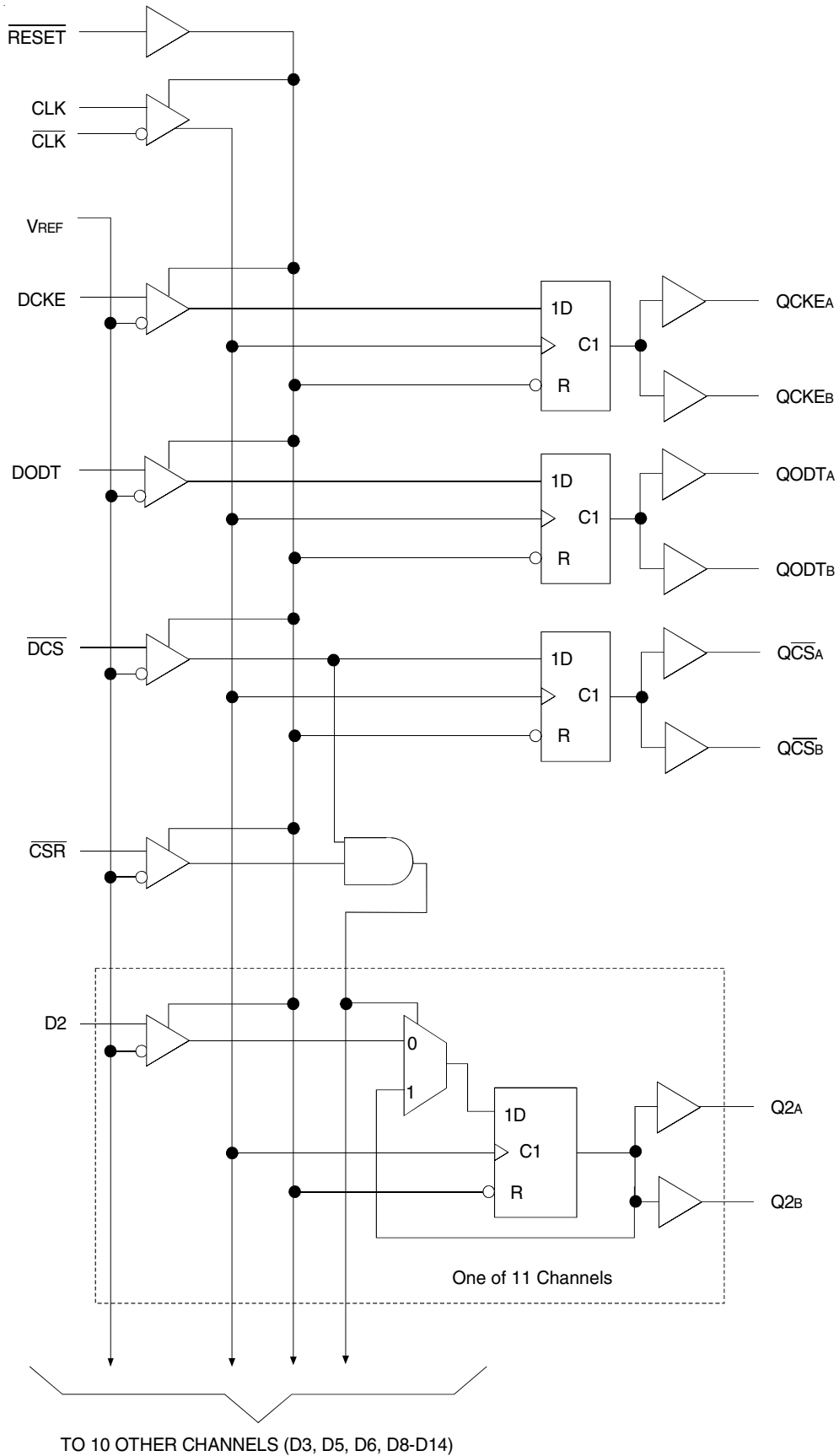
The device supports low-power standby operation. When  $\overline{RESET}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{REF}$ ) inputs are allowed. In addition, when  $\overline{RESET}$  is low, all registers are reset and all outputs except  $\overline{QERR}$  are forced low. The LVCMOS  $\overline{RESET}$  and Cn inputs always must be held at a valid logic high or low level.

There are two  $V_{REF}$  pins (A3 and T3). However, it is necessary to only connect one of the two  $V_{REF}$  pins to the external  $V_{REF}$  power supply. An unused  $V_{REF}$  pin should be terminated with a  $V_{REF}$  coupling capacitor.

The device also supports low-power active operation by monitoring both system chip select ( $\overline{DCS}$  and  $\overline{CSR}$ ) inputs and will gate the Qn and PPO outputs from changing states when both  $\overline{DCS}$  and  $\overline{CSR}$  inputs are high. If either  $\overline{DCS}$  or  $\overline{CSR}$  input is low, the Qn and PPO outputs will function normally. Also, if the internal low power signal ( $\overline{LPS1}$ ) is high, the device will gate the  $\overline{QERR}$  output from changing states. If  $\overline{LPS1}$  is low, the  $\overline{QERR}$  output will function normally. The  $\overline{RESET}$  input has priority over the  $\overline{DCS}$  and  $\overline{CSR}$  control and when driven low will force the Qn and PPO outputs low, and the  $\overline{QERR}$  output high. If the  $\overline{DCS}$  control functionality is not desired, then the  $\overline{CSR}$  input can be hard-wired to ground, in which case the setup-time requirement for  $\overline{DCS}$  would be the same as for the other D data inputs. To control the low-power mode with  $\overline{DCS}$  only, then the  $\overline{CSR}$  input should be pulled up to  $V_{DD}$  through a pullup resistor.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{RESET}$  must be held in the low state during power up.

FUNCTIONAL BLOCK DIAGRAM (1:2) - A CONFIGURATION (POSITIVE LOGIC)





### PIN CONFIGURATION (TYPE A)

6	QCKEB	Q2B	Q3B	QODTB	Q5B	Q6B	C0	$\overline{\text{QCSB}}$	NC	Q8B	Q9B	Q10B	Q11B	Q12B	Q13B	Q14B
5	QCKEA	Q2A	Q3A	QODTA	Q5A	Q6A	C1	$\overline{\text{QCSA}}$	NC	Q8A	Q9A	Q10A	Q11A	Q12A	Q13A	Q14A
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	PPO	DNU	DNU	$\overline{\text{QERR}}$	DNU	DNU	$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	DNU	DNU	DNU	DNU	DNU	DNU	DNU
1	DCKE	D2	D3	DODT	D5	D6	PAR_IN	CLK	$\overline{\text{CLK}}$	D8	D9	D10	D11	D12	D13	D14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

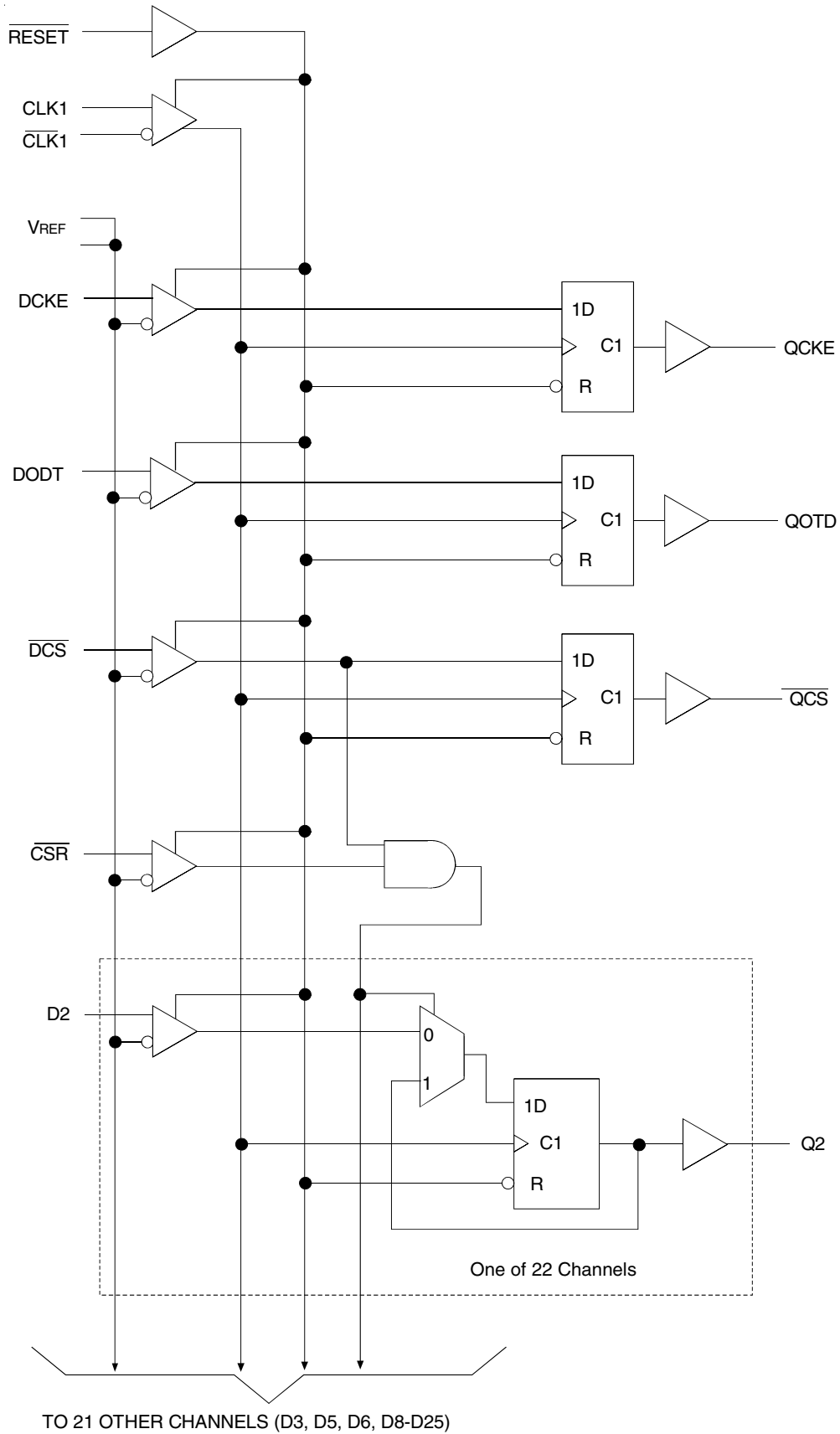
96-PIN LFBGA  
1:2 REGISTER (TYPE A, FRONTSIDE)  
TOP VIEW

### PIN CONFIGURATION (TYPE B)

6	Q1B	Q2B	Q3B	Q4B	Q5B	Q6B	C0	$\overline{\text{QCSB}}$	NC	Q8B	Q9B	Q10B	QODTB	Q12B	Q13B	QCKEB
5	Q1A	Q2A	Q3A	Q4A	Q5A	Q6A	C1	$\overline{\text{QCSA}}$	NC	Q8A	Q9A	Q10A	QODTA	Q12A	Q13A	QCKEA
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	PPO	DNU	DNU	$\overline{\text{QERR}}$	DNU	DNU	$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	DNU	DNU	DNU	DNU	DNU	DNU	DNU
1	D1	D2	D3	D4	D5	D6	PAR_IN	CLK	$\overline{\text{CLK}}$	D8	D9	D10	DODT	D12	D13	DCKE
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

96-PIN LFBGA  
1:2 REGISTER (TYPE B, BACKSIDE)  
TOP VIEW

### FUNCTIONAL BLOCK DIAGRAM (1:1)



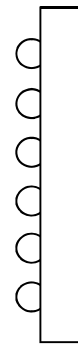
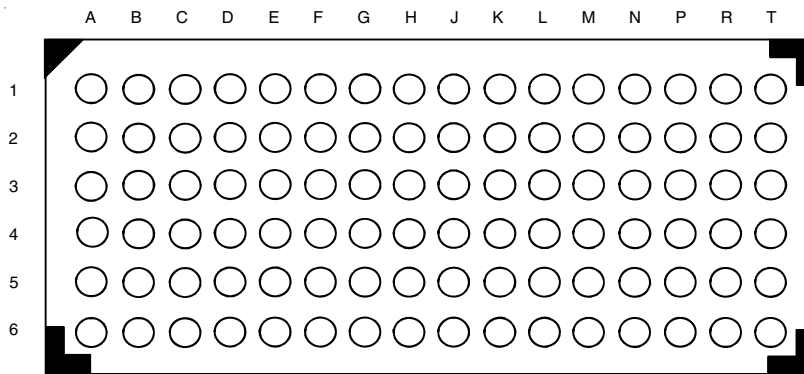
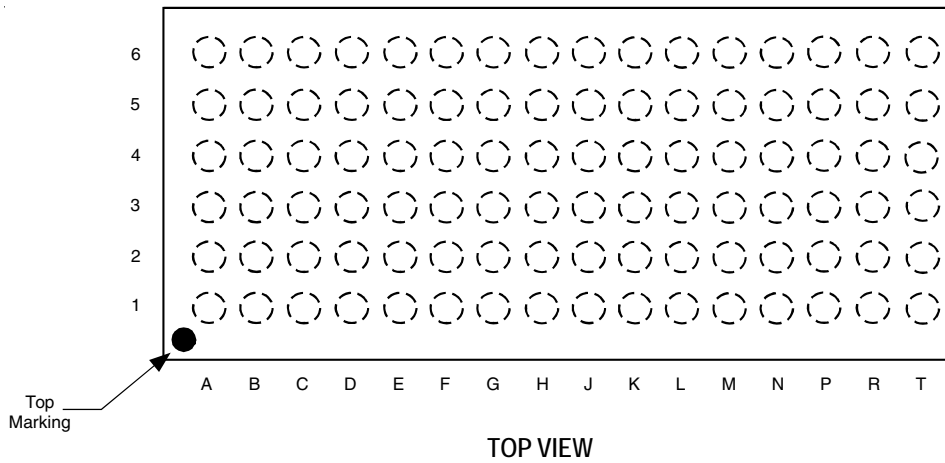
### PIN CONFIGURATION

6	DNU	Q15	Q16	DNU	Q17	Q18	C0	DNU	NC	Q19	Q20	Q21	Q22	Q23	Q24	Q25
5	QCKE	Q2	Q3	QODT	Q5	Q6	C1	$\overline{QCS}$	NC	Q8	Q9	Q10	Q11	Q12	Q13	Q14
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	PPO	D15	D16	$\overline{QEERR}$	D17	D18	$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	D19	D20	D21	D22	D23	D24	D25
1	DCKE	D2	D3	DODT	D5	D6	PAR_IN	CLK	$\overline{CLK}$	D8	D9	D10	D11	D12	D13	D14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

\*Rows 3 and 4 are reserved for VDD and GND.

96-PIN LFBGA  
 1:1 REGISTER  
 TOP VIEW

### 96 BALL LFBGA PACKAGE ATTRIBUTES



BOTTOM VIEW

SIDE VIEW

FUNCTION TABLE (EACH FLIP-FLOP) (1)

Inputs						Qx Outputs	$\overline{QCSx}$ Output	QODTx, QCKEx Outputs
RESET	DCS	CSR	CLK	CLK	Dx, DODT, DCKE			
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	$Q_0^{(2)}$	$Q_0^{(2)}$	$Q_0^{(2)}$
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	$Q_0^{(2)}$	$Q_0^{(2)}$	$Q_0^{(2)}$
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	$Q_0^{(2)}$	$Q_0^{(2)}$	$Q_0^{(2)}$
H	H	H	↑	↓	L	$Q_0^{(2)}$	H	L
H	H	H	↑	↓	H	$Q_0^{(2)}$	H	H
H	H	H	L or H	L or H	X	$Q_0^{(2)}$	$Q_0^{(2)}$	$Q_0^{(2)}$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW to HIGH  
↓ = HIGH to LOW
- Output level before the indicated steady-state conditions were established.

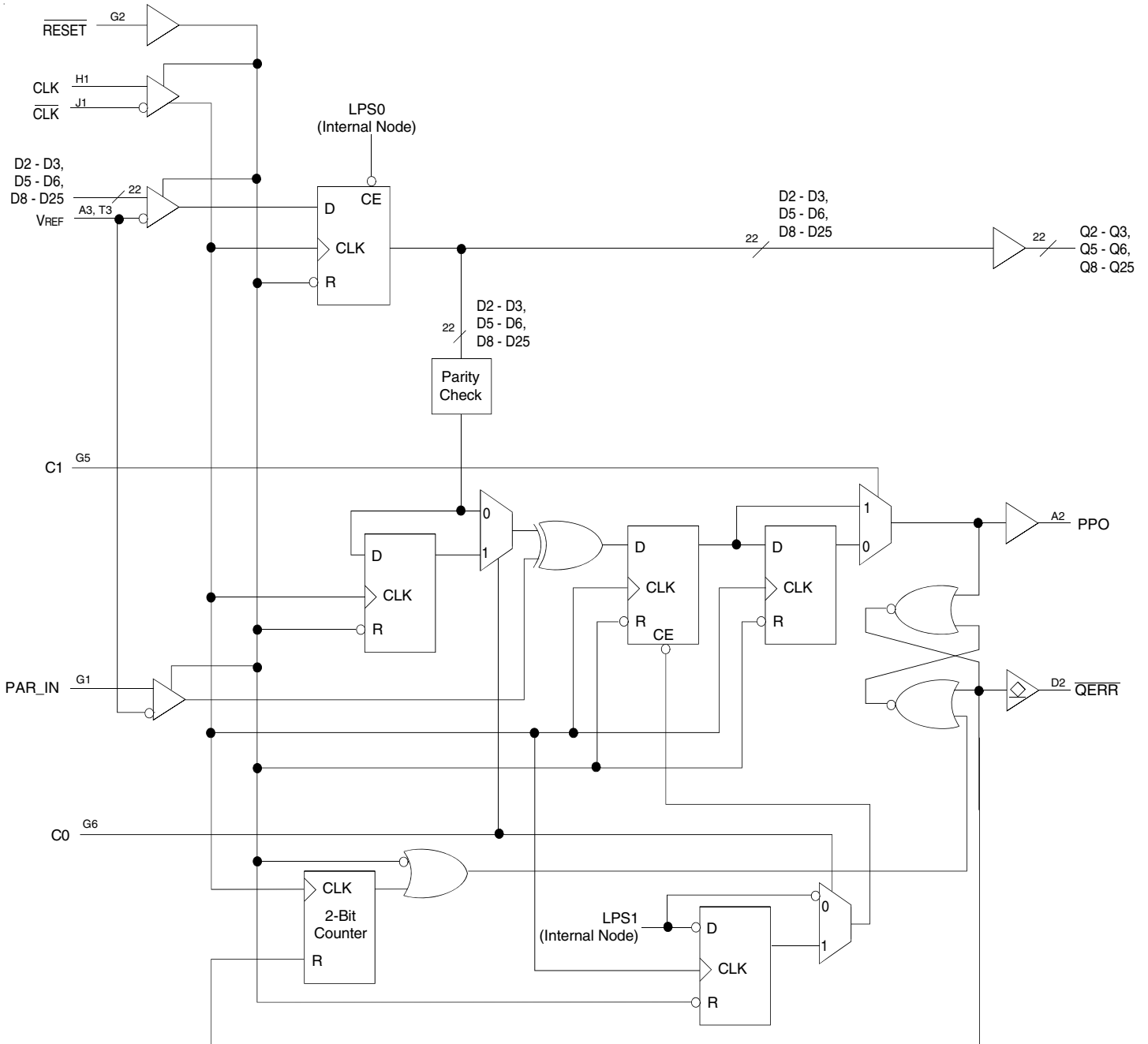
PARITY AND STANDBY FUNCTION TABLE(1)

Inputs						Outputs		
RESET	DCS	CSR	CLK	CLK	$\Sigma$ of Inputs = H (D1 - D25)	PAR_IN <sup>(2)</sup>	PPO <sup>(3)</sup>	$\overline{QERR}$ <sup>(4)</sup>
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	H	L	↑	↓	Even	L	L	H
H	H	L	↑	↓	Odd	L	H	L
H	H	L	↑	↓	Even	H	H	L
H	H	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	PPO <sub>0</sub>	$\overline{QERR}_0$
H	X	X	L or H	L or H	X	X	PPO <sub>0</sub>	$\overline{QERR}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	H

NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW to HIGH  
↓ = HIGH to LOW
- Data Inputs = D2, D3, D5, D6, D8 - D25 when C0 = 0 and C1 = 0.  
Data Inputs = D2, D3, D5, D6, D8 - D14 when C0 = 0 and C1 = 1.  
Data Inputs = D1 - D6, D8 - D10, D12, D13 when C0 = 1 and C1 = 1.
- PAR\_IN arrives one clock cycle (C0 = 0), or two clock cycles (C0 = 1), after the data to which it applies.
- This transition assumes  $\overline{QERR}$  is HIGH at the crossing of CLK going HIGH and CLK going LOW. If  $\overline{QERR}$  is LOW, it stays latched LOW for two clock cycles or until RESET is driven LOW.

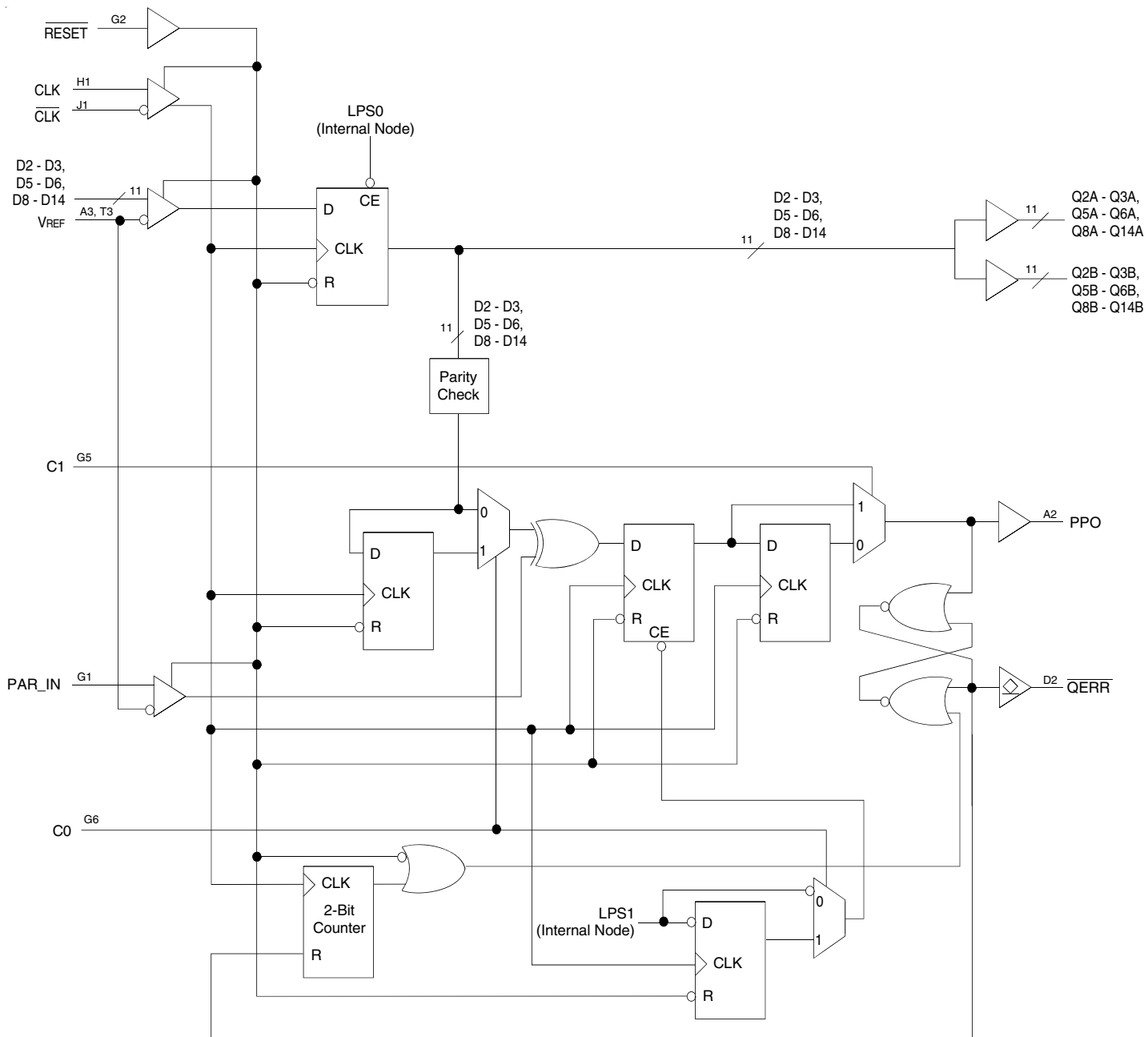
LOGIC DIAGRAM (1:1)



Parity Logic Diagram for 1:1 Register - A Configuration (Positive Logic); C0 = 0, C1 = 0



LOGIC DIAGRAM (1:2)



Parity Logic Diagram for 1:2 Register - A Configuration (Positive Logic);  $C0 = 0, C1 = 1$

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V <sub>DD</sub>	Supply Voltage Range	-0.5 to 2.5	V
V <sub>I</sub> <sup>(2,3)</sup>	Input Voltage Range	-0.5 to 2.5	V
V <sub>O</sub> <sup>(2,3)</sup>	Output Voltage Range	-0.5 to V <sub>DD</sub> +0.5	V
I <sub>IK</sub>	Input Clamp Current	±50	mA
	V <sub>I</sub> < 0		
	V <sub>I</sub> > V <sub>DD</sub>		
I <sub>OK</sub>	Output Clamp Current	±50	mA
	V <sub>O</sub> < 0		
	V <sub>O</sub> > V <sub>DD</sub>		
I <sub>O</sub>	Continuous Output Current, V <sub>O</sub> = 0 to V <sub>DD</sub>	±50	mA
V <sub>DD</sub>	Continuous Current through each V <sub>DD</sub> or GND	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

## MODE SELECT

C <sub>0</sub>	C <sub>1</sub>	Device Mode
0	0	1:1 25-bit to 25-bit
0	1	1:2 14-bit to 28-bit, Front (Type A)
1	0	Reserved
1	1	1:2 14-bit to 28-bit, Back (Type B)

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
- This value is limited to 2.5V maximum.

## TERMINAL FUNCTIONS (ALL PINS)

Terminal Name	Electrical Characteristics	Description
GND	Ground Input	Ground
V <sub>DD</sub>	1.8V nominal	Power Supply Voltage
V <sub>REF</sub>	0.9V nominal	Input Reference Voltage
CLK	Differential Input	Positive Master Clock Input
$\overline{\text{CLK}}$	Differential Input	Negative Master Clock Input
C <sub>X</sub>	LVC MOS Input	Configuration Control Inputs
$\overline{\text{RESET}}$	LVC MOS Input	Asynchronous Reset Input. Resets registers and disables V <sub>REF</sub> data and clock differential-input receivers.
$\overline{\text{CSR}}, \overline{\text{DCS}}$	SSTL_18 Input	Chip Select Inputs. Disables outputs Dx switching when both inputs are HIGH.
D <sub>X</sub>	SSTL_18 Input	Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$ .
D <sub>ODT</sub>	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
D <sub>CKE</sub>	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
Q <sub>X</sub>	1.8V CMOS	Data Outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
$\overline{\text{QCS}}_x$	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
Q <sub>ODTx</sub>	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
Q <sub>CKEx</sub>	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
PAR_IN	SSTL_18 Input	Parity Input. Clocked on the rising edge of CLK one cycle after corresponding data input.
$\overline{\text{QERR}}$	Open Drain Output	Output Error bit, generated one cycle after the corresponding data output
PPO	1.8V CMOS	Partial Parity Output. Indicates ODD parity of Data Inputs and Parity In.

OPERATING CHARACTERISTICS,  $T_A = 25^\circ\text{C}$  (1,2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	1.7	—	1.9	V
VREF	Reference Voltage	$0.49 * V_{DD}$	$0.5 * V_{DD}$	$0.51 * V_{DD}$	V
VTT	Termination Voltage	$V_{REF} - 40\text{mV}$	VREF	$V_{REF} + 40\text{mV}$	V
Vi	Input Voltage	0	—	VDD	V
VIH	AC High-Level Input Voltage	$V_{REF} + 250\text{mV}$	—	—	V
VIL	AC Low-Level Input Voltage	—	—	$V_{REF} - 250\text{mV}$	
VIH	DC High-Level Input Voltage	$V_{REF} + 125\text{mV}$	—	—	
VIL	DC Low-Level Input Voltage	—	—	$V_{REF} - 125\text{mV}$	
VIH	High-Level Input Voltage	$0.65 * V_{DD}$	—	—	V
VIL	Low-Level Input Voltage	—	—	$0.35 * V_{DD}$	V
VICR	Common Mode Input Voltage	0.675	—	1.125	V
VID	Differential Input Voltage	600	—	—	mV
IOH	High-Level Output Current	—	—	-8	mA
IOL	Low-Level Output Current	—	—	8	
TA	Operating Free-Air Temperature	0	—	70	$^\circ\text{C}$

NOTES:

1. The  $\overline{\text{RESET}}$  and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless  $\overline{\text{RESET}}$  is LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOH	Output HIGH Voltage	$I_{OH} = -6\text{ mA}$	1.2	—	—	V
VOL	Output LOW Voltage	$I_{OL} = 6\text{ mA}$	—	—	0.5	V
Ii	All Inputs <sup>(1)</sup>	$V_i = V_{DD}$ or GND; $V_{DD} = 1.9\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
IDD	Static Standby	$I_O = 0$ , $V_{DD} = 1.9\text{V}$ , $\overline{\text{RESET}} = \text{GND}$	—	—	100	$\mu\text{A}$
	Static Operating	$I_O = 0$ , $V_{DD} = 1.9\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$	—	—	40	mA
IDDD	Dynamic Operating (Clock Only)	$I_O = 0$ , $V_{DD} = 1.8\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$ , CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.	—	—	—	$\mu\text{A}/\text{Clock MHz}$
	Dynamic Operating (Per Each Data Input)	$I_O = 0$ , $V_{DD} = 1.8\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$ , CLK and $\overline{\text{CLK}}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	1:1 Mode	—	—	$\mu\text{A}/\text{Clock MHz}/\text{Data Input}$
			1:2 Mode	—	—	
Ci	Data Inputs, $\overline{\text{CSR}}$ , PAR_IN		2.5	—	3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR} = 0.9\text{V}$ , $V_{ID} = 600\text{mV}$	2	—	3	
	$\overline{\text{RESET}}$	$V_i = V_{DD}$ or GND	—	—	—	

NOTE:

1. Each VREF pin (A3, T3) should be tested independently, with the other pin open circuit.

## TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter	V <sub>DD</sub> = 1.8V ± 0.1V		Unit	
		Min.	Max.		
f <sub>CLOCK</sub>	Clock Frequency	—	410	MHz	
t <sub>w</sub>	Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW	1	—	ns	
t <sub>ACT</sub> <sup>(1,2)</sup>	Differential Inputs Active Time	—	10	ns	
t <sub>INACT</sub> <sup>(1,3)</sup>	Differential Inputs Inactive Time	—	15	ns	
t <sub>SU</sub>	Setup Time	$\overline{\text{DCS}}$ before CLK $\uparrow$ , CLK $\downarrow$ , $\overline{\text{CSR}}$ HIGH; $\overline{\text{CSR}}$ before CLK $\uparrow$ , CLK $\downarrow$ , $\overline{\text{DCS}}$ HIGH	0.7	—	ns
		$\overline{\text{DCS}}$ before CLK $\uparrow$ , CLK $\downarrow$ , $\overline{\text{CSR}}$ LOW	0.5	—	
		DODT, DCKE, and data before CLK $\uparrow$ , CLK $\downarrow$	0.5	—	
		PAR_IN before CLK $\uparrow$ , CLK $\downarrow$	0.5	—	
t <sub>H</sub>	Hold Time	$\overline{\text{DCS}}$ , DODT, DCKE, and data after CLK $\uparrow$ , CLK $\downarrow$	0.5	—	ns
		PAR_IN after CLK $\uparrow$ , CLK $\downarrow$	0.5	—	

### NOTES:

1. This parameter is not production tested.
2. Data and V<sub>REF</sub> inputs must be low a minimum time of t<sub>ACT</sub> max, after  $\overline{\text{RESET}}$  is taken HIGH.
3. Data, V<sub>REF</sub>, and clock inputs must be held at valid levels (not floating) a minimum time of t<sub>INACT</sub> max, after  $\overline{\text{RESET}}$  is taken LOW.

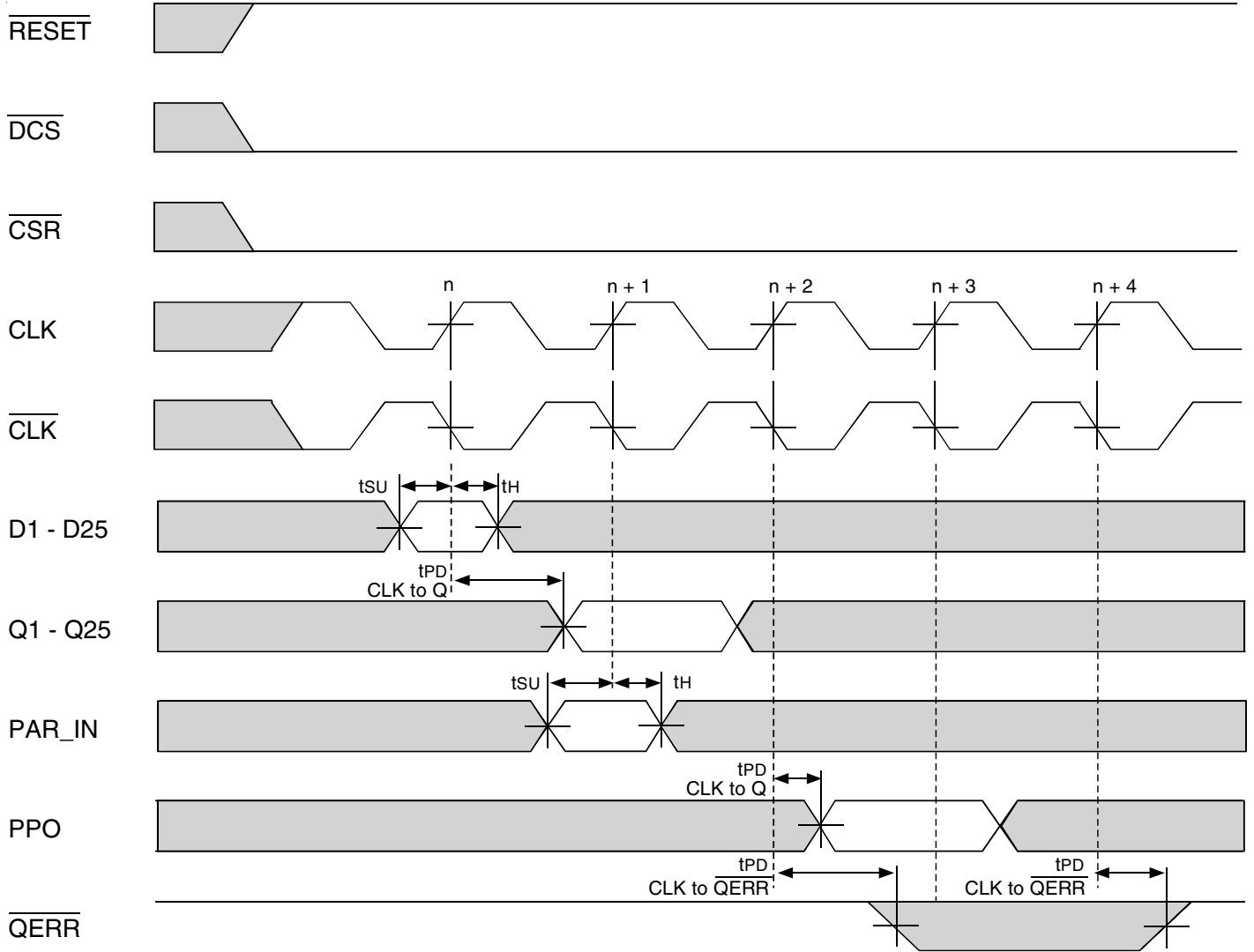
## SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) <sup>(1)</sup>

Symbol	Parameter	V <sub>DD</sub> = 1.8V ± 0.1V		Unit
		Min	Max.	
f <sub>MAX</sub>		410	—	MHz
t <sub>PDM</sub> <sup>(2)</sup>	CLK and $\overline{\text{CLK}}$ to Q	1.2	1.9	ns
t <sub>PDMSS</sub> <sup>(2,3)</sup>	CLK and $\overline{\text{CLK}}$ to Q (simultaneous switching)	—	2	ns
t <sub>RPHL</sub>	$\overline{\text{RESET}}$ to Q	—	3	ns
dV/dt <sub>r</sub>	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt <sub>f</sub>	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt $\Delta$ <sup>(4)</sup>	Output slew rate from 20% to 80%	—	1	V/ns
t <sub>PD</sub>	CLK and $\overline{\text{CLK}}$ to PPO	0.5 <sup>(5)</sup>	1.8 <sup>(5)</sup>	ns
t <sub>PLH</sub>	CLK and $\overline{\text{CLK}}$ to QERR	1.2 <sup>(5)</sup>	3 <sup>(5)</sup>	ns
t <sub>PHL</sub>	CLK and $\overline{\text{CLK}}$ to QERR	1 <sup>(5)</sup>	2.4 <sup>(5)</sup>	ns
t <sub>RPHL</sub>	$\overline{\text{RESET}}$ to PPO	—	3	ns
t <sub>RPLH</sub>	$\overline{\text{RESET}}$ to QERR	—	3	ns

### NOTES:

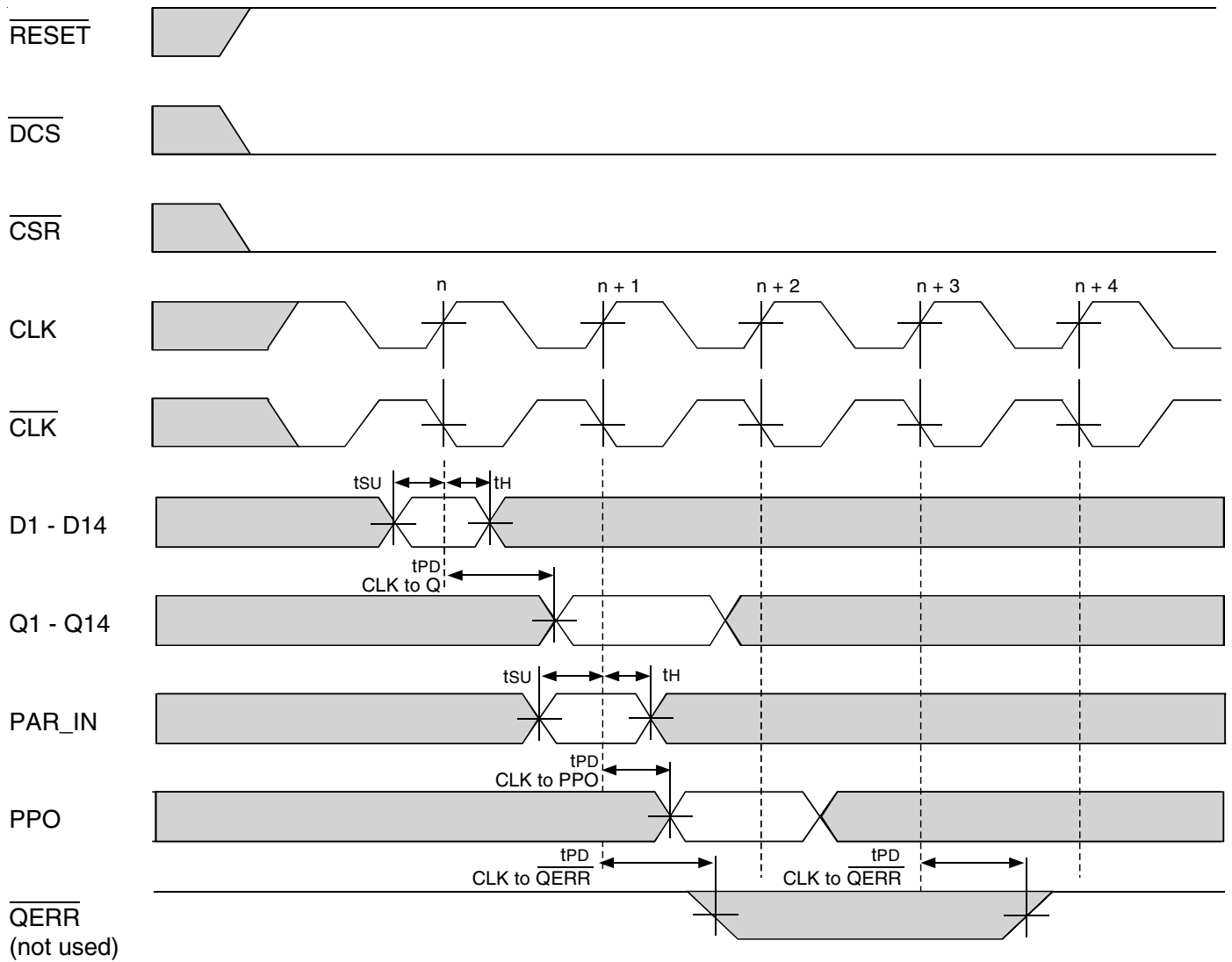
1. See TEST CIRCUITS AND WAVEFORMS.
2. Includes 350ps of test load transmission line delay.
3. This parameter is not production tested.
4. Difference between dV/dt<sub>r</sub> (rising edge rate) and dV/dt<sub>f</sub> (falling edge rate).
5. For reference only. Final values to be determined.

REGISTER TIMING



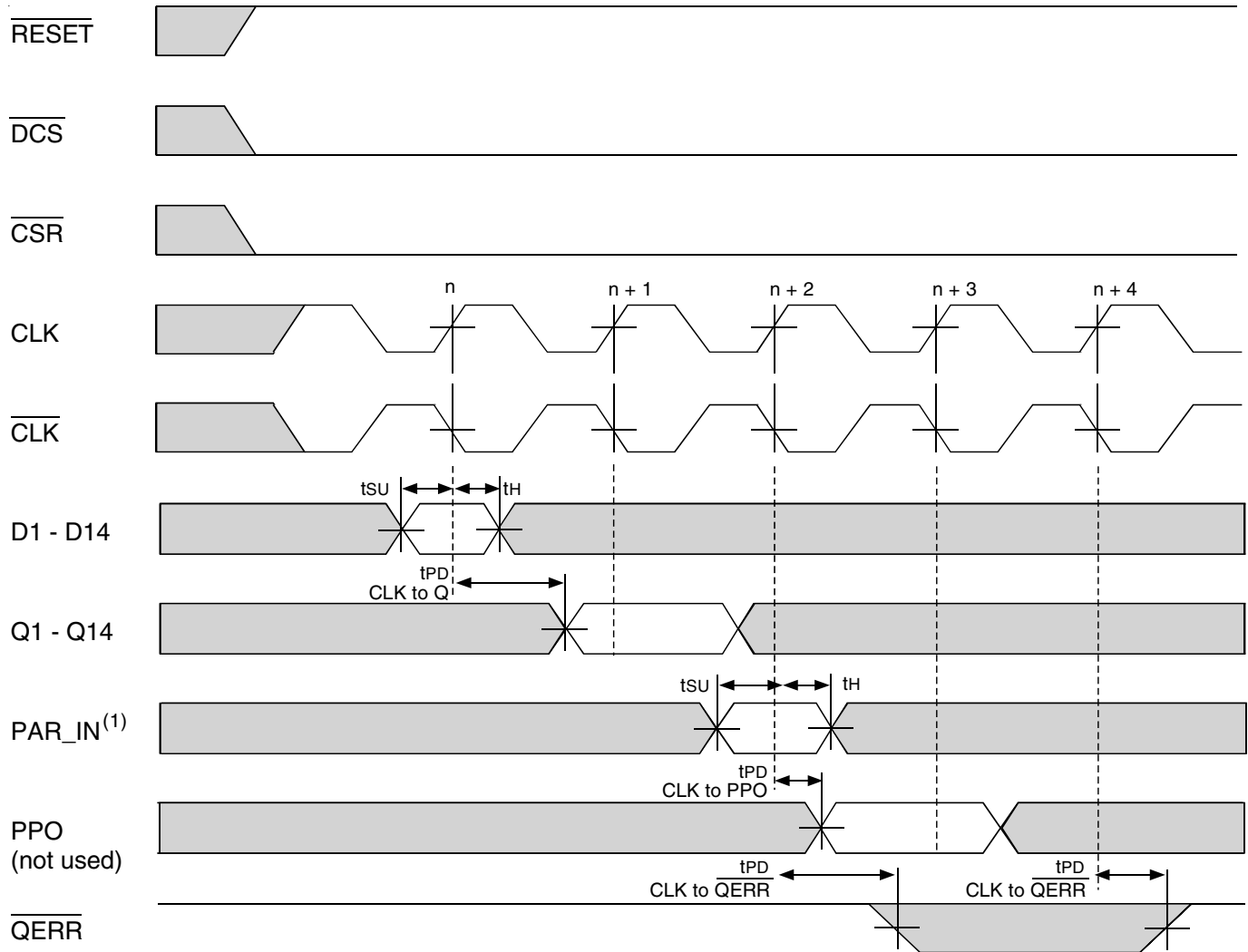
Timing Diagram for SSTUA32866 Used as a Single Device; C0 = 0, C1 = 0

## REGISTER TIMING



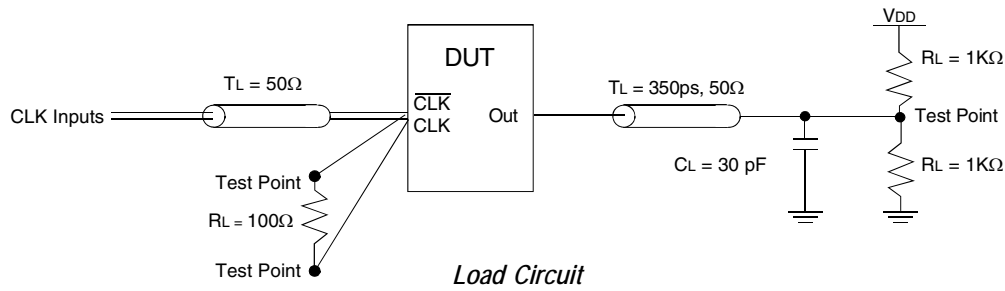
Timing Diagram for the First SSTUA32866 (1:2 Register-A Configuration) Device Used in a Pair; C0 = 0, C1 = 1

## REGISTER TIMING

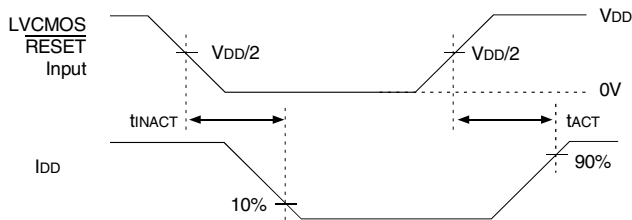


Timing Diagram for the First SSTUA32866 (1:2 Register-B Configuration) Device Used in a Pair; C0 = 1, C1 = 1

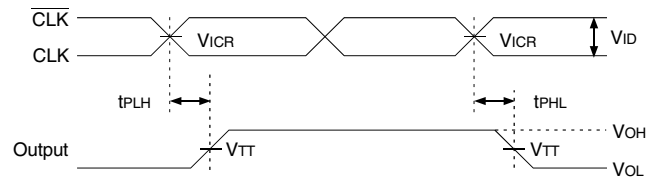
TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )



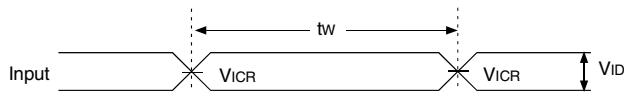
Load Circuit



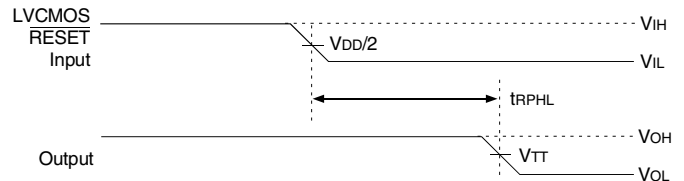
Voltage and Current Waveforms  
Inputs Active and Inactive Times



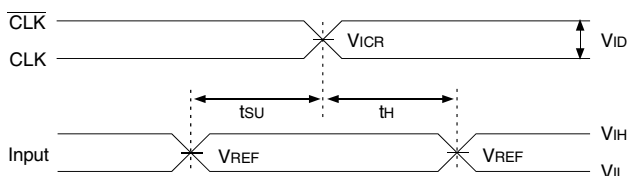
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



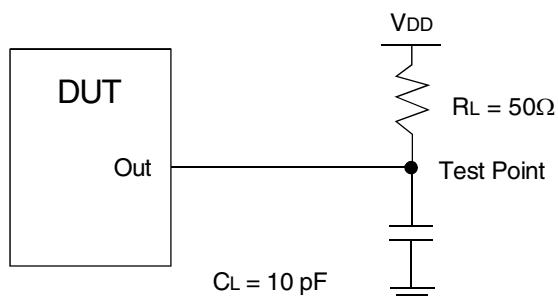
Voltage Waveforms - Setup and Hold Times

NOTES:

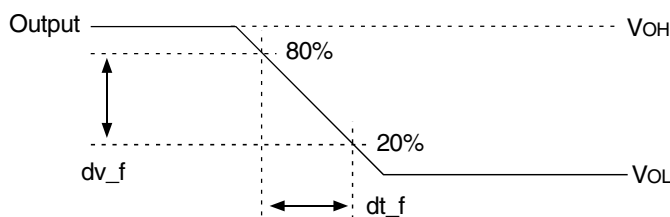
1. CL includes probe and jig capacitance.
2. IDD tested with clock and data inputs held at VDD or GND, and Io = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Zo = 50Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. VTT = VREF = VDD/2
6. VIH = VREF + 250mV (AC voltage levels) for differential inputs. VIH = VDD for LVC MOS input.
7. VIL = VREF - 250mV (AC voltage levels) for differential inputs. VIL = GND for LVC MOS input.
8. VID = 600mV.
9. tPLH and tPHL are the same as tPDM.



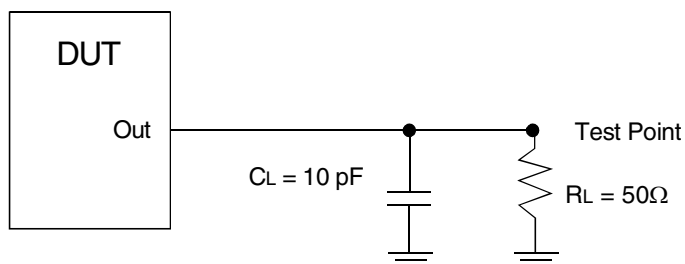
TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )



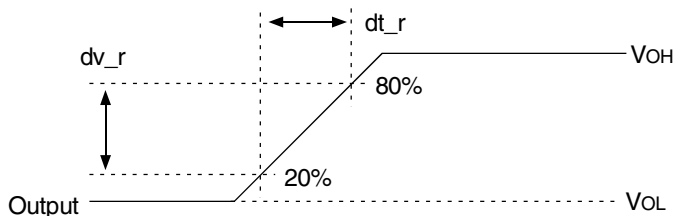
*Load Circuit: High-to-Low Slew-Rate Adjustment*



*Voltage Waveforms: High-to-Low Slew-Rate Adjustment*



*Load Circuit: Low-to-High Slew-Rate Adjustment*

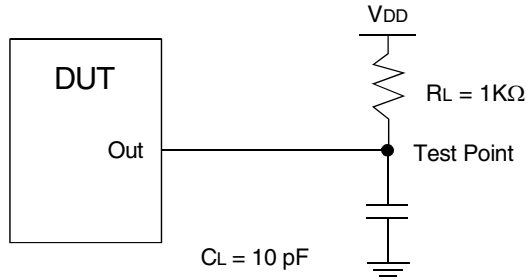


*Voltage Waveforms: Low-to-High Slew-Rate Adjustment*

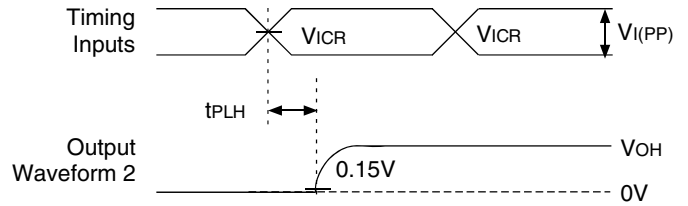
NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Zo = 50Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

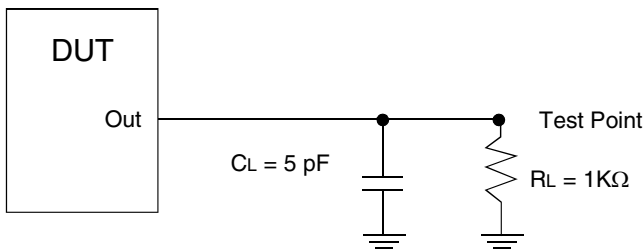
TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )



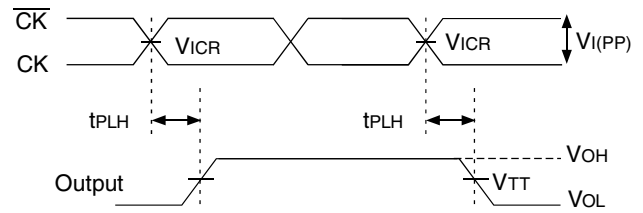
Load Circuit: **QERR** Output



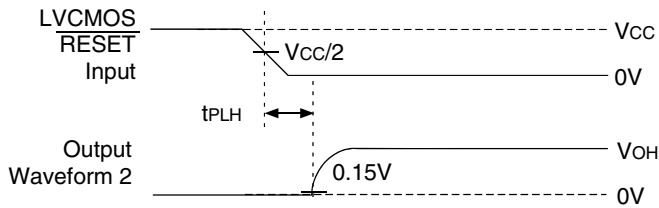
Voltage Waveforms - Open-Drain Output LOW-to-HIGH Transition Time with Respect to Clock Inputs



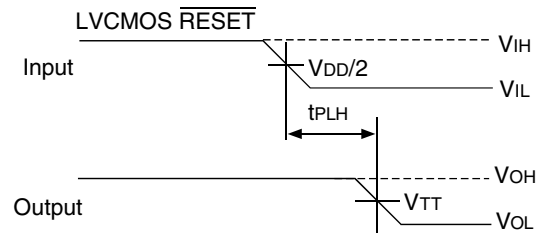
Load Circuit: Partial-Parity-Out Load Circuit



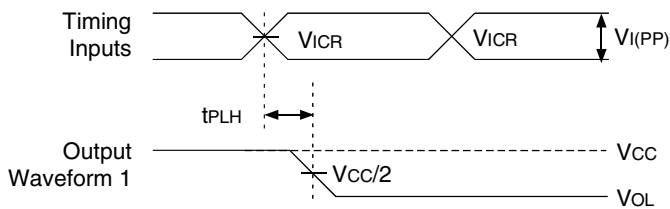
Voltage Waveforms - Propagation Delay Times with with Respect to Clock Inputs



Voltage Waveforms - Open-Drain Output LOW-to-HIGH Transition Time with Respect to Reset Input



Voltage Waveforms - Propagation Delay Times with with Respect to Reset Input

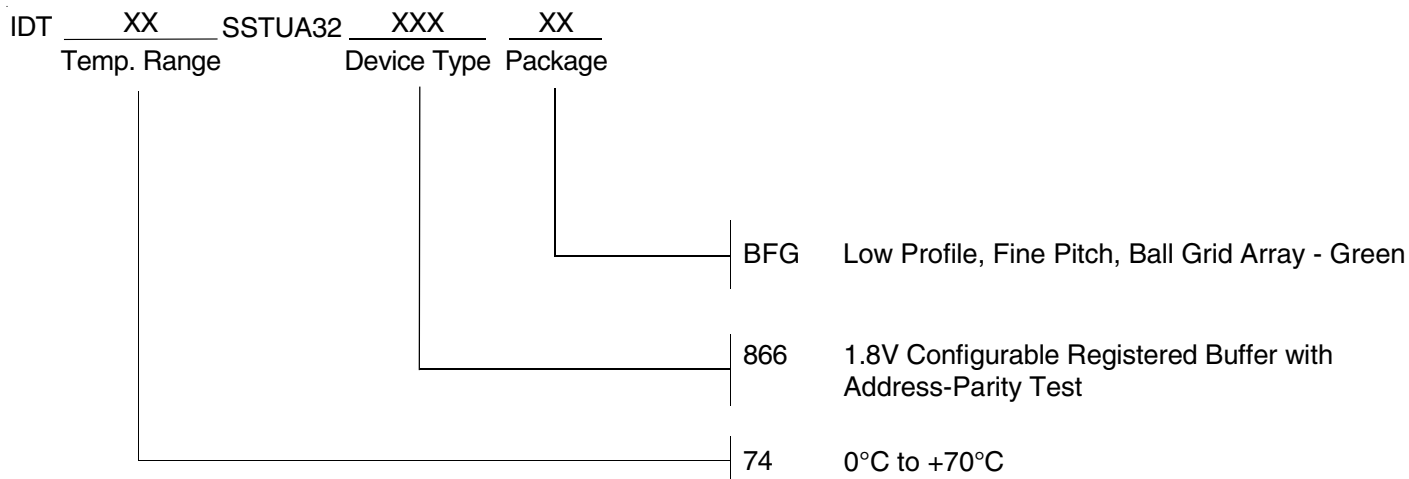


Voltage Waveforms - Open-Drain Output HIGH-to-LOW Transition Time with Respect to Clock Inputs

NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Zo = 50Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

## ORDERING INFORMATION



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