TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91CW12A

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to 4, INTRTC) which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP91CW12AF

1. Outline and Features

TMP91CW12AF is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91CW12AF comes in a 100-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (1.0 μs/2 bytes at 16 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 4 Kbytes
Built-in ROM: 128 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ・・・Dynamic data bus sizing

(5) 8-bit timers: 8 channels

(6) 16-bit timer/event counter: 2 channels

(7) General-purpose serial interface: 2 channels
- UART/Synchronous mode: 2 channels
- IrDA ver 1.0 (115.2 kbps) supported: 1 channel

(8) Serial bus interface: 1 channel
- I^2C bus mode/clock synchronous select mode

(9) 10-bit AD converter (sample-hold circuit is built in): 8 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip Select/Wait controller: 4 channels

(13) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 26 internal interrupts: 7-level priority can be set.
- 10 external interrupts: 7-level priority can be set.

(14) Input/output ports: 81 pins

(15) Standby function
Three Halt modes: Idle2 (programmable), Idle1, Stop

(16) Triple-clock controller
- Clock Doubler (DFM)
- Clock Gear (fc to fc/16)
- Slow mode (fs = 32.768 kHz)

(17) Operating voltage
- V_{CC} = 2.7 V to 3.6 V (fc max = 27 MHz)
- V_{CC} = 1.8 V to 3.6 V (fc max = 10 MHz)

(18) Package
- 100-pin QFP: P-LQFP100-1414-0.50F

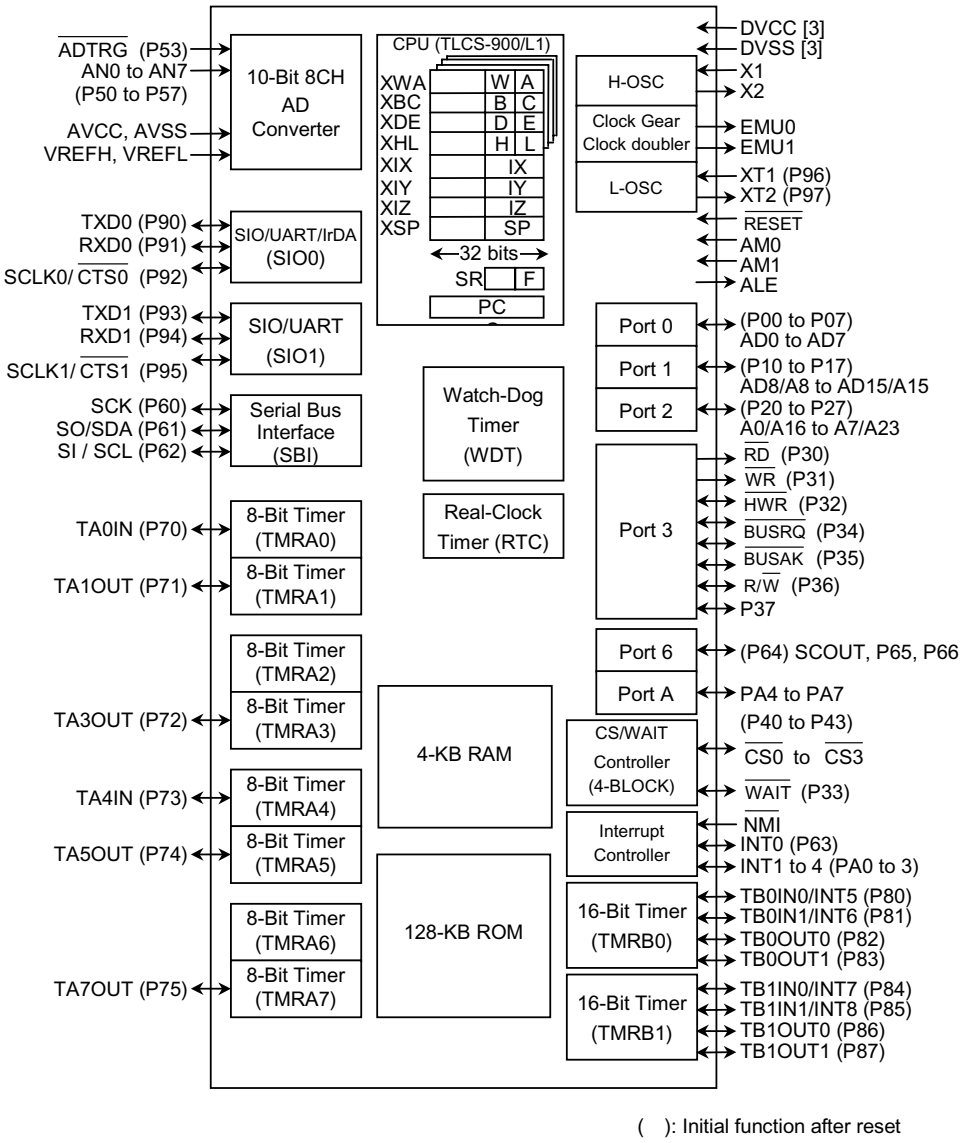


Figure 1.1 TMP91CW12AF Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91CW12AF, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91CW12AF.

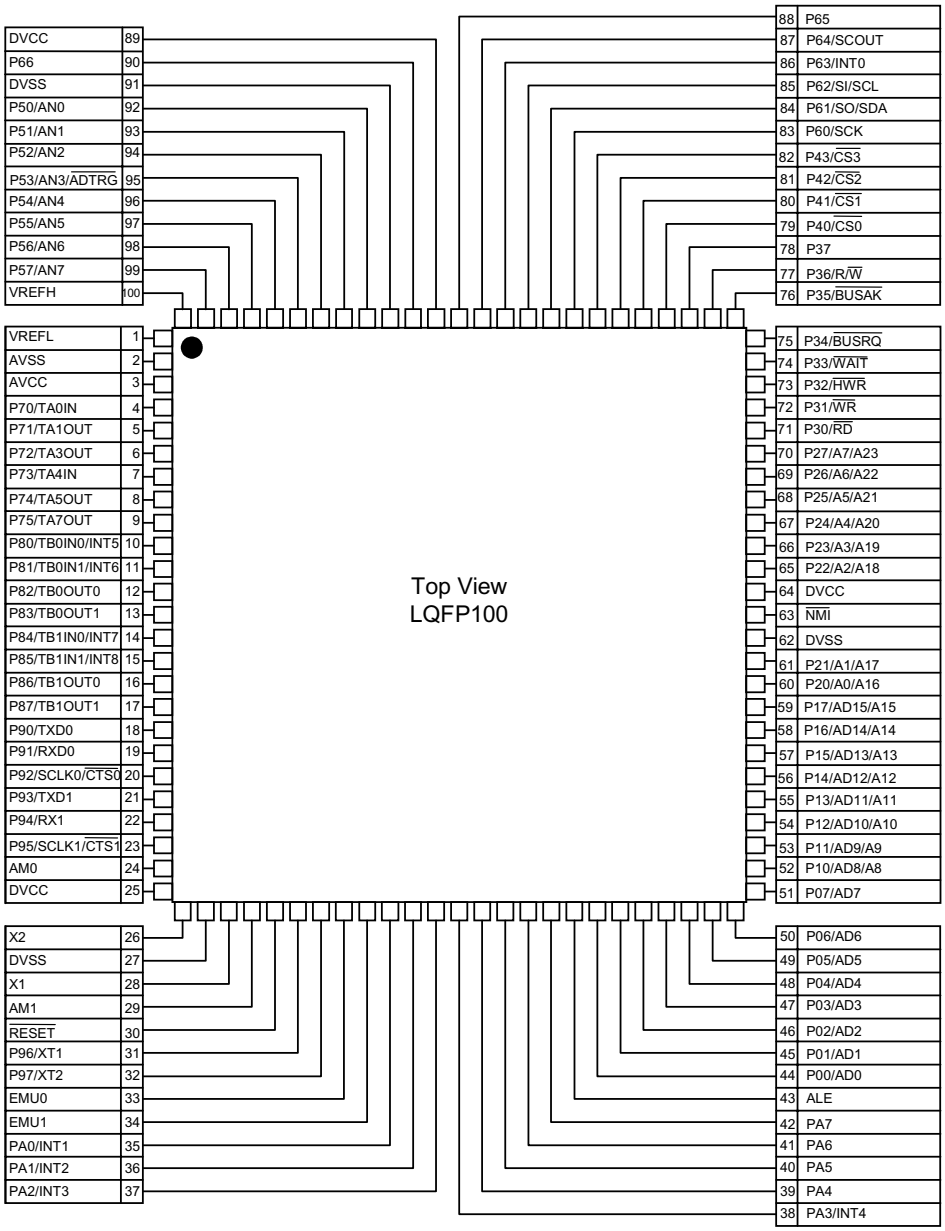


Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin Names and Functions (1/3)

Pin Name	Number of Pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows I/O to be selected at the bit level
AD0 to AD7		Tri-state	Address and data (lower): Bits 0 to 7 of address and data bus
P10 to P17	8	I/O	Port 1: I/O port that allows I/O to be selected at the bit level
AD8 to AD15		Tri-state	Address and data (upper): Bits 8 to 15 for address and data bus
A8 to A15		Output	Address: Bits 8 to 15 of address bus
P20 to P27	8	I/O	Port 2: I/O port that allows I/O to be selected at the bit level
A0 to A7		Output	Address: Bits 0 to 7 of address bus
A16 to A23		Output	Address: Bits 16 to 23 of address bus
P30	1	Output	Port 30: Output port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data to pins AD0 to AD7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High Write: Strobe signal for writing data to pins AD8 to AD15
P33	1	I/O	Port 33: I/O port (with pull-up resistor)
$\overline{WAIT}$		Input	Wait: Pin used to request CPU bus wait
P34	1	I/O	Port 34: I/O port (with pull-up resistor)
$\overline{BUSRQ}$		Input	Bus Request: Signal used to request Bus Release
P35	1	I/O	Port 35: I/O port (with pull-up resistor)
$\overline{BUSAK}$		Output	Bus Acknowledge: Signal used to acknowledge Bus Release
P36	1	I/O	Port 36: I/O port (with pull-up resistor)
R/$\overline{W}$		Output	Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40	1	I/O	Port 40: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip Select 0: Outputs 0 when address is within specified address area
P41	1	I/O	Port 41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip Select 1: Outputs 0 if address is within specified address area
P42	1	I/O	Port 42: I/O port (with pull-up resistor)
$\overline{CS2}$		Output	Chip Select 2: Outputs 0 if address is within specified address area
P43	1	I/O	Port 43: I/O port (with pull-up resistor)
$\overline{CS3}$		Output	Chip Select 3: Outputs 0 if address is within specified address area
P50 to P57	8	Input	Port 5: Pin used to input port
AN0 to AN7		Input	Analog input: Pin used to input to AD converter
$\overline{ADTRG}$		Input	AD Trigger: Signal used to request start of AD converter
P60	1	I/O	Port 60: I/O port
SCK		I/O	Serial bus interface clock in SIO Mode
P61	1	I/O	Port 61: I/O port
SO		Output	Serial bus interface output data in SIO Mode
SDA		I/O	Serial bus interface data in I^2C bus Mode
P62	1	I/O	Port 62: I/O port
SI		Input	Serial bus interface input data in SIO Mode
SCL		I/O	Serial bus interface clock in I^2C bus Mode
P63	1	I/O	Port 63: I/O port
INT0		Input	Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64	1	I/O	Port 64: I/O port
SCOUT		Output	System Clock Output: Outputs f_{FPH} or fs clock.

Table 2.2.1 Pin Names and Functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P65	1	I/O	Port 65: I/O port
P66	1	I/O	Port 66: I/O port
P70 TA0IN	1	I/O Input	Port 70: I/O port Timer A0 Input
P71 TA1OUT	1	I/O Output	Port 71: I/O port Timer A1 Output
P72 TA3OUT	1	I/O Output	Port 72: I/O port Timer A3 Output
P73 TA4IN	1	I/O Input	Port 73: I/O port Timer A4 Input
P74 TA5OUT	1	I/O Output	Port 74: I/O port Timer A5 Output
P75 TA7OUT	1	I/O Output	Port 75: I/O port Timer A7 Output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port Timer B0 Input 0 Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge.
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port Timer B0 Input 1 Interrupt Request Pin 6: Interrupt request on rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port Timer B0 Output 0
P83 TB0OUT1	1	I/O Output	Port 83: I/O port Timer B0 Output 1
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O port Timer B1 Input 0 Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge.
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O port Timer B1 Input 1 Interrupt Request Pin 8: Interrupt request on rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O port Timer B1 Output 0
P87 TB1OUT1	1	I/O Output	Port 87: I/O port Timer B1 Output 1
P90 TXD0	1	I/O Output	Port 90: I/O port Serial Send Data 0 (Programmable open-drain)
P91 RXD0	1	I/O Input	Port 91: I/O port Serial Receive Data 0
P92 SCLK0 $\overline{CTS0}$	1	I/O I/O Input	Port 92: I/O port Serial Clock I/O 0 Serial Data Send Enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial Send Data 1 (Programmable open-drain)
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial Receive Data 1
P95 SCLK1 $\overline{CTS1}$	1	I/O I/O Input	Port 95: I/O port (with pull-up resistor) Serial Clock I/O 1 Serial Data Send Enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (Open-drain output) Low-frequency oscillator connection pin

Table 2.2.1 Pin Names and Functions (3/3)

Pin Name	Number of Pins	I/O	Functions
P97 XT2	1	I/O Output	Port 97: I/O port (Open-drain output) Low-frequency oscillator connection pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Ports A0 to A3: I/O ports Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge.
PA4 to PA7	4	I/O	Ports A4 to A7: I/O ports
ALE	1	Output	Address Latch Enable Can be disabled to reduce noise.
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge.
AM0 to 1	2	Input	Address Mode: The Vcc pin should be connected.
EMU0/EMU1	1	Output	Test Pins: Open pins
$\overline{\text{RESET}}$	1	Input	Reset: initializes TMP91CW12A. (With pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1	I/O	High-frequency oscillator connection pins
AVSS	1		Power supply pin for AD converter
X1/X2	2		GND pin for AD converter (0 V)
DVCC	3		Power supply pins (All VCC pins should be connected with the power supply pin.)
DVSS	3		GND pins (0 V) (All VSS pins should be connected with the power supply pin.)

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

3. Operation

This section describes the basic components, functions and operation of the TMP91CW12AF.

3.1 CPU

The TMP91CW12AF incorporates a high-performance 16-bit CPU (the 900/L1 CPU). For a description of this CPU's operation, please refer to the section of this data book which describes the TLCS-900/L1 CPU.

The following sub-sections describe functions peculiar to the CPU used in the TMP91CW12AF; these functions are not covered in the section devoted to the TLCS-900/L1 CPU.

3.1.1 Reset

When resetting the TMP91CW12AF microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input Low for at least 10 system clocks (ten states: 80 μs at 4 MHz).

When the Reset has been accepted, the CPU performs the following:

- Sets the Program Counter (PC) as follows in accordance with the Reset Vector stored at address FFFF00H to FFFF02H:

  PC<0 to 7> ← Data in location FFFF00H
  PC<8 to 15> ← Data in location FFFF01H
  PC<16 to 23> ← Data in location FFFF02H
- Sets the Stack Pointer (XSP) to 100H.
- Sets bits <IFF0 to IFF2> of the Status Register (SR) to 111 (thereby setting the Interrupt Level Mask Register to level 7).
- Sets the <MAX> bit of the Status Register to 1 (MAX Mode).
- Clears bits <RFP0 to RFP2> of the Status Register to 000 (thereby selecting Register Bank 0).

When the Reset is cleared, the CPU starts executing instructions according to the Program Counter settings. CPU internal registers not mentioned above do not change when the Reset is cleared.

When the Reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to General-Purpose Input or Output Port Mode.
- Sets the ALE pin to High-Z.

Note 1: Except PC,SR and XSP register of CPU and data of internal RAM are not change by reset operation.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91CW12AF.

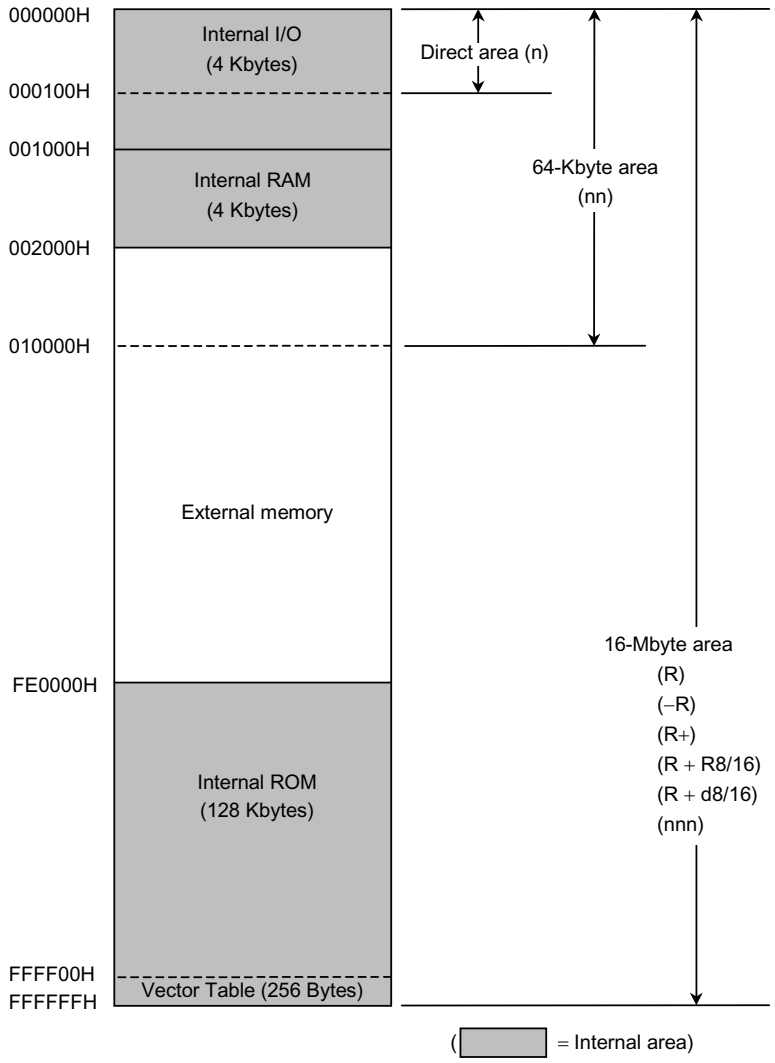


Figure 3.2.1 Memory Map

3.3 Differences Between TMP91CW12AF and TMP91CW12F

(1) Outline

TMP91CW12AF is a high-speed and low-voltage products of TMP91CW12F.

The specification of function is added following item to TMP91CW12F.

The major difference points of A, C and D, C characteristics are operation voltage (CW12F: 5 V/3 V, CW12AF: 3 V/2 V) and Fmax (CW12F: 16 MHz, CW12AF:27 MHz) at 3 V.

For the details, please refer to 4.Electrical Characteristics.

(2) Differences of Function

3.3.1 CS/WAIT controller

Wait operation setting is added in order to high-speed of operation frequency on TMP91CW12AF. It is explained at Table 3.3.1.

Figure 3.3.1 shows SFR setting.

Table 3.3.1 Wait operation settings

<BxW2 to BxW0>	No. of Waits	Wait Operation
000	2 waits	Inserts a wait of two states, irrespective of the $\overline{\text{WAIT}}$ pin state.
001	1 wait	Inserts a wait of one state, irrespective of the $\overline{\text{WAIT}}$ pin state.
010	1 wait + N	Inserts one wait state, then continuously samples the state of the $\overline{\text{WAIT}}$ pin. While the $\overline{\text{WAIT}}$ pin remains Low, the wait continues; the the bus cycle is prolonged until the pin goes High.
011	0 waits	Ends the bus cycle without a wait, regardless of the $\overline{\text{WAIT}}$ pin state.
100	Reserved	Don't setting
101	3 waits	Inserts a wait of three states, irrespective of the $\overline{\text{WAIT}}$ pin state.
110	4 waits	Inserts a wait of four states, irrespective of the $\overline{\text{WAIT}}$ pin state.
111	8 waits	Inserts a wait of eight states, irrespective of the $\overline{\text{WAIT}}$ pin state.

Chip Select/Wait Control Register

		7	6	5	4	3	2	1	0
B0CS (00C0H)	Bit symbol	B0E		B0OM1	B0OM0	B0BUS	B0W2	B0W1	B0W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
Read-Modify-Write instructions are prohibited.	Function	Chip Select Set up 0: Disable 1: Enable		Chip Select output waveform selection 00: For ROM/SRAM 01: } Reserved 10: } 11: }		Data bus width 0: 16 bits 1: 8 bits	Number of Waits 000: 2 waits 001: 1 wait 010: 1 wait + N 011: 0 waits	 100: Reserved 101: 3 waits 110: 4 waits 111: 8 waits	
B1CS (00C1H)	Bit symbol	B1E		B1OM1	B1OM0	B1BUS	B1W2	B1W1	B1W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
Read-Modify-Write instructions are prohibited.	Function	Chip Select Set up 0: Disable 1: Enable		Chip Select output waveform selection 00: For ROM/SRAM 01: } Reserved 10: } 11: }		Data bus width 0: 16 bits 1: 8 bits	Number of Waits 000: 2 waits 001: 1 wait 010: 1 wait + N 011: 0 waits	 100: Reserved 101: 3 waits 110: 4 waits 111: 8 waits	
B2CS (00C2H)	Bit symbol	B2E	B2M	B2OM1	B2OM0	B2BUS	B2W2	B2W1	B2W0
	Read/Write	W							
	After reset	1	0	0	0	0	0	0	0
Read-Modify-Write instructions are prohibited.	Functions	Chip Select Set up 0: Disable 1: Enable	CS2 area selection 0: 16-Mbyte area 1: CS area	Chip Select output waveform selection 00: For ROM/SRAM 01: } Reserved 10: } 11: }		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: 1 wait + N 011: 0 waits	 100: Reserved 101: 3 waits 110: 4 waits 111: 8 waits	
B3CS (00C3H)	Bit symbol	B3E		B3OM1	B3OM0	B3BUS	B3W2	B3W1	B3W0
	Read/Write	W		W					
	After reset	0		0	0	0	0	0	0
Read-Modify-Write instructions are prohibited.	Function	Chip Select Set up 0: Disable 1: Enable		Chip Select output waveform selection 00: For ROM/SRAM 01: } Reserved 10: } 11: }		Data bus width 0: 16 bits 1: 8 bits	Number of waits 000: 2 waits 001: 1 wait 010: 1 wait+ N 011: 0 waits	 100: Reserved 101: 3 waits 110: 4 waits 111: 8 waits	
BEXCS (00C7H)	Bit symbol					BEXBUS	BEXW2	BEXW1	BEXW0
	Read/Write					0			
	After reset					0	0	0	0
Read-Modify-Write instructions are prohibited.	Function					Data bus width 0: 16 bits 1: 8 bits	Number of Waits 000: 2 waits 001: 1 waits 010: 1 wait + N 011: 0 waits	 100: Reserved 101: 3 waits 110: 4 waits 111: 8 waits	

Master enable bit

0	Prohibit
1	Permission

CS2 area selection

0	16-Mbyte area
1	Specified address area

Chip select output waveform selection

00	For ROM/SRAM
01 10 11	Reserved

Number of address area waits
(See 3.3.1 Wait Control.)

Data bus width selection

0	16-bit data bus
1	8-bit data bus

Figure 3.3.1 Chip Select/Wait Control Registers

3.3.2 IrDA function

The SIRCR<RXSEL> register is added. This register can be the selection the logic of recieving data from external IrDA module.

Figure 3.3.3 shows SFR setting.

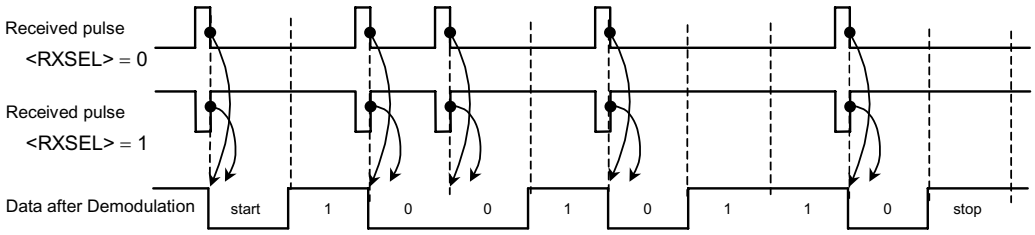


Figure 3.3.2 Demodulation of Received data

SIRCR (0207H)

	7	6	5	4	3	2	1	0
Bit symbol	PLSEL	RXSEL	TXEN	RXEN	SIRWD3	SIRWD2	SIRWD1	SIRWD0
Read/Write	R/W							
After reset	0	0	0	0	0	0	0	0
Function	Select transmit pulse width 0: 3/16 1: 1/16	Received Data 0: H pulse 1: L	Transmit 0: disable 1: enable	Receive 0: disable 1: enable	Select receive pulse width Set effective pulse width for equal or more than 2x × x (value + 1) Values in the range 1 to 14 can be set			

Select receive pulse width

Formula: Effective pulse width ≥ 2x × x (value + 1)

$x = 1/f_{FPH}$

0000	Cannot be set
0001	Equal or more than 4x + 100 ns
to	
1110	Equal or more than 30x + 100 ns
1111	Can not be set

Receive operation

0	Disabled
1	Enabled

Transmit operation

0	Disabled
1	Enabled

Select transmit pulse width

0	3/16
1	1/16

Note: When the baud rate is slow and the IrDA1.0-specified pulse width (minimum: 1.6 μs) can be secured, setting this bit to 1 enables infrared light-up time to be decreased reducing power consumption.

Figure 3.3.3 IrDA Control Register

3.3.3 Clock Doubler (DFM) function

Input frequency range to DFM (frequency of high-frequency oscillator) is different from TMP91CW12.

Therefore, the DFMCR1 register is added to select frequency-range. (DFMCR1 register don't exist in TMP91CW12)

Write the following data according to the operating condition before starting lock-up.

DFMCR1 (00E9H)

	7	6	5	4	3	2	1	0
Bit symbol								
Read/Write	R/W							
After reset	0	0	0	1	0	0	1	1
Function	Write 0BH when the f_{OSCH} = 4 to 6.75 MHz at Vcc = 3 V ±10% Write 1BH when the f_{OSCH} = 2 to 2.5 MHz at Vcc = 2 V ±10%							

Figure 3.3.4 DFM Control Register 1

3.3.4 Others

(1) Limitation of selecting drivability of High-frequency oscillator

The case of V_{CC} = 2.0 V ± 10%, it is impossible to use selecting function of drivability of High-frequency oscillator.

Do not write 0 to EMCCR0<DRVOSCH>.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 4.0	V
Input Voltage	VIN	−0.5 to Vcc + 0.5	V
Output Current	IOL	2	mA
Output Current	IOH	−2	mA
Output Current (total)	ΣIOL	80	mA
Output Current (total)	ΣIOH	−80	mA
Power Dissipation (Ta = 85°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	−65 to 150	°C
Operating Temperature	TOPR	−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition		Min	Typ. (Note1)	Max	Unit
Power Supply Voltage (AVcc = DVcc) (AVss = DVss = 0 V)		VCC	fc = 4 to 27 MHz	fs = 30 to 34 kHz	2.7		3.6	V
			fc = 2 to 10 MHz		1.8			
Input Low Voltage	P00 to P17 (AD0 to 15)	V_{IL}	Vcc ≥ 2.7 V		−0.3		0.6	V
			Vcc < 2.7 V				0.2 Vcc	
	P20 to PA7 (except P63)	V_{IL1}	Vcc ≥ 2.7 V				0.3 Vcc	
			Vcc < 2.7 V				0.2 Vcc	
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IL2}	Vcc ≥ 2.7 V				0.25 Vcc	
			Vcc < 2.7 V				0.15 Vcc	
	AM0, 1	V_{IL3}	Vcc ≥ 2.7 V				0.3	
			Vcc < 2.7 V				0.3	
	X1	V_{IL4}	Vcc ≥ 2.7 V				0.2 Vcc	
			Vcc < 2.7 V				0.1 Vcc	
Input High Voltage	P00 to P17 (AD0 to 15)	V_{IH}	Vcc ≥ 2.7 V		2.0		Vcc + 0.3	
			Vcc < 2.7 V		0.7 Vcc			
	P20 to PA7 (except P63)	V_{IH1}	Vcc ≥ 2.7 V		0.7 Vcc			
			Vcc < 2.7 V		0.8 Vcc			
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IH2}	Vcc ≥ 2.7 V		0.75 Vcc			
			Vcc < 2.7 V		0.85 Vcc			
	AM0, 1	V_{IH3}	Vcc ≥ 2.7 V		Vcc−0.3			
			Vcc < 2.7 V		Vcc−0.3			
	X1	V_{IH4}	Vcc ≥ 2.7 V		0.8 Vcc			
			Vcc < 2.7 V		0.9 Vcc			
Output Low Voltage		V_{OL}	IOL = 1.6mA	Vcc ≥ 2.7 V			0.45	V
			IOL = 0.4mA	Vcc < 2.7 V			0.15 Vcc	
Output High Voltage		V_{OH}	IOH = −400 μA	Vcc ≥ 2.7 V	2.4			
			IOH = −200 μA	Vcc < 2.7 V	0.8 Vcc			

Note1: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note1)	Max	Unit
Input Leakage Current	ILI	$0.0 \leq V_{IN} \leq Vcc$		0.02	±5	μA
Output Leakage Current	ILO	$0.2 \leq V_{IN} \leq Vcc - 0.2$		0.05	±10	
Power Down Voltage (at STOP, RAM back-up)	VSTOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	1.8		3.6	V
$\overline{RESET}$ Pull-up Resistor	RRST	Vcc = 3 V ± 10%	100		400	KΩ
		Vcc = 2 V ± 10%	200		1000	
Pin Capacitance	CIO	fc = 1 MHz			10	PF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	VTH	Vcc ≥ 2.7 V	0.4	1.0		V
		Vcc < 2.7 V	0.3	0.8		
Programmable Pull-up Resistor	RKH	Vcc = 3 V ± 10%	100		400	KΩ
		Vcc = 2 V ± 10%	200		1000	
Normal (Note 2)	Icc	Vcc = 3 V ± 10% fc = 27 MHz		7.0	10.0	mA
Idle2				2.5	3.5	
Idle1				1.0	1.8	
Normal (Note 2)		Vcc = 2 V ± 10% fc = 10 MHz (Typ.: Vcc = 2.0 V)		1.7	2.5	mA
Idle2				0.6	0.9	
Idle1				0.25	0.4	
Slow (Note 2)		Vcc = 3 V ± 10% fs = 32.768 kHz		11.6	30	μA
Idle2				5.2	19	
Idle1		Ta ≤ 70°C		3.0	8	
		Ta ≤ 85°C			15	
Slow (Note 2)		Vcc = 2 V ± 10% fs = 32.768 kHz (Typ.: Vcc = 2.0 V)		7.7	20	μA
Idle2				3.5	13	
Idle1				2.0	10	
Stop		Vcc = 1.8 to 3.3V		0.1	10	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

Note 2: Icc measurement conditions (Normal, Slow):
All functions are operating; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10%

No.	Symbol	Parameter	Variable		f_{FPH} = 27 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} Period (= x)	37.0	31250	37.0		ns
2	t_{AL}	A0 to A15 Vaild → ALE Fall	0.5x – 6		12		ns
3	t_{LA}	ALE Fall → A0 to A15 Hold	0.5x – 16		2		ns
4	t_{LL}	ALE High Width	x – 20		17		ns
5	t_{LC}	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	0.5x – 14		4		ns
6	t_{CLR}	$\overline{RD}$ Rise → ALE Rise	0.5x – 10		8		ns
7	t_{CLW}	$\overline{WR}$ Rise → ALE Rise	x – 10		27		ns
8	t_{ACL}	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	x – 23		14		ns
9	t_{ACH}	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	1.5x – 26		29		ns
10	t_{CAR}	$\overline{RD}$ Rise → A0 to A23 Hold	0.5x – 13		5		ns
11	t_{CAW}	$\overline{WR}$ Rise → A0 to A23 Hold	x – 13		24		ns
12	t_{ADL}	A0 to A15 Valid → D0 to D15 Input		3.0x – 38		73	ns
13	t_{ADH}	A0 to A23 Valid → D0 to D15 Input		3.5x – 41		88	ns
14	t_{RD}	$\overline{RD}$ Fall → D0 to D15 Input		2.0x – 30		44	ns
15	t_{RR}	$\overline{RD}$ Low Width	2.0x – 15		59		ns
16	t_{HR}	$\overline{RD}$ Rise → D0 to A15 Hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ Rise → A0 to A15 Output	x – 15		22		ns
18	t_{WW}	$\overline{WR}$ Low Width	1.5x – 15		40		ns
19	t_{DW}	D0 to D15 Valid → $\overline{WR}$ Rise	1.5x – 35		20		ns
20	t_{WD}	$\overline{WR}$ Rise → D0 to D15 Hold	x – 25		12		ns
21	t_{AWH}	A0 to A23 Valid → $\overline{WAIT}$ Input [1 WAIT +n Mode]		3.5x – 60		69	ns
22	t_{AWL}	A0 to A15 Valid → $\overline{WAIT}$ Input [1 WAIT +n Mode]		3.0x – 50		61	ns
23	t_{CW}	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold [1 WAIT +n Mode]	2.0x + 0		74		ns
24	t_{APH}	A0 to A23 Valid → Port Input		3.5x – 89		40	ns
25	t_{APH2}	A0 to A23 Valid → Port Hold	3.5x		129		ns
26	t_{AP}	A0 to A23 Valid → Port Valid		3.5x + 80		209	ns

AC Measuring Conditions

- Output Level: High = 0.7 × Vcc, Low = 0.3 × Vcc, CL = 50 pF
- Input Level: High = 0.9 × Vcc, Low = 0.1 × Vcc

Note: x used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>.
The value of x changes according to whether a clock gear or a low-speed oscillator is selected.
An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR2 to 0> = 0000).

(2) Vcc = 2.0 V ± 10%

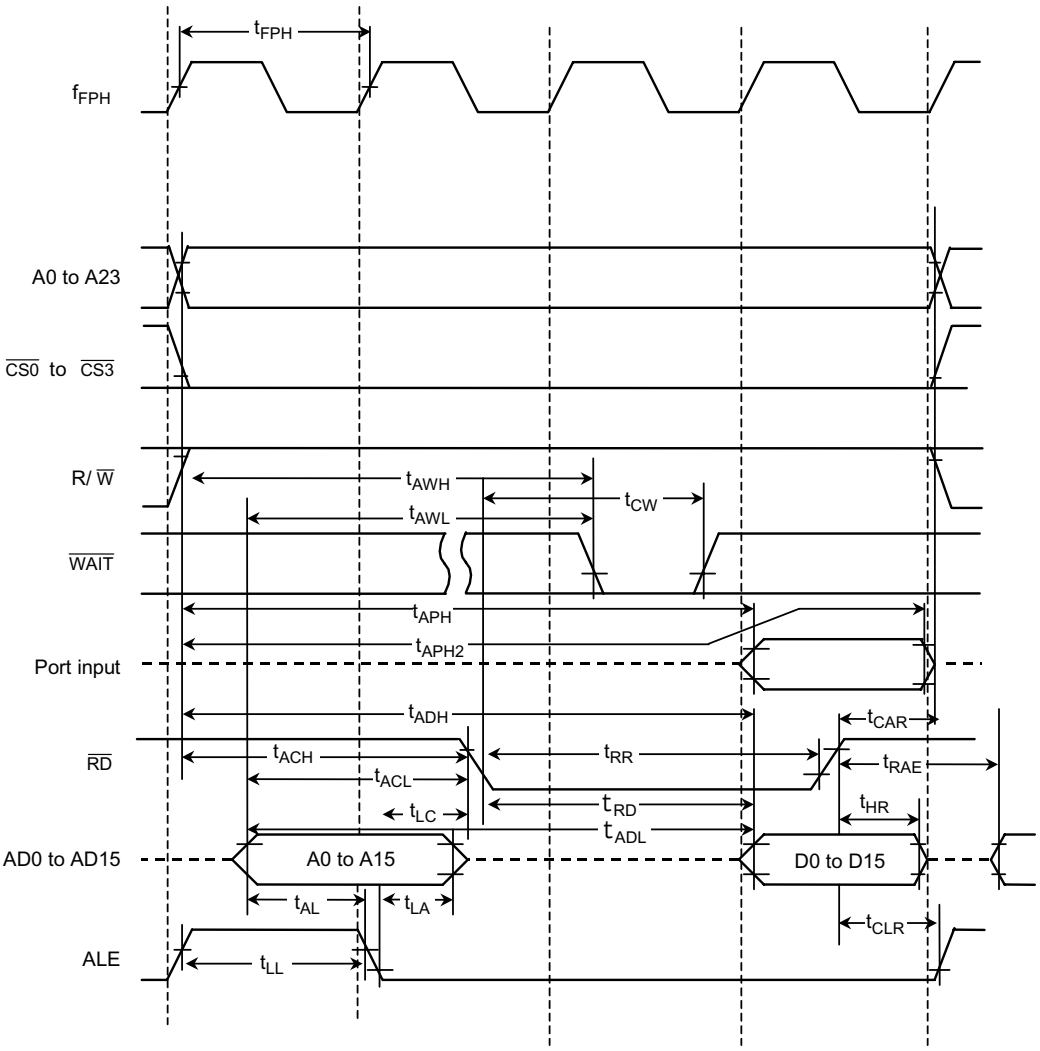
No.	Symbol	Parameter	Variable		f_{FPH} = 10 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} Period (= x)	100	31250	100		ns
2	t_{AL}	A0 to A15 → ALE Fall	0.5 x – 28		22		ns
3	t_{LA}	ALE Fall → A0 to A15 Hold	0.5 x – 35		15		ns
4	t_{LL}	ALE High Width	x – 40		60		ns
5	t_{LC}	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	0.5x – 28		22		ns
6	t_{CLR}	$\overline{RD}$ Rise → ALE Rise	0.5x – 20		30		ns
7	t_{ACW}	$\overline{WR}$ Rise → ALE Rise	x – 20		80		ns
8	t_{ACL}	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	x – 75		25		ns
9	T_{ACH}	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	1.5x –70		80		ns
10	t_{CAR}	$\overline{RD}$ Rise → A0 to A23 Hold	0.5x – 30		20		ns
11	T_{CAW}	$\overline{WR}$ Rise → A0 to A23 Hold	x – 30		70		ns
12	t_{ADL}	A0 to A15 Valid → D0 to D15 Input		3.0x – 76		224	ns
13	t_{ADH}	A0 to A23 Valid → D0 to D15 Input		3.5x – 82		268	ns
14	T_{RD}	$\overline{RD}$ Fall → D0 to D15 Input		2.0x – 60		140	ns
15	t_{RR}	$\overline{RD}$ Low Width	2.0x – 30		170		ns
16	t_{HR}	$\overline{RD}$ Rise → D0 to D15 Hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ Rise → A0 to A15 Output	x – 30		70		ns
18	t_{WW}	$\overline{WR}$ Low Width	1.5 x – 30		120		ns
19	t_{DW}	D0 to D15 Valid → $\overline{WR}$ Rise	1.5 x – 70		80		ns
20	t_{WD}	$\overline{WR}$ Rise →D0 to D15 Hold	x – 50		50		ns
21	t_{AWH}	A0 to A23 Valid → $\overline{WAIT}$ Input [1WAIT +n mode]		3.5x – 120		230	ns
22	t_{AWL}	A0 to A15 Valid → $\overline{WAIT}$ Input [1WAIT +n mode]		3.0x – 100		200	ns
23	t_{CW}	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold [1WAIT +n mode]	2.0x + 0		200		ns
24	t_{APH}	A0 to A23 Valid → Port Input		3.5x – 170		180	ns
25	t_{APH2}	A0 to A23 Valid → Port Hold	3.5x		350		ns
26	t_{AP}	A0 to A23 Valid → Port Valid		3.5x + 170		520	ns

AC Measuring Conditions

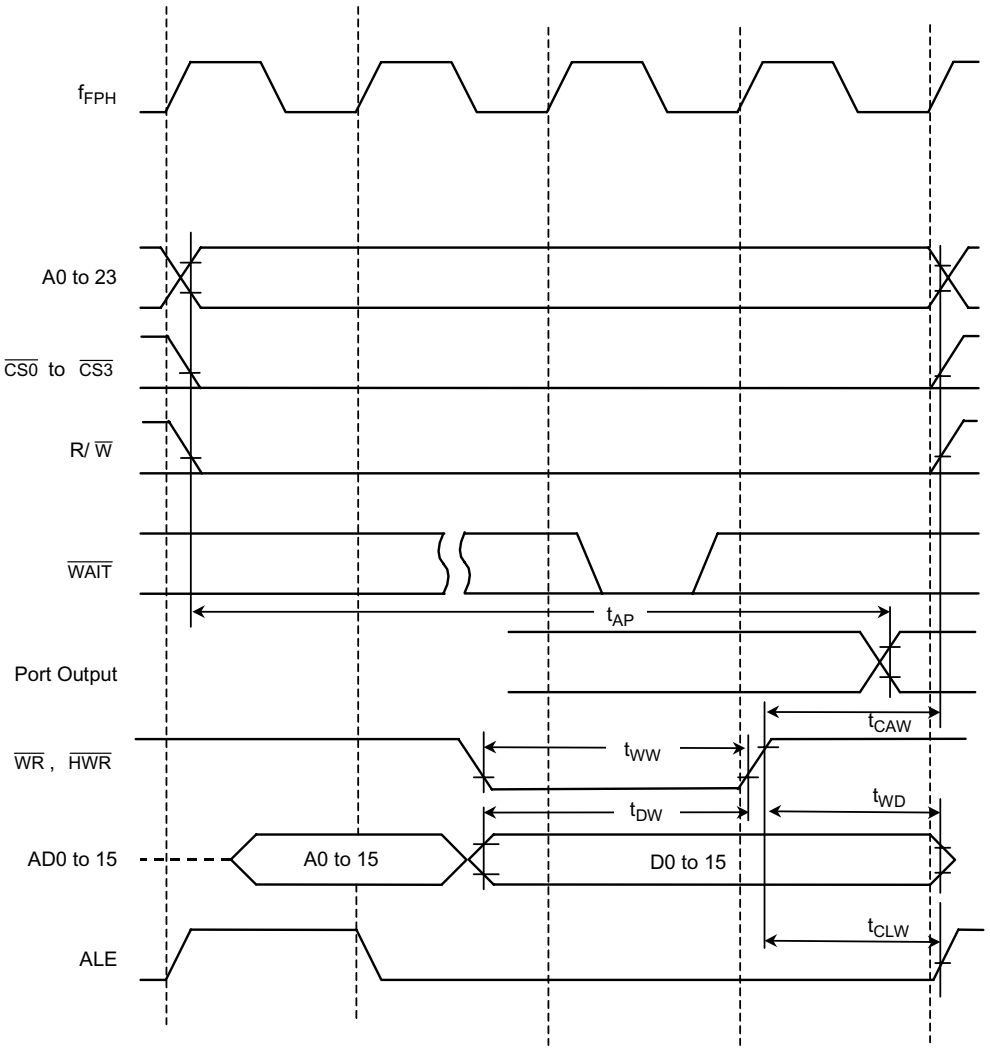
- Output Level: High = 0.7 × Vcc, Low = 0.3 × Vcc, CL = 50 pF
- Input Level: High = 0.9 × Vcc, Low = 0.1 × Vcc

Note: x used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>.
The value of x changes according to whether a clock gear or a low-speed oscillator is selected.
An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR2 to 0> = 0000).

(3) Read Cycle


t_{FPH}
f_{FPH}
A0 to A23
$\overline{CS0}$ to $\overline{CS3}$
R/$\overline{W}$
t_{AWH}
t_{CW}
t_{AWL}
$\overline{WAIT}$
t_{APH}
t_{APH2}
Port input
t_{ADH}
t_{CAR}
$\overline{RD}$
t_{ACH}
t_{RR}
t_{RAE}
t_{ACL}
t_{LC}
t_{RD}
t_{HR}
t_{ADL}
AD0 to AD15
A0 to A15
D0 to D15
t_{AL}
t_{LA}
t_{CLR}
ALE
t_{LL}

(4) Write Cycle



4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	VREFH	V_{CC} = 3 V ± 10%	V_{CC} − 0.2 V	Vcc	Vcc	V
		V_{CC} = 2 V ± 10%	V_{CC}	Vcc	Vcc	
Analog Reference Voltage (−)	VREFL	V_{CC} = 3 V ± 10%	V_{SS}	Vss	Vss + 0.2 V	
		V_{CC} = 2 V ± 10%	V_{SS}	Vss	Vss	
Analog Input Voltage Range	VAIN		V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage <VREFON> = 1	IREF (VREFL = 0V)	V_{CC} = 3 V ± 10%		0.94	1.20	mA
		V_{CC} = 2 V ± 10%		0.65	0.90	
<VREFON> = 0		V_{CC} = 1.8 V to 3.3 V		0.02	5.0	μA
Error (not including quantizing errors)	−	V_{CC} = 3 V ± 10%		±1.0	±4.0	LSB
		V_{CC} = 2 V ± 10%		±1.0	±4.0	

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Interface Mode)

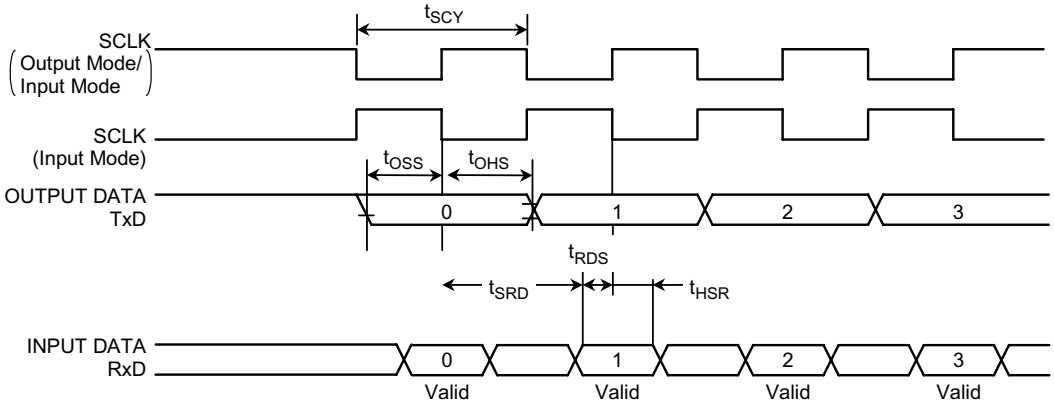
(1) SCLK Input Mode

Parameter		Symbol	Variable		10 MHz		27 MHz		Unit
			Min	Max	Min	Max	Min	Max	
SCLK Period		t_{SCY}	16X		1.6		0.59		μs
Output Data →SCLK Rising/Falling Edge*	Vcc = 3V ± 10%	t_{OSS}	$t_{SCY}/2 - 4X - 110$		290		38		ns
	Vcc = 2V ± 10%		$t_{SCY}/2 - 4X - 180$		220		–		ns
SCLK Rising/Falling Edge* → Output Data Hold		t_{OHS}	$t_{SCY}/2 + 2X + 0$		1000		370		ns
SCLK Rising/Falling Edge* → Input Data Hold		t_{HSR}	3X + 10		310		121		ns
SCLK Rising/Falling Edge* → Valid Data Input		t_{SRD}		$t_{SCY} - 0$		1600		592	ns
Valid Data Input → SCLK Rising/Falling Edge*		t_{RDS}	0		0		0		ns

(2) SCLK Output Mode

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period	t_{SCY}	16X	8192X	1.6	819	0.59	303	μs
Output Data → SCLK Rising /Falling Edge*	t_{OSS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising/Falling Edge* → Output Data Hold	t_{OHS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising/Falling Edge* → Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising/Falling Edge* → Valid Data Input	t_{SRD}		$t_{SCY} - 1X - 180$		1320		375	ns
Valid Data Input → SCLK Rising/Falling Edge*	t_{RDS}	1X + 180		280		217		ns

Note: SCLK Rinsing/Falling Edge: The rising edge is used in SCLK Rising Mode.
The falling edge is used in SCLK Falling Mode.
27 MHz and 10 MHz values are calculated from t_{SCY} = 16X case.



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Perild	t_{VCK}	8X + 100		900		396		ns
Clock Low Level Width	t_{VCKL}	4X + 40		440		188		ns
Clock High Level Width	t_{VCKH}	4X + 40		440		188		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 to INT4 Interrupts

Symbol	Parameter	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 to INT4 Low level width	4X + 40		440		188		ns
t_{INTAH}	$\overline{NMI}$, INT0 to INT4 High level width	4X + 40		440		188		ns

(2) INT5 to INT8 Interrupts, Capture

The INT5 to INT8 input width depends on the system clock and prescaler clock settings.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1, PRCK0>	t_{INTBL} (INT5 to INT8 Low level Width)		t_{INTBH} (INT5 to INT8 High Level Width)		Unit
		Variable	f_{FPH} = 27 MHz	Variable	f_{FPH} = 27 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	396	8X + 100	396	ns
	10 (fc/16)	128Xc + 0.1	4.8	128Xc + 0.1	4.8	μs
1 (fs)	00 (f_{FPH})	8X + 0.1	244.3	8X + 0.1	244.3	

Note: Xc = Period of Clock fc

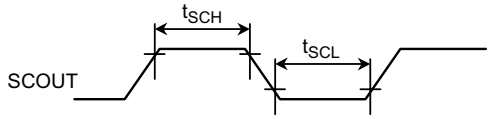
4.8 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		10 MHz		27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Low level Width	t_{SCH}	0.5T – 13		37		5		Vcc ≥ 2.7 V	ns
		0.5T – 25		25		–		Vcc < 2.7 V	
High level Width	t_{SCL}	0.5T – 13		37		5		Vcc ≥ 2.7 V	ns
		0.5T – 25		25		–		Vcc < 2.7 V	

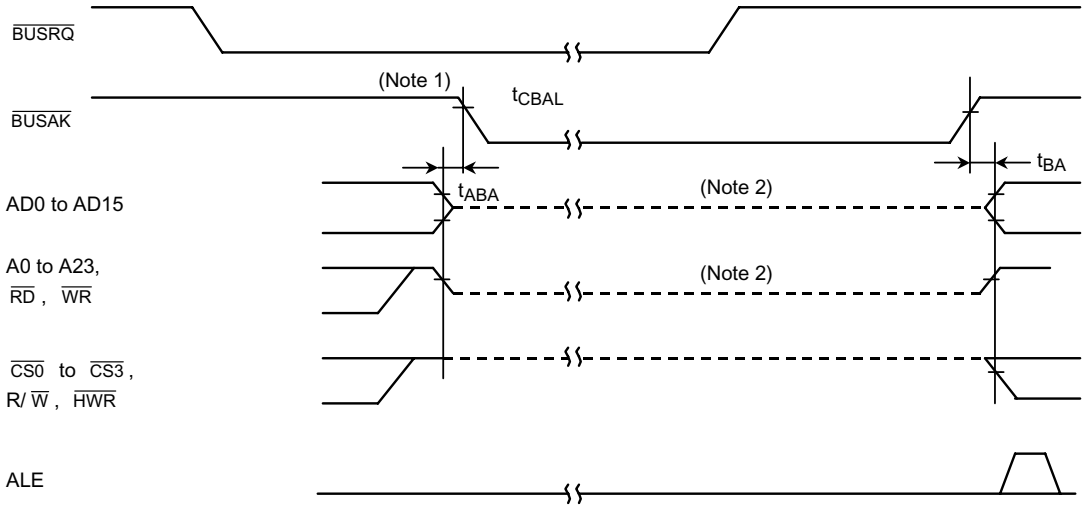
Note: T = Period of SCOUT

Measrement Condition

- Output Level: High 0.7 Vcc/Low 0.3 Vcc, CL = 10pF



4.9 Bus Request/Bus Acknowledge



Paramter	Symbol	Variable		f_{FPH} = 10 MHz		f_{FPH} = 27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Output Buffer Off to $\overline{BUSAK}$ Low	t_{ABA}	0	80	0	80	0	80	Vcc ≥ 2.7 V	ns
		0	300	0	300	0	300	Vcc < 2.7 V	
$\overline{BUSAK}$ High to Output Buffer On	t_{BAA}	0	80	0	80	0	80	Vcc ≥ 2.7 V	ns
		0	300	0	300	0	300	Vcc < 2.7 V	

Note 1: Even if the $\overline{BUSRQ}$ Signal goes Low, the bus will not be released while the $\overline{WAIT}$ signal is Low. The bus will only be released when $\overline{BUSRQ}$ goes Low while $\overline{WAIT}$ is High.

Note 2: This line shows only that the output buffer is in the Off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resister during bus release, careful design is necessary, since fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the Active and Non-Active states by the internal signal.

4.10 Recommended Oscillation Circuit

The TMP91CW12AF has been evaluated by the following resonator manufacturer. The evaluation results are shown below for your information.

Note: The load capacitance of the oscillation terminal is the sum of the load capacitances of C1 and C2 to be connected and the stray capacitance on the board. Even if the ratings of C1 and C2 are used, the load capacitance varies with each board and the oscillator may malfunction. Therefore, when designing a board, make the pattern around the oscillation circuit shortest. It is recommended that final evaluation of the resonator be performed on the board.

(1) Examples of resonator connection

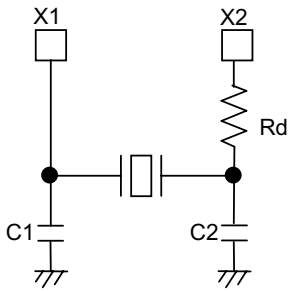


Figure 4.10.1 High-frequency Oscillator Connection

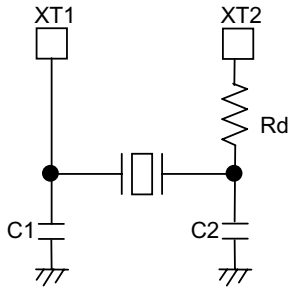


Figure 4.10.2 Low-frequency Oscillator Connection

(2) Recommended ceramic resonators for the TMP91CW12AF: Murata Manufacturing Co., Ltd.

Ta = −40 to 85°C

Item	Oscillation frequency [MHz]	Recommended resonator	Recommended rating			VCC[V]	Remarks
			C1[pF]	C2[pF]	Rd[kΩ]		
High-frequency oscillator	2.0	CSA2.00MG042	100	100	0	1.8 to 2.2	–
		CST2.00MG042	(100)	(100)			
	2.5	CSA2.50MG042	100	100			
		CST2.50MGW042	(100)	(100)			
	4.0	CSA4.00MG040	100	100		2.7 to 3.3	
		CST4.00MGW040	(100)	(100)			
		CSTS0400MG06	(47)	(47)			
		CSA4.00MGU040	100	100		1.8 to 2.2	
		CST4.00MGWU040	(100)	(100)			
	6.75	CSA6.75MTZ040	100	100		2.7 to 3.3	
		CST6.75MTW040	(100)	(100)			
		CSTS0675MG06	(47)	(47)			
		CSA6.75MTZ093	30	30		1.8 to 2.2	
		CST6.75MTW093	(30)	(30)			
	10.0	CSA10.0MTZ	30	30		2.7 to 3.3	
		CST10.0MTW	(30)	(30)			
		CSA10.0MTZ093	30	30		1.8 to 2.2	
		CST10.0MTW093	(30)	(30)			
	12.5	CSA12.5MTZ	30	30		2.7 to 3.3	
		CST12.5MTW	(30)	(30)			
	20.0	CSA20.00MXZ040	7	7			
	27.0	CSA27.00MXZ040	5	5			
		CST27.00MXW040	(5)	(5)			

- The values enclosed in brackets in the C1 and C2 columns apply to the condenser built-in type.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
  http://www.murata.co.jp/search/index.html