

0.5- μm 2MI Process Cross Section

General Description

The 0.5- μm Heterostructure FET (HFET) process is a depletion-mode 2MI (2-metal-interconnect) process for applications through 20 GHz. The HFET I-V characteristics provide for high power, high linearity, extraordinary transconductance uniformity and high breakdown voltages. Passives include 2 thick-metal interconnect layers, precision TaN resistors, GaAs resistors, MIM capacitors and through-substrate vias. The capacitor-over-via process aides in size compaction and offers excellent grounds at higher frequencies.

Features

- 0.5- μm amplifier transistors
- 0.5- μm switch transistors
- 0.5- μm diodes
- Device passivation
- High-Q passives
- MIM capacitors
- TaN resistors
- GaAs resistors
- 2 metal layers
- Air bridges
- Substrate vias
- Operation up to $V_d = 10\text{ V}$

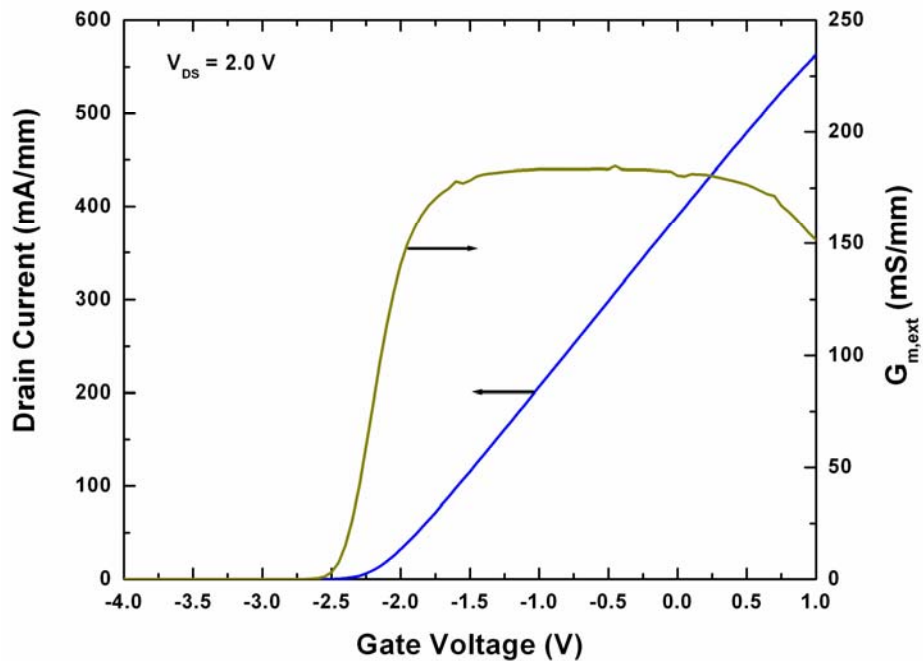
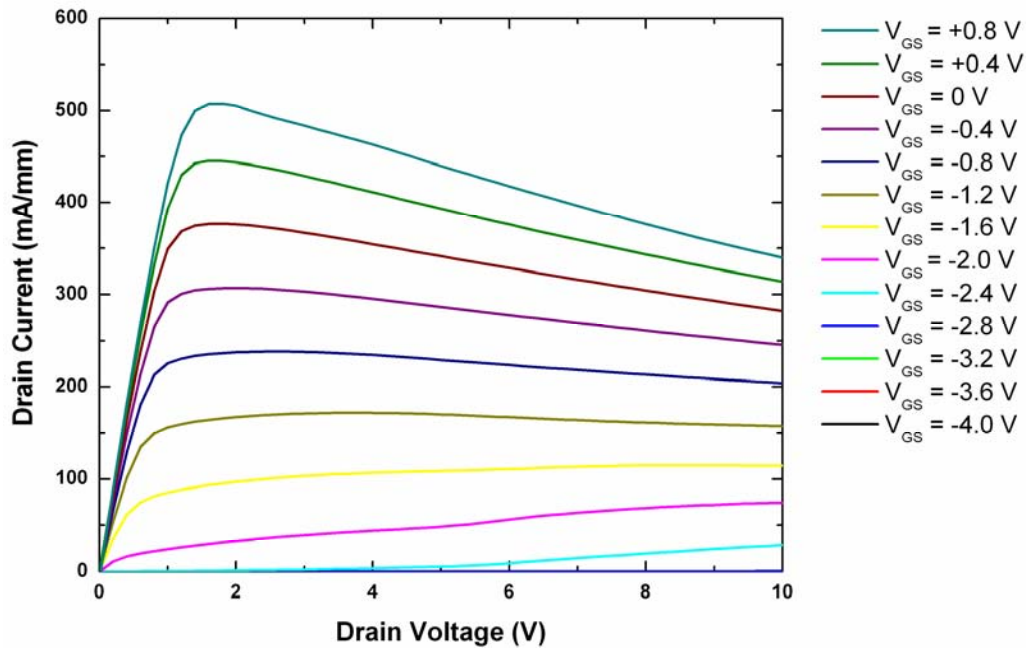
Applications

- Up to 20 GHz
- Communications
- Space
- Military
- Power amplifiers
- Driver amplifiers
- AGC amplifiers
- Limiting amplifiers
- Transimpedance amplifiers
- Differential amplifiers

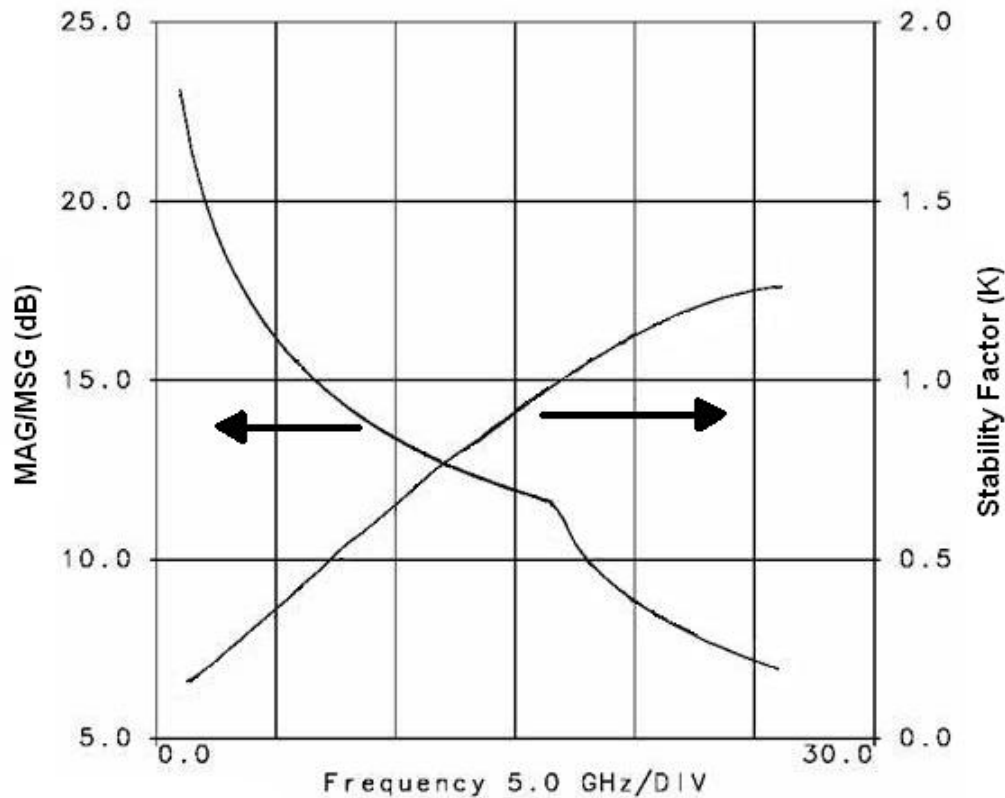
0.5- μm HFET Process Details			
Element	Parameter	Typical Value	Units
FETs	I_{dss}	225	mA/mm
	G_m	165	mS/mm
	V_{bd}	-22	V
	V_p	-1.85	V
MIM capacitors	density	300	pF/mm ²
Capacitors over vias		yes	
TaN resistors	sheet resistance	50	Ω/sq
GaAs resistors	sheet resistance	110	Ω/sq
Vias		yes	
Substrate	thickness	100	μm

FET Models Available (Noise)		
Gate Pitch (μm)	Gate Fingers	FET Sizes (μm)
25 40	12	1200
26 26	4	300
38 38	10	600

0.5- μ m HFET 2MI
DC Characteristics



0.5- μ m HFET 2MI
Maximum Available Gain/Stable Gain (MAG/MSG)
10 x 60 μ m FET @ 8 Volts, 75 mA/mm

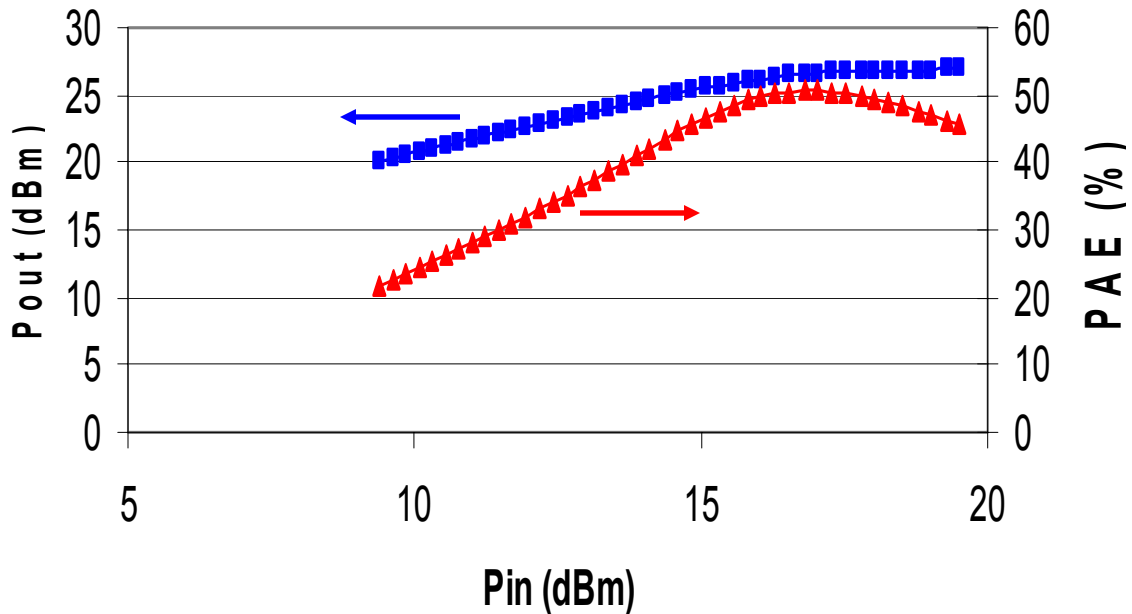


Application Examples

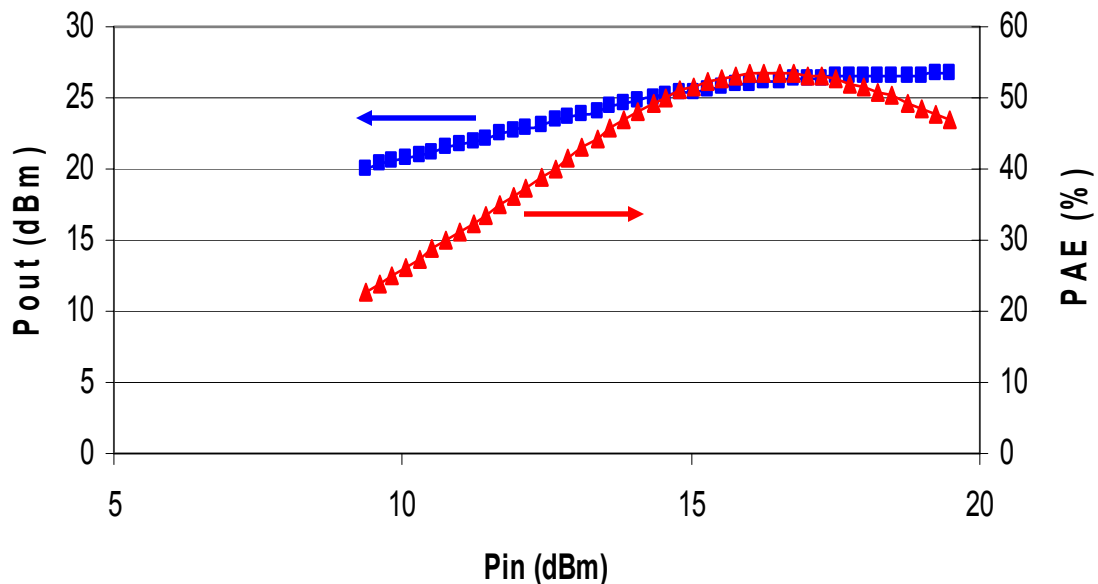
Ultra-Linear Power Amplifier TGA2801D-SG:

This amplifier provides a flat gain along with ultra-low distortion. It also provides a high output power with a low DC power consumption. This amplifier is ideally suited for use in CATV distribution systems or other applications requiring high output powers and extremely low distortion.

0.5- μ m HFET 2MI
Power Tuned Load
600 μ m FET @ 8 Volts, 45 mA, 10 GHz



0.5- μ m HFET 2MI
Efficiency Tuned Load
600 μ m FET @ 8 Volts, 45 mA, 10 GHz



Prototyping and Development

- Prototype Wafer Option (PWO)
 - Customer-specific masks
 - Customer schedule
 - 2 wafers delivered
 - Backside vias included
 - PCM (process control monitor) qualified wafers

Design Tools

- Device libraries of circuit elements:
 - FETs
 - Thin-film and implanted resistors
 - Capacitors
 - Inductors
- Agilent ADS design kit
- MASC Library
- AWR Microwave Office library

Training

- GaAs design classes:
 - Half-day introduction upon request
 - 3 day technical training upon request at the TriQuint Texas facility

Process Status

- 0.5- μ m Heterostructure FET (HFET) is fully released and qualified
- Contact TriQuint or visit <http://www.triquint.com/company/quality/> for more information on quality and reliability.

Applications Services

- Tiling of GDSII stream files including PCM (process control monitor)
- Design rule checking
- Layout versus schematic checking
- Engineering:
 - On-wafer DC test
 - On-wafer RF test
 - Thermal analysis
 - Yield enhancement
- Part qualification
- Failure analysis

Manufacturing Services

- Mask making
- Wafer thinning
- Wafer dicing
- Substrate vias
- DC die-sort testing
- RF on-wafer testing
- Final visual testing