Filtronic

FPD750

Datasheet v3.0

0.5W POWER PHEMT

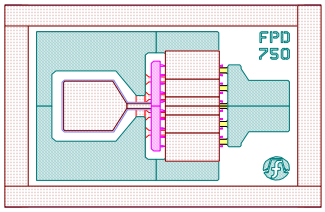
FEATURES:

- 27.5 dBm Linear Output Power at 12 GHz
- 11.5 dB Power Gain at 12 GHz
- 14.5 dB Max Stable Gain at 12 GHz
- 38 dBm Output IP3
- 50% Power-Added Efficiency

GENERAL DESCRIPTION:

The FPD750 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 μm by 750 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750 also features Si_3N_4 passivation and is available in the low cost plastic SOT89 SOT343 and DFN packages.

LAYOUT:



TYPICAL APPLICATIONS:

- Narrowband and broadband high-performance amplifiers
- SATCOM uplink transmitters
- PCS/Cellular low-voltage high-efficiency output amplifiers
- Medium-haul digital radio transmitters

ELECTRICAL SPECIFICATIONS[1]:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 8 V; IDS = 50% IDSS	26.5	27.5		dBm
Maximum Stable Gain (S21/S12)	MSG	VDS = 8 V; IDS = 50% IDSS	13.5	14.5		dB
Power Gain at P1dB	G1dB	VDS = 8 V; IDS = 50% IDSS	10.5	11.5		dB
Power-Added Efficiency	PAE	VDS = 8 V; IDS = 50% IDSS; POUT = P1dB		45		%
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 8V; IDS = 50% IDSS Matched for optimal power; Tuned for best IP3		38 40		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	185	230	280	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		370		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		200		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		10		μA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 0.75 mA		1.0		V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 0.75 mA	12.0	14.0		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 0.75 mA	14.5	16.0		V
Thermal Resistivity (see Notes)	θ_{JC}	VDS > 6V		65		°C/W

Note: [1]$T_{Ambient}$ = 22°C; RF specifications measured at *f* = 12 GHz using CW signal

Specifications subject to change without notice
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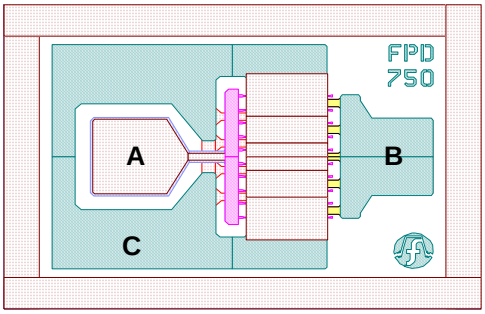
ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < -0.5V [6]	10V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDss
Gate Current	IG	Forward or reverse current	7.5mA
RF Input Power	PIN	Under any acceptable bias state	22dBm
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-65°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	2.3W
Simultaneous Combination of Limits [4]		2 or more Max. Limits	80%

Notes:
[1] $T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2] Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
[3] Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 2.3 - (0.015W/°C) x T_{HS}
where T_{HS}= heatsink or ambient temperature above 22°C
Example: For a 85°C carrier temperature: P_{TOT} = 2.3 - (0.015 x (85 – 22)) = 1.4W
[4] Users should avoid exceeding 80% of 2 or more Limits simultaneously
[5] Thermal Resitivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
[6] Operating at absolute maximum VD continuously is not recommended. If operation at 10V is considered then IDS must be reduced in order to keep the part within it's thermal power dissipation limits. Therefore VGS is restricted to < -0.5V.

PAD LAYOUT:



PAD	DESCRIPTION	PIN COORDINATES (µm)
A	Gate Pad	130, 170
B	Drain Pad	380, 170
C	Source Pad	

Note: Co-ordinates are referenced from the bottom left hand corner of the die to the centre of bond pad opening

DIE SIZE (µm)	DIE THICKNESS (µm)	MIN. BOND PAD OPENING (µm x µm)
470 x 340	75	70 x 80

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PREFERRED ASSEMBLY INSTRUCTIONS:

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

PART NUMBER	DESCRIPTION
FPD750	Die

HANDLING PRECAUTIONS:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

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