

32-Mbit (2M x 16) Static RAM

Features

- Very high speed: 70 ns
- Wide voltage range: 1.7V – 2.2V
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
 - Typical active current: 12 mA at f = f_{MAX}
- Ultra low standby power
- Easy memory expansion with \overline{CE}_1 , CE₂, and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in 48-ball VFBGA package

Functional Description

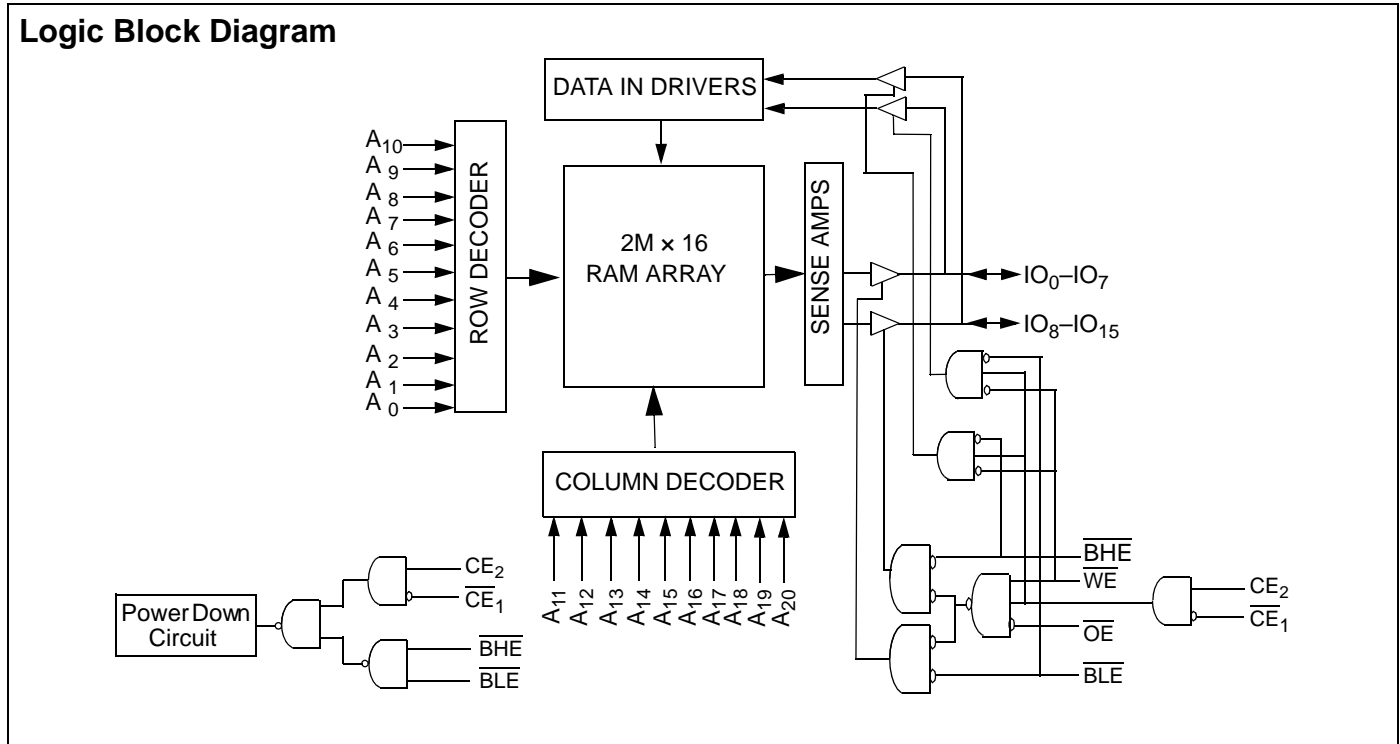
The CY62177DV20 is a high performance CMOS static RAM organized as 2M words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption

by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE₂ LOW or both BHE and BLE are HIGH). The input and output pins (IO₀ through IO₁₅) are placed in a high impedance state when: the device is deselected (\overline{CE}_1 HIGH or CE₂ LOW); outputs are disabled (\overline{OE} HIGH); both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH); when a write operation is in progress (\overline{CE}_1 LOW, CE₂ HIGH and WE LOW).

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE₂ HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO₀ through IO₇) is written into the location specified on the address pins (A₀ through A₂₀). If Byte High Enable (BHE) is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₂₀).

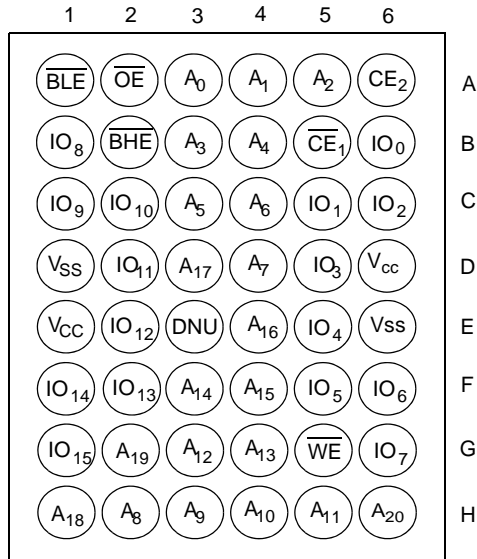
To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE₂ HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on IO₀ to IO₇. If Byte High Enable (BHE) is LOW, then data from memory appears on IO₈ to IO₁₅. See the Truth Table on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.



Pin Configuration

Figure 1. 48-Ball VFBGA (8 x 9.5 x 1.2 mm) Top View ^[1]



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1 MHz		f = f _{max}			
Min	Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max		
CY62177DV20LL	1.7	1.8	2.2	70	2	4	12	25	5	50

Notes

1. DNU pins must be connected to V_{SS} or left open.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to + 150°C
 Ambient Temperature with
 Power Applied -55°C to + 125°C
 Supply Voltage to Ground
 Potential -0.2V to $V_{CC(max)}$ + 0.2V
 DC Voltage Applied to Outputs
 in High Z State^[3, 4] -0.2V to $V_{CC(max)}$ + 0.2V

DC Input Voltage^[3, 4] -0.2V to $V_{CC(max)}$ + 0.2V
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage >2001V
 (MIL-STD-883, Method 3015)
 Latch up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[5]
CY62177DV20LL	Industrial	-40°C to +85°C	1.7V to 2.2V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	70 ns			Unit
			Min	Typ ^[2]	Max	
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA	1.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA			0.2	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 1.7V$ to $2.2V$	1.4		$V_{CC} + 0.2V$	V
V_{IL}	Input LOW Voltage	$V_{CC} = 1.7V$ to $2.2V$	-0.2		0.4	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$		12	25	mA
		$f = 1$ MHz	$V_{CC} = V_{CC(max)}$ $I_{OUT} = 0$ mA CMOS levels	2	4	
I_{SB1}	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ $f = f_{max}$ (Address and Data Only), $f = 0$ (\overline{OE} , \overline{WE} , \overline{BHE} and \overline{BLE}), $V_{CC} = V_{CC(max)}$		5	100	μA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = V_{CC(max)}$		5	50	μA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	12	pF
C_{OUT}	Output Capacitance		12	pF

Notes

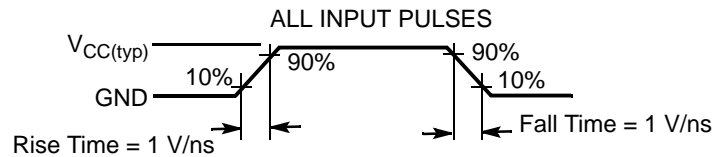
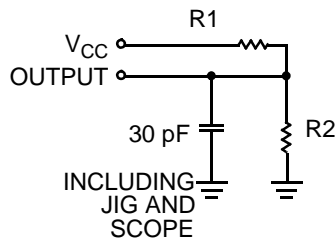
- $V_{IL(min)} = -2.0V$ for pulse durations less than 20 ns.
- $V_{IH(max)} = V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full Device AC operation is based on a 100 μs ramp time from 0 to $V_{CC(min)}$ and 100 μs wait time after V_{CC} stabilization.

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		16	°C/W

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



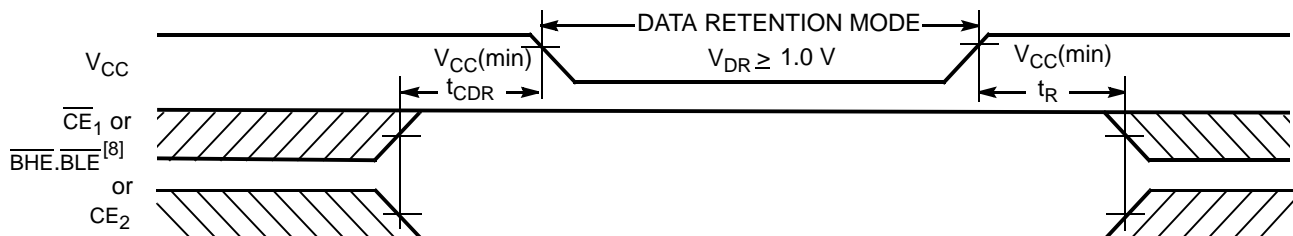
Parameters	1.8V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[2]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V, CE_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	μA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\min) > 100 \mu s$ or stable at $V_{CC}(\min) > 100 \mu s$.
- $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

 Over the Operating Range ^[9]

Parameter	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE}_1 LOW and CE ₂ HIGH to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low-Z ^[10]	5		ns
t _{HZOE}	\overline{OE} HIGH to High-Z ^[10, 11]		25	ns
t _{LZCE}	\overline{CE}_1 LOW and CE ₂ HIGH to Low-Z ^[10]	10		ns
t _{HZCE}	\overline{CE}_1 HIGH and CE ₂ LOW to High-Z ^[10, 11]		25	ns
t _{PU}	\overline{CE}_1 LOW and CE ₂ HIGH to Power Up	0		ns
t _{PD}	\overline{CE}_1 HIGH and CE ₂ LOW to Power Down		70	ns
t _{DBE}	$\overline{BLE/BHE}$ LOW to Data Valid		70	ns
t _{LZBE}	$\overline{BLE/BHE}$ LOW to Low-Z ^[10]	5		ns
t _{HZBE}	$\overline{BLE/BHE}$ HIGH to High-Z ^[10, 11]		25	ns
Write Cycle^[12]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE}_1 LOW and CE ₂ HIGH to Write End	60		ns
t _{AW}	Address Setup to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Setup to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	45		ns
t _{BW}	$\overline{BLE/BHE}$ LOW to Write End	60		ns
t _{SD}	Data Setup to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[10, 11]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[10]	10		ns

Notes

9. Test conditions are based on signal transition time of 2 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL} .
10. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
12. The internal memory write time is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 2 shows address transition controlled read cycle waveforms.^[13, 14]

Figure 2. Read Cycle No. 1

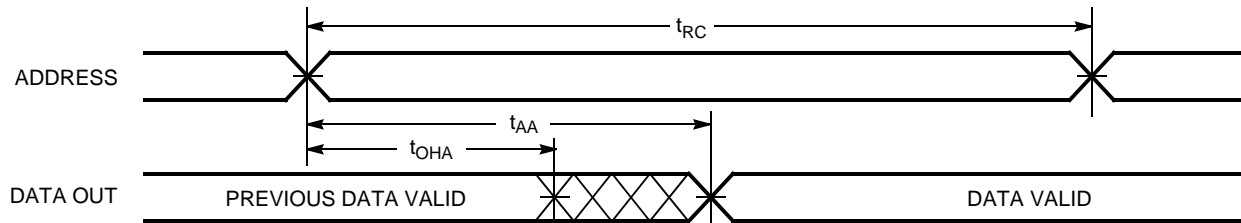
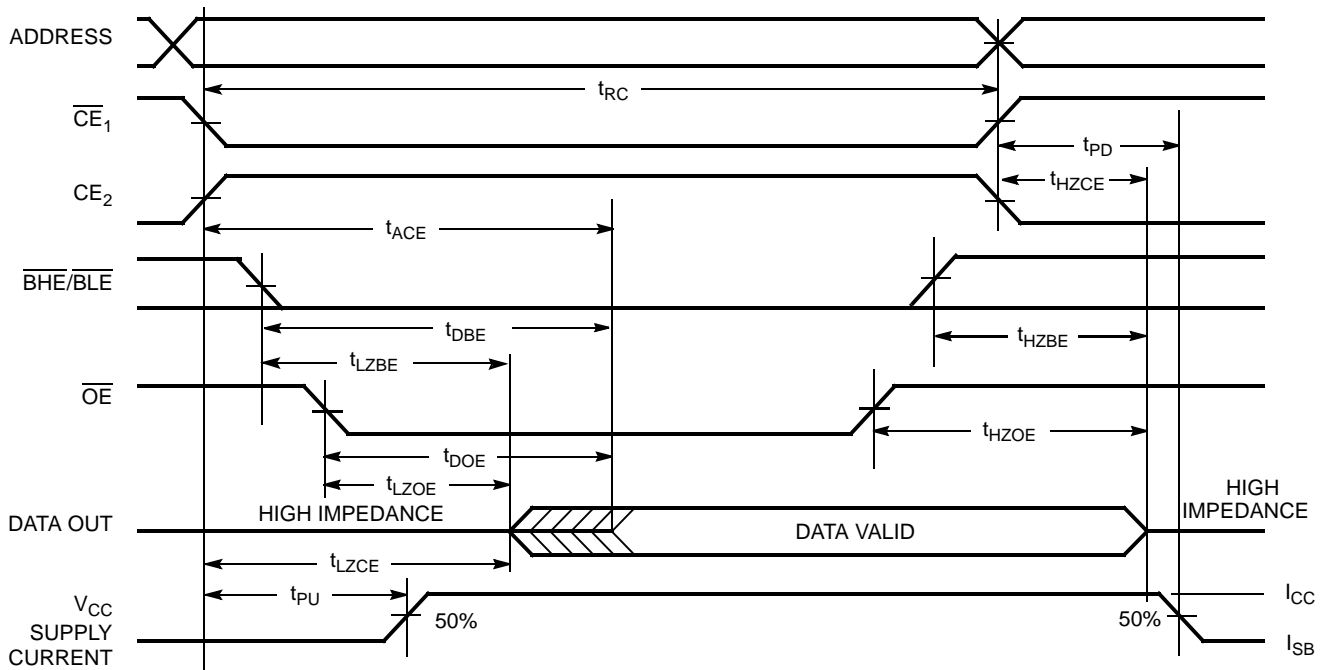


Figure 3 shows \overline{OE} controlled read cycle waveforms.^[14, 15]

Figure 3. Read Cycle No. 2



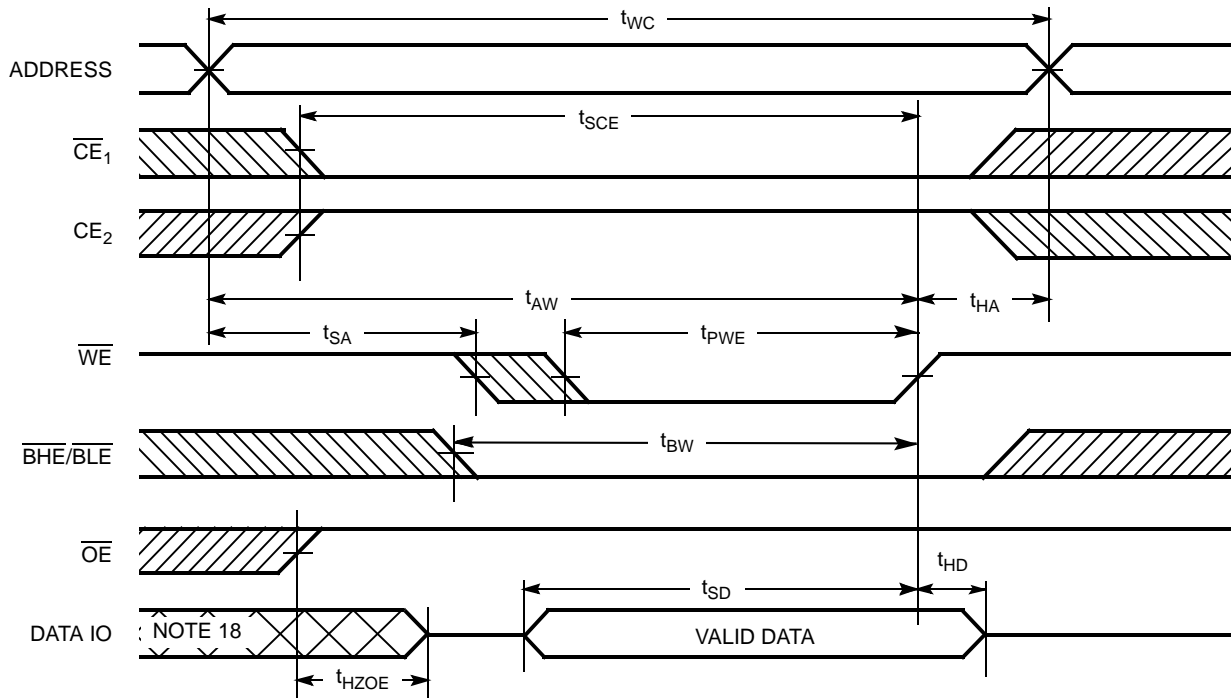
Notes

13. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$.
14. \overline{WE} is HIGH for read cycle.
15. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 4 shows \overline{WE} controlled write cycle waveforms.^[12, 16, 17]

Figure 4. Write Cycle No. 1



Notes

- 16. Data IO is high impedance if $\overline{OE} = V_{IH}$.
- 17. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 18. During this period the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 5 shows \overline{CE}_1 or CE_2 controlled write cycle waveforms.^[12, 16, 17]

Figure 5. Write Cycle No. 2

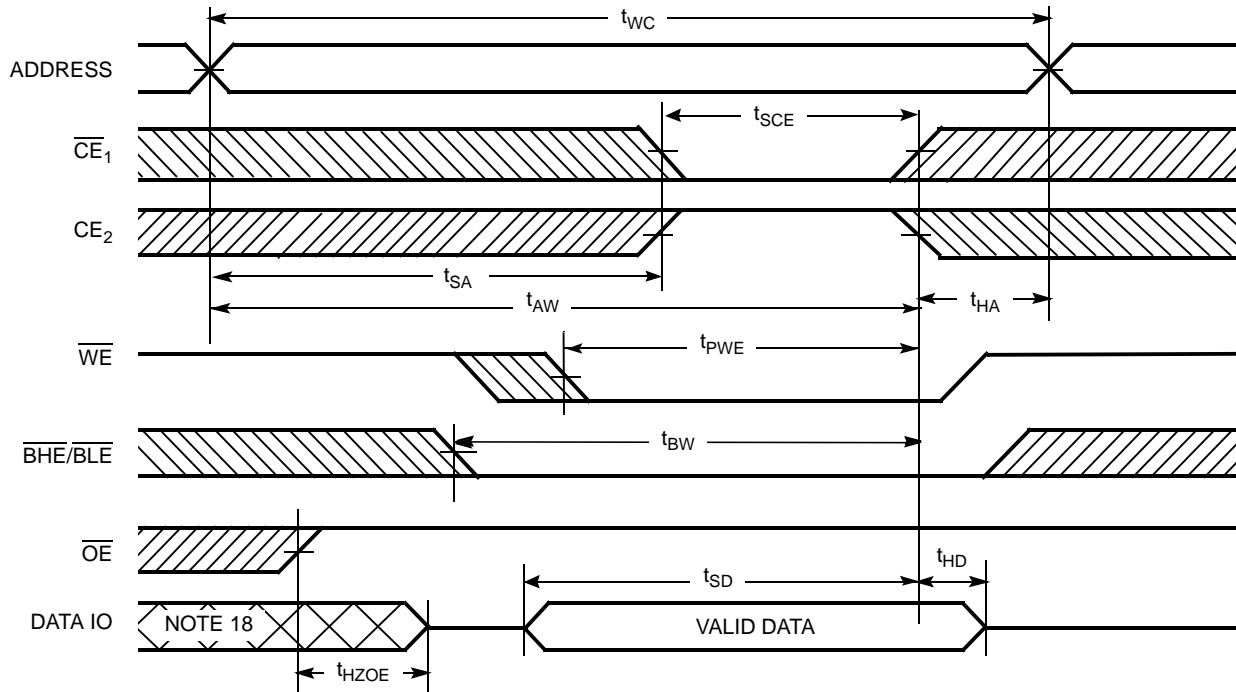
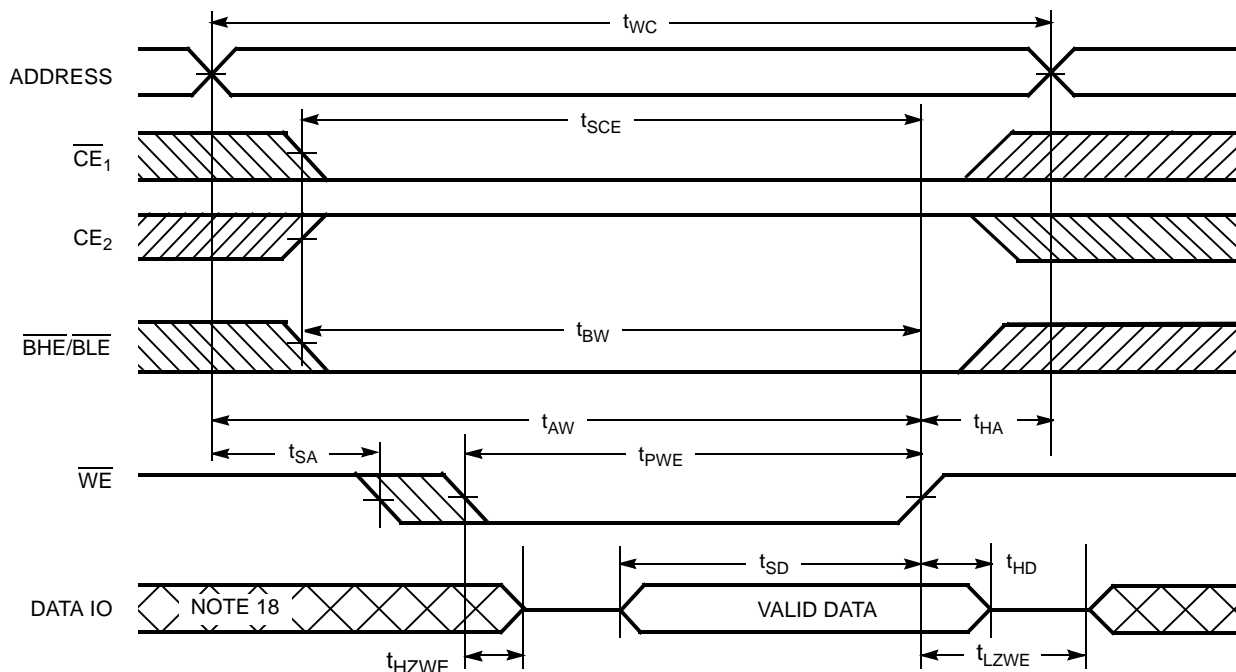


Figure 6 shows \overline{WE} controlled, \overline{OE} LOW write cycle waveforms.^[17]

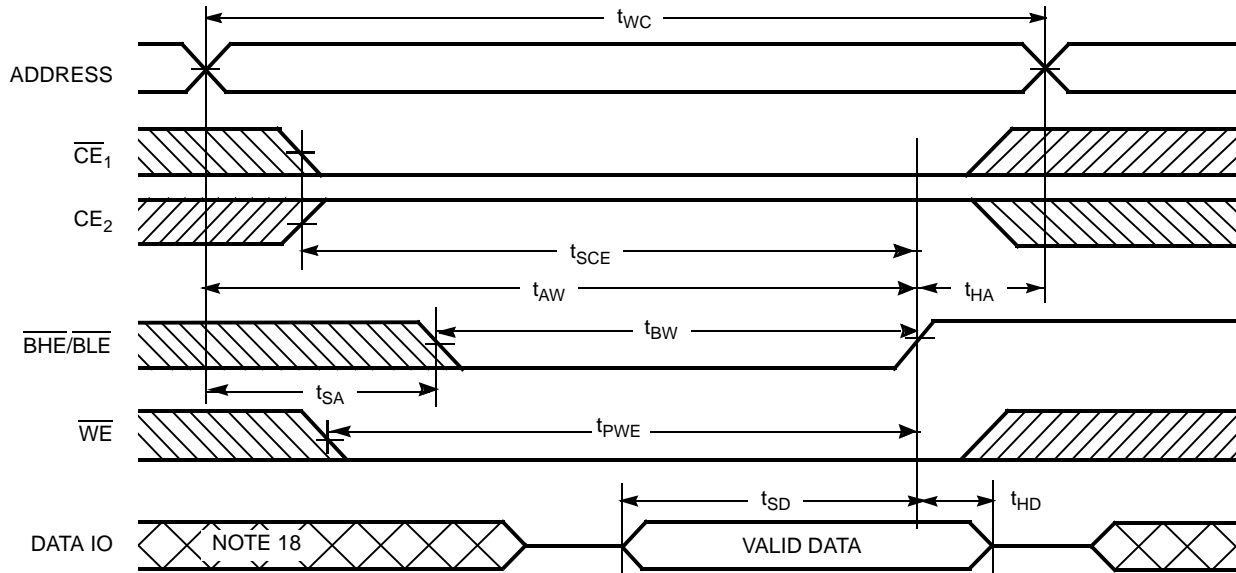
Figure 6. Write Cycle No. 3



Switching Waveforms (continued)

Figure 7 shows $\overline{\text{BHE}}/\overline{\text{BLE}}$ controlled, $\overline{\text{OE}}$ LOW write cycle waveforms.^[17]

Figure 7. Write Cycle No. 4



Truth Table

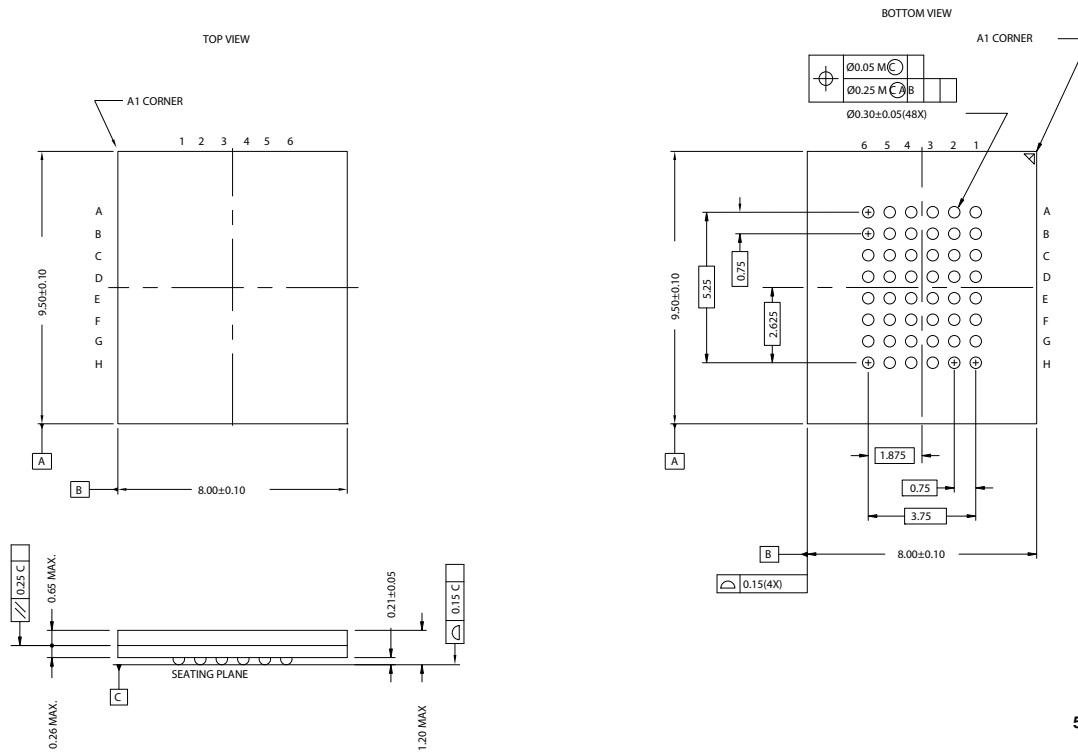
$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect / Power Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect / Power Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect / Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out ($\text{IO}_0\text{--}\text{IO}_{15}$)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out ($\text{IO}_0\text{--}\text{IO}_7$); High Z ($\text{IO}_8\text{--}\text{IO}_{15}$)	Read	Active (I_{CC})
L	H	H	L	L	H	High Z ($\text{IO}_0\text{--}\text{IO}_7$); Data Out ($\text{IO}_8\text{--}\text{IO}_{15}$)	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In ($\text{IO}_0\text{--}\text{IO}_{15}$)	Write	Active (I_{CC})
L	H	L	X	H	L	Data In ($\text{IO}_0\text{--}\text{IO}_7$); High Z ($\text{IO}_8\text{--}\text{IO}_{15}$)	Write	Active (I_{CC})
L	H	L	X	L	H	High Z ($\text{IO}_0\text{--}\text{IO}_7$); Data In ($\text{IO}_8\text{--}\text{IO}_{15}$)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62177DV20LL-70BAI	51-85191	48-ball VFBGA (8.0 x 9.5 x 1.2 mm)	Industrial

Package Diagram

Figure 8. 48-Ball VFBGA (8.0 x 9.5 x 1.2 mm)



51-85191-**

Document History Page

Document Title: CY62177DV20 MoBL2™ 32-Mbit (2M x 16) Static RAM				
Document Number: 001-44018				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	1910928	See ECN	VKN/AESA	New Data Sheet

© Cypress Semiconductor Corporation, 2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.