CY2303

Phase-Aligned Clock Multiplier

Features

- **3-multiplier configuration (1x, 2x, 4x Ref)**
- **10 MHz to 166.67 MHz operating range (reference input from 10 MHz to 41.67 MHz)**
- **Phase Alignment**
- **80 ps typical period jitter**
- **Output enable pin**
- **3.3V operation**
- **5V Tolerant input**
- **8-pin 150-mil SOIC package**
- **Commercial and Industrial Temperature available**

Functional Description

The CY2303 is a 3 output 3.3V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows user to obtain 1x, 2x, and 4x Ref output frequencies on respective output pins.

The CY2303 has an on-chip PLL, which locks to an input clock presented on the REFIN pin. The PLL feedback is internally connected to the REF output. The input-to-output skew is guaranteed to be less than ±200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

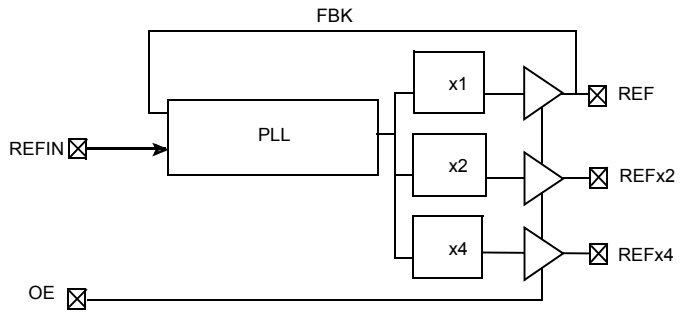
Multiple CY2303 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2303 is available in commercial and industrial temperature ranges.

Selector Guide

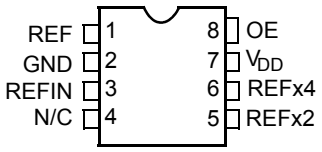
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2303SC, CY2303SXC	3	10 MHz–41.67 MHz	10 MHz–166.67 MHz	Commercial Temperature
CY2303SI, CY2303SXI	3	10 MHz–41.67 MHz	10 MHz–166.67 MHz	Industrial Temperature

Block Diagram



Pin Configuration

8-pin SOIC
Top View



Pin Description

Pin	Signal[1]	Description
1	REF	REF output (1x Reference input)
2	GND	Ground
3	REFIN	Input reference frequency, 5V tolerant input
4	N/C	No Connect
5	REFx2	2x Reference input
6	REFx4	4x Reference input
7	VDD	3.3V Supply
8	OE	Output Enable (weak pull-up)

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except Ref).....–0.5V to V_{DD} + 0.5V

DC Input Voltage REFIN .....–0.5 to 7V

Storage Temperature ..... –65°C to +150°C

Junction Temperature..... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .....>2000V

Operating Conditions for CY2303SC Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, Fout < 133.33 MHz	–	18	pF
	Load Capacitance, 133.33 MHz < Fout < 166.67 MHz	–	12	pF
C_{IN}	Input Capacitance	–	7	pF
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2303SC Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		–	0.8	V
V_{IH}	Input HIGH Voltage		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	100	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	50	μA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply Current	Unloaded outputs, REFIN = 41.67 MHz	–	45	mA
		Unloaded outputs, REFIN = 25 MHz	–	32	mA
		Unloaded outputs, REFIN = 10 MHz	–	18	mA

Notes:
1. Weak pull-down on all outputs.
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.

Switching Characteristics for CY2303SC Commercial Temperature Devices

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency	18-pF load	10	–	133.33	MHz
		12-pF load	–	–	166.67	MHz
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise Time[3]	Measured between 0.8V and 2.0V	–	–	1.20	ns
t_4	Fall Time[3]	Measured between 0.8V and 2.0V	–	–	1.20	ns
t_5	Output to Output Skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$	–	–	200	ps
t_6	Delay, REFIN Rising Edge to REF Rising Edge[3]	Measured at $V_{DD}/2$ from REFIN to any output	–	–	±200	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$ on the REF pin of the device (pin 1)	–	–	400	ps
t_J	Period Jitter[3]	Measured at Fout < 133.33 MHz, loaded outputs, 18-pF load	–	80	±175	ps
t_{LOCK}	PLL Lock Time[3]	Stable power supply, valid clocks presented on REFIN	–	–	1.0	ms

Operating Conditions for CY2303SI Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, Fout <133.33 MHz	–	15	pF
	Load Capacitance, 133.33 MHz < Fout < 166.67 MHz,	–	10	pF
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2303SI Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		–	0.8	V
V_{IH}	Input HIGH Voltage		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	100	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	–	50	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply Current	Unloaded outputs, REFIN = 41.67 MHz	–	48	mA
		Unloaded outputs, REFIN = 25 MHz	–	35	mA
		Unloaded outputs, REFIN = 10 MHz	–	20	mA

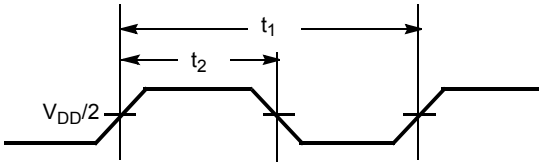
Note:
3. All parameters are specified with loaded outputs.

Switching Characteristics for CY2303SI Industrial Temperature Devices

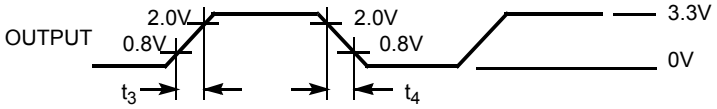
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency	15-pF load	10	–	133.33	MHz
		10-pF load	–	–	166.67	MHz
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise Time[3]	Measured between 0.8V and 2.0V	–	–	1.20	ns
t_4	Fall Time[3]	Measured between 0.8V and 2.0V	–	–	1.20	ns
t_5	Output to Output Skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$	–	–	200	ps
t_6	Delay, REFIN Rising Edge to REF Rising Edge[3]	Measured at $V_{DD}/2$ from REFIN to any output	–	–	±200	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$ on the REF pin of the device (pin 1)	–	–	400	ps
t_J	Period Jitter[3]	Measured at Fout < 133.33 MHz, loaded outputs, 15-pF load	–	80	±175	ps
t_{LOCK}	PLL Lock Time[3]	Stable power supply, valid clocks presented on REFIN	–	–	1.0	ms

Switching Waveforms

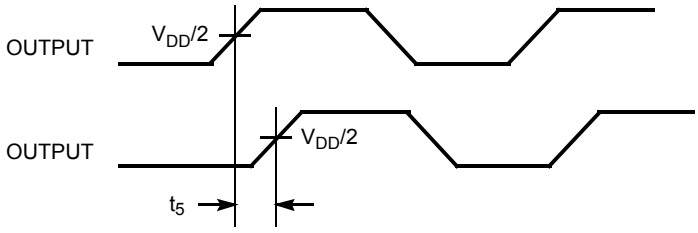
Duty Cycle Timing



All Outputs Rise/Fall Time

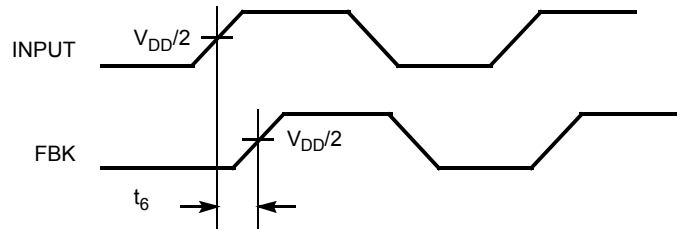


Output-Output Skew

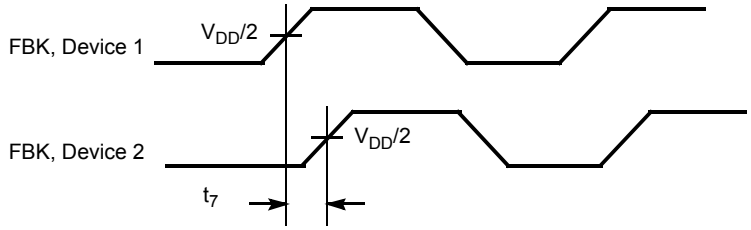


Switching Waveforms (continued)

Input-Output Propagation Delay

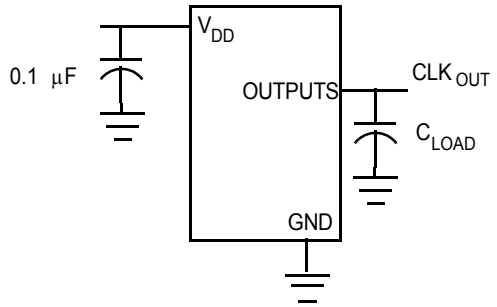


Device-Device Skew



Test Circuits

Test Circuit # 1

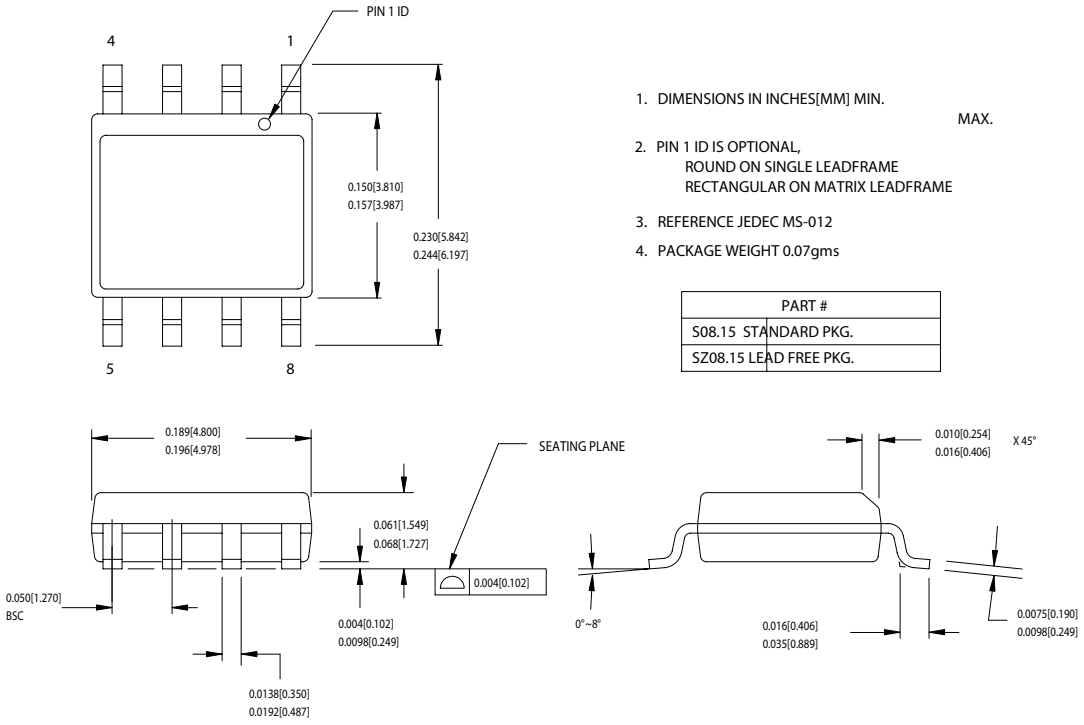


Ordering Information

Ordering Code	Package Type	Operating Range
CY2303SC	8-Pin 150-mil SOIC	Commercial
CY2303SCT	8-Pin 150-mil SOIC - Tape and Reel	Commercial
CY2303SI	8-Pin 150-mil SOIC	Industrial
CY2303SIT	8-Pin 150-mil SOIC - Tape and Reel	Industrial
Lead-free		
CY2303SXC	8-Pin 150-mil SOIC	Commercial
CY2303SXCT	8-Pin 150-mil SOIC - Tape and Reel	Commercial
CY2303SXI	8-Pin 150-mil SOIC	Industrial
CY2303SXIT	8-Pin 150-mil SOIC - Tape and Reel	Industrial

Package Diagram

8-lead (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

51-85066-*C

Document Title: CY2303 Phase-Aligned Clock Multiplier Document Number: 38-07249				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110514	01/07/02	SZV	Change from Spec number: 38-01036 to 38-07249
*A	121852	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	390413	See ECN	RGL	Added Lead-free devices Added typical values for jitter