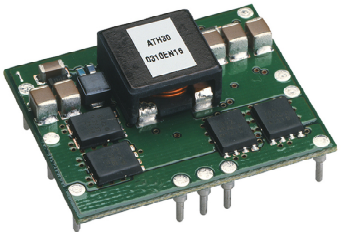
ATH26K12 Series - 12-V Input

26-A, 12-V Input Non-Isolated Wide-Output Adjust Power Module

POLA Point-of-Load Alliance

REVISION 00 (30APR2004)



NOMINAL SIZE = **1.37 in x 1.12 in (34,8 mm x 28,5 mm)**

Features

- Up to 26 A Output Current
- 12-V Input Voltage
- Wide-Output Voltage Adjust (1.2 V to 5.5 V)
- Efficiencies up to 94 %
- 235 W/in³ Power Density
- On/Off Inhibit
- Output Voltage Sense
- Pre-Bias Startup
- Margin Up/Down Controls
- Dual-Phase Topology
- Auto-Track™ Sequencing
- Under-Voltage Lockout
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Over-Temperature Protection
- Operating Temp: –40 to +85 °C
- Safety Agency Approvals: UL 1950, CSA 22.2 950, EN60950 VDE (Pending)
- Point-of-Load Alliance (POLA) Compatible

Description

The ATH26K12 is a series of high-current non-isolated power module. This product is characterized by high efficiencies, and up to 26 A of output current, while occupying a mere 1.64 in² of PCB area. In terms of cost, size, and performance, the series provides OEM's with a flexible module that meets the requirements of the most complex and demanding mixed-signal applications. These include the most densly populated, multi-processor systems that incorporate high-speed DSP's, microprocessors, and ASICs.

The series uses double-sided surface mount construction and provides high-performance step-down power conversion from a 12-V input bus voltage. The output voltage of the ATH26K12 can be set to any value over the range, 1.2 V to 5.5 V, using a single resistor.

This series includes Auto-Track™. Auto-Track simplifies power-up and power-down supply voltage sequencing in a system by enabling modules to track each other, or any other external voltage.

Each model also includes an on/off inhibit, output voltage adjust (trim), and margin up/down controls. An output voltage sense ensures tight load regulation, and an output over-current and thermal shutdown feature provide for protection against external load faults.

Package options inlude both through-hole and surface mount connfigurations.

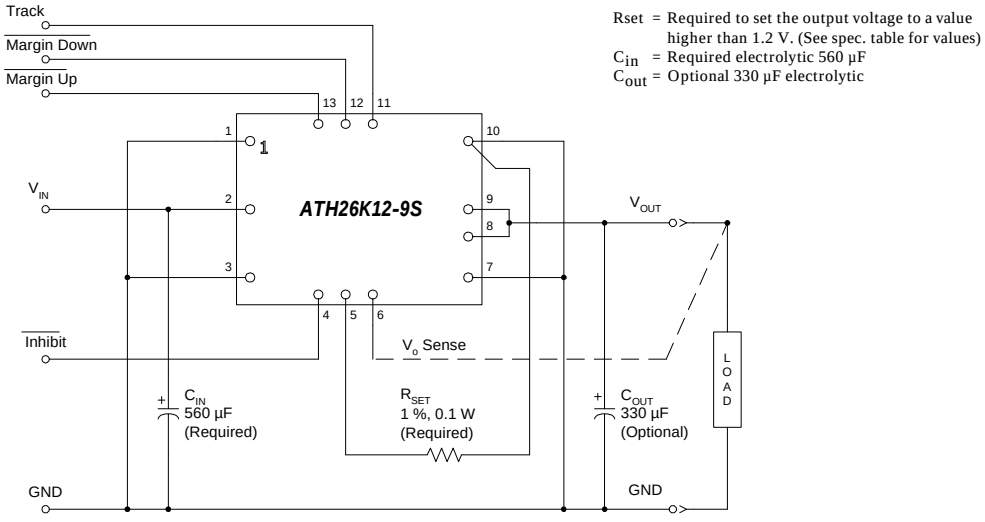
Pin Configuration

Pin	Function
1	GND
2	V_{in}
3	GND
4	Inhibit *
5	V_o Adjust
6	V_o Sense
7	GND
8	V_{out}
9	V_{out}
10	GND
11	Track
12	Margin Down *
13	Margin Up *

* *Denotes negative logic:*
Open = Normal operation
Ground = Function active

Auto-Track™ Sequencing

Standard Application



Rset = Required to set the output voltage to a value higher than 1.2 V. (See spec. table for values)
C_{in} = Required electrolytic 560 µF
C_{out} = Optional 330 µF electrolytic

Ordering Information

Input Voltage	Output Voltage	Output Current	Model Number
10.8V to 13.2V	1.2V[1] to 5.5V	26A	ATH26K12-9(S)(J)

Options:

"-J" - Through-hole Termination, Tray Packaging
"-SJ" - SMT Termination, Tray Packaging

Notes:
[1]Preset output voltage is 1.2V; externally adjustable to 5.5V through the Vo,Adjust pin

Pin Descriptions

Vin: The positive input voltage power node to the module, which is referenced to common *GND*.

Vout: The regulated positive power output with respect to the *GND* node.

GND: This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's *output and turns off the output voltage*. *When the Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

Vo Adjust: A 0.1 W, 1 % tolerance (or better) resistor must be connected directly between this pin and the output ground (pin 10) to set the output voltage to the desired value. The set point range for the output voltage is from 1.2 V to 5.5 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output will default to its lowest output voltage value. For further information on output voltage adjustment consult the related application note.

$$R_{set} = 10\ k\Omega \cdot \frac{0.8\ V}{V_{out} - 1.2\ V} - 1.82\ k\Omega$$

The specification table gives the preferred resistor values for a number of standard output voltages.

Vo Sense: The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vo Sense* should be connected to *Vout*. It can also be left disconnected.

Track: This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused this input should *be connected to* V_{in}. *Note: Due to the under-voltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, consult the related application note.*

Margin Down: When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accomodated with a series resistor. For further information, consult the related application note.

Margin Up: When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, consult the related application note.

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Signal Input Voltages		Track control (pin 11) Inhibit control (pin 4)	–0.3 –0.3	— —	V_{in} + 0.3 5	V
Operating Temperature Range	T_a	Over V_{in} Range	–40	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			235 (i)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	15	—	G's
Weight	—		—	10	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.*

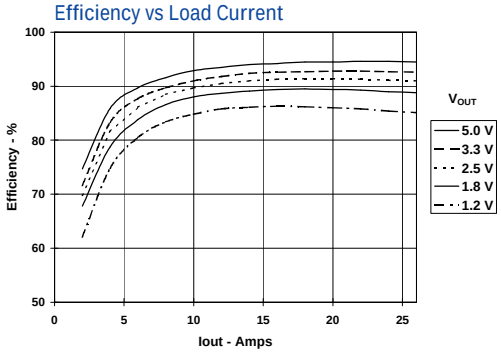
Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =12 V, V_{out} =3.3 V, C_{in} =560 µF, C_{out} =0 µF, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	ATH26K12 Min	ATH26K12 Typ	ATH26K12 Max	Units
Output Current	I_o	60 °C, 200 LFM airflow 25 °C, natural convection	0 0	— —	26 (1) 26 (1)	A
Input Voltage Range	V_{in}	Over I_o range	10.2	—	13.8	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	% V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±5	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±5	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3 (2)	%V_o
Efficiency	η	I_o =18 A R_{SET} = 280 Ω V_o = 5.0 V R_{SET} = 2.0 kΩ V_o = 3.3 V R_{SET} = 4.32 kΩ V_o = 2.5 V R_{SET} = 11.5 kΩ V_o = 1.8 V R_{SET} = 24.3 kΩ V_o = 1.5 V R_{SET} = open cct. V_o = 1.2 V	— — — — — —	94.5 92.7 91.4 89.5 88.2 86.2	— — — — — —	%
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth All voltages	—	25	—	mVpp
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery	—	50	—	A
Transient Response	t_{tr} ΔV_{tr}	1 A/µs load step, 50 to 100 % $I_o$max, C_{out} =330 µF Recovery Time V_o over/undershoot	— —	50 150	— —	µSec mV
Margin Up Down Adjust	V_o adj	With V_o Adjust control	—	± 5	—	%
Margin Input Current (pins 12 /13)	I_{IL} margin	Pin to GND	—	– 8 (3)	—	µA
Track Input Current (pin 11)	I_{IL} track	Pin to GND	—	—	–0.13 (3)	mA
Track Slew Rate Capability	dV_{track}/dt	C_{out} ≤ C_{out}(max)	—	—	1	V/ms
Under-Voltage Lockout	UVLO	V_{in} increasing V_{in} decreasing	— 8	9.5 8.5	10 —	V
Inhibit Control (pin4) Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to GND	 2.5 –0.2	 — —	 Open (4) 0.5	V
Input Low Current	I_{IL} inhibit	Pin to GND	—	–0.5	—	mA
Input Standby Current	I_{in} inh	Inhibit (pin 4) to GND, Track (pin 11) to V_{in}	—	10	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	475	575	675	kHz
External Input Capacitance	C_{in}		560 (5)	—	—	µF
External Output Capacitance	C_{out}	Capacitance value non-ceramic ceramic	0 0	330 (6) —	7,150 (7) 300	µF
		Equiv. series resistance (non-ceramic)	4 (8)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign	3	—	—	10^6 Hrs

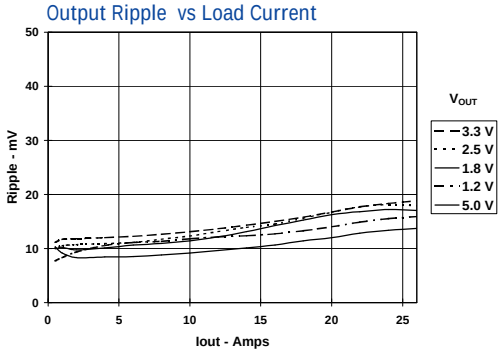
Notes: *(1) See SOA curves or consult factory for appropriate derating.*
(2) The set-point voltage rolerance is affected be the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1 % with 100 ppm/°C or better temperature stability.
(3) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(4) This control pin has an internal pull-up to 5 V nominal. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(5) A 560 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 500 mArms of ripple current.
(6) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.
(7) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.
(8) This is the typcial ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 mW as the minimum when using max-ESR values to calculate.

Characteristic Data; V_{in} =12 V *(See Note A)*

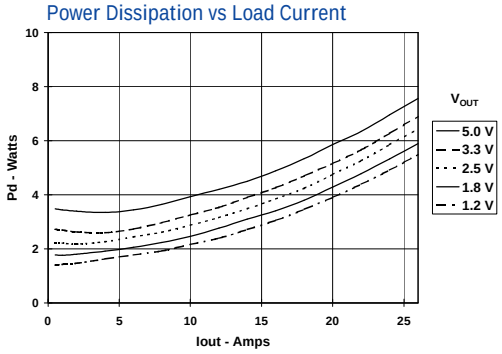
Efficiency vs Load Current



Output Ripple vs Load Current

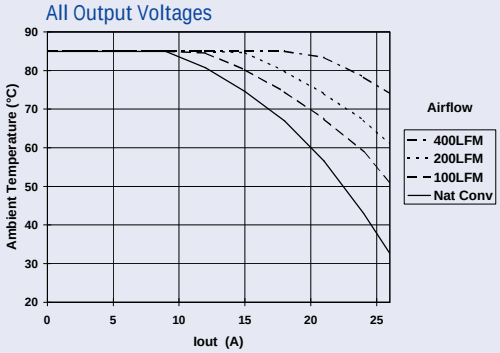


Power Dissipation vs Load Current



Safe Operating Area; V_{in} =12 V *(See Note B)*

All Output Voltages



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. ´ 4 in. double-sided PCB with 1 oz. copper.*

Capacitor Recommendations for the ATH26K12 Series of Power Modules

Input Capacitor

The recommended input capacitor(s) is determined by the 560 µF [3] minimum capacitance and 500 mArms minimum ripple current rating.

Ripple current, less than 100 mΩ equivalent series resistance (ESR), and temperature are major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (max. DC voltage + AC ripple). This is standard practice to ensure reliability. There were no tantalum capacitors, with sufficient voltage rating, found to meet this requirement. [1] When the operating temperature is below 0 °C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-tantalum types should be considered.

Adding one or two ceramic capacitors to the input will further reduce high-frequency reflected ripple current. [4]

Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from external output capacitance. The recommended output capacitance of 330 µF will allow the module to meet its transient response specification (see product data sheet). For most applications, a high quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0 °C. For operation below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 1-1.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors can only be used on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

Capacitor Table

Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Very Fast Load Transients

The transient response of the DC/DC converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any DC/DC converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, or the total amount of load capacitance is above 3,000 µF, the selection of output capacitors becomes more important. For further guidance consult the separate application note, *"Selecting Output Capacitors for PTH Products in High-Performance Applications."*

Table 1-1: Input/Output Capacitors

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85 °C (Irms)	Physical Size(mm)	Input Bus	Optional Output Bus	Vendor Part Number
Panasonic	25 V	330	0.090 Ω	>1100 mA	10×12.5	2	1	EEUFC1E331
FC (Radial)	25 V	560	0.065 Ω	1205 mA	12.5×15	1	1	EEUFC1E561S
	25 V	470	0.080 Ω	>1100 mA	10×10.2	2	1	EEVFK1E471P
FK (SMD)	35 V	680	0.060 Ω	1100 mA	12.5×13.5	1	1	EEVFK1V681Q
United Chemi-Con	16 V	330	0.018 Ω	4500 mA	10×10.5	2	≤3	16FX330M
FX, Os-con (SMD)	16 V	330	0.090 Ω	760 mA	10×12.5	2	1	LXZ25VB331M10X12LL
LXZ, Aluminum (Radial)	25 V	680	0.068 Ω	1050 mA	10×16	1	1	LXZ16VB681M10X16LL
PS, Poly-Aluminum(Radial)	16 V	330	0.014 Ω	5060 mA	10 ×12.5	2	≤3	16PS330MJ12
PXA, Poly-Aluminum (SMD)	16 V	330	0.014 Ω	5050 m A	10×12.2	2	≤3	PXA16VCMJ12
Nichicon, Aluminum	25 V	560	0.060 Ω	1060 mA	12.5×15	1	1	UPM1E561MHH6
HD (Radial)	25 V	680	0.038 Ω	1430 mA	10×16	1	1	UHD1C681MHR
PM (Radial)	35 V	560	0.048 Ω	1360 mA	16×15	1	1	UPM1V561MHH6
Panasonic, Poly-Aluminum:								
WA (SMD)	16 V	330	0.022 Ω	4100 mA	10×10.2	2	≤3	EEFWA1C331P
S/SE (SMD)	6.3 V	180	0.005 Ω	4000 mA	7.3×4.3×–4.2	N/R [1]	≤1 [2]	EEFSE0J181R **(V_o£5.1V)**
Sanyo	10 V	330	0.025 Ω	3000 mA	7.3L	N/R [1]	≤4	10TPE330M
TPE, Poscap (SMD)	16 V	270	0.018 Ω	>3500 mA	×5.7W	2 [3]	≤3	16SP270M
SP, Os-Con (Radial)	16 V	330	0.016 Ω	4700 mA	10×10.5	2	≤3	16SVP330M
SVP, Os-Con (SMD)					11×12			
AVX, Tantalum, Series III	10 V	470	0.045 Ω	>1723 mA	7.3L	N/R [1]	≤5 [2]	TPSE477M010R0045 **(V_o£5.1V)**
TPS (SMD)	10 V	330	0.045 Ω	>1723 mA	×5.7W	N/R [1]	≤5 [2]	TPSE337M010R0045 **(V_o£5.1V)**
					×4.1H			
Kemet, Poly-Tantalum								
T520 (SMD)	10 V	330	0.040 Ω	1800 mA	4.3W	N/R [1]	≤5	T520X337M010AS
T530 (SMD)	10 V	330	0.015 Ω	>3800 mA	×7.3L	N/R [1]	≤2	T530X337M010AS
	6.3 V	470	0.012 Ω	4200 mA	×4.0H	N/R [1]	≤2 [2]	T530X477M006AS **(V_o£5.1V)**
Vishay-Sprague	10 V	470	0.100 Ω	1440 mA	7.2L×6W	N/R [1]	≤5 [2]	595D477X0010R2T **(V_o£5.1V**
595D, Tantalum (SMD)					×4.1H			
94SA, Os-con (Radial)	16 V	1,000	0.015 Ω	9740 mA	16×25	1	≤2	94SA108X0016HBP
Kemet, Ceramic X5R (SMD)	16 V	10	0.002 Ω	—	1210 case	1 [4]	≤5	C1210C106M4PAC
	6.3 V	47	0.002 Ω		3225 mm	N/R [1]	≤5	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V	100	0.002 Ω	—	1210 case	N/R [1]	≤3	GRM32ER60J107M
	6.3 V	47			3225 mm	N/R [1]	≤5	GRM32ER60J476M
	16 V	22				1 [4]	≤5	GRM32ER61C226K
	16 V	10				1 [4]	≤5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V	100	0.002 Ω	—	1210 case	N/R [1]	≤3	C3225X5R0J107MT
	6.3 V	47			3225 mm	N/R [1]	≤5	C3225X5R0J476MT
	16 V	22				1 [4]	≤5	C3225X5R1C226MT
	16 V	10				1 [4]	≤5	C3225X5R1C106MT

[1] N/R –Not recommended. The voltage rating does not meet the minimum operating limits.
[2] The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V.
[3] Total capacitance of 540 µF is acceptable based on the combined ripple current rating.
[4] Small ceramic capacitors may used to complement electrolytic types at the input to further reduce high-frequency ripple current.

Adjusting the Output Voltage of the ATH26K12 Wide-Output Adjust Power Module

The V_o *Adjust* control (pin 5) sets the output voltage of the ATH26K12 product. The adjustment range is from 1.2 V to 5.5 V. To adjust the output voltage above 1.2 V a single external resistor, R_{set}, must be connected directly between the V_o *Adjust* and the *GND* pins [1]. Table 2-1 gives the preferred value for the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2-2. Figure 2-1 shows the placement of the required resistor.

$$R_{set} = 10\ k\Omega \cdot \frac{0.8\ V}{V_{out} - 1.2\ V} - 1.82\ k\Omega$$

Table 2-1; Preferred Values of R_{set} for Standard Output Voltages

V_{out} (Standard)	R_{set} (Pref'd Value)	V_{out} (Actual)
5 V	280 Ω	5.009 V
3.3 V	2 kΩ	3.294V
2.5 V	4.32 kΩ	2.503 V
2 V	8.06 kΩ	2.010V
1.8 V	11.5 kΩ	1.801 V
1.5 V	24.3 kΩ	1.506 V
1.2 V	Open	1.200 V

Figure 2-1; V_o Adjust Resistor Placement

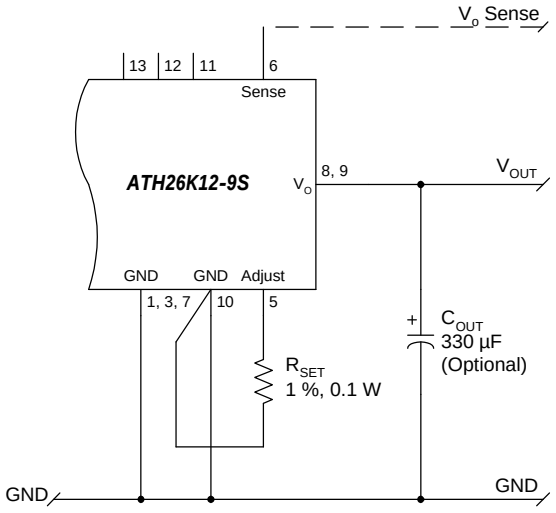


Table 2-2; Output Voltage Set-Point Resistor Values

V_a Req'd	R_{set}	V_a Req'd	R_{set}
1.200	Open	2.75	3.34 kΩ
1.225	318 kΩ	2.80	3.18 kΩ
1.250	158 kΩ	2.85	3.03 kΩ
1.275	105 kΩ	2.90	2.89 kΩ
1.300	78.2 kΩ	2.95	2.75 kΩ
1.325	62.2 kΩ	3.00	2.62 kΩ
1.350	51.5 kΩ	3.05	2.5 kΩ
1.375	43.9 kΩ	3.10	2.39 kΩ
1.400	38.2 kΩ	3.15	2.28 kΩ
1.425	33.7 kΩ	3.20	2.18 kΩ
1.450	30.2 kΩ	3.25	2.08 kΩ
1.475	27.3 kΩ	3.30	1.99 kΩ
1.50	24.8 kΩ	3.35	1.9 kΩ
1.55	21 kΩ	3.40	1.82 kΩ
1.60	18.2 kΩ	3.45	1.74 kΩ
1.65	16 kΩ	3.50	1.66 kΩ
1.70	14.2 kΩ	3.55	1.58 kΩ
1.75	12.7 kΩ	3.6	1.51 kΩ
1.80	11.5 kΩ	3.7	1.38 kΩ
1.85	10.5 kΩ	3.8	1.26 kΩ
1.90	9.61 kΩ	3.9	1.14 kΩ
1.95	8.85 kΩ	4.0	1.04 kΩ
2.00	8.18 kΩ	4.1	939 Ω
2.05	7.59 kΩ	4.2	847 Ω
2.10	7.07 kΩ	4.3	761 Ω
2.15	6.6 kΩ	4.4	680 Ω
2.20	6.18 kΩ	4.5	604 Ω
2.25	5.8 kΩ	4.6	533 Ω
2.30	5.45 kΩ	4.7	466 Ω
2.35	5.14 kΩ	4.8	402 Ω
2.40	4.85 kΩ	4.9	342 Ω
2.45	4.85 kΩ	5.0	285 Ω
2.50	4.33 kΩ	5.1	231 Ω
2.55	4.11 kΩ	5.2	180 Ω
2.60	3.89 kΩ	5.3	131 Ω
2.65	3.7 kΩ	5.4	85 Ω
2.70	3.51 kΩ	5.5	41 Ω

Notes:

1. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly from pin 5 to pin 10 using dedicated PCB traces.
2. Never connect capacitors from V_o *Adjust* to either *GND* or V_{out}. Any capacitance added to the V_o *Adjust* pin will affect the stability of the regulator.

Features of the ATH Family of Non-Isolated Wide Output Adjust Power Modules

Point-of-Load Alliance

The ATH family of non-isolated, wide-output adjust power modules are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the "Point-of-Load Alliance" (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Texas Instruments, Artesyn Technologies, and Astec Power to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the ATH06 (6 A), ATH10 (10 A), ATH12/15 (12/15 A), ATH18/22 (18/22 A), and the ATH26/30 (26/30 A).

From the basic, "Just Plug it In" functionality of the 6-A modules, to the 30-A rated feature-rich ATH30, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the available features by product and input bus voltage.

Table 3-1; Operating Features by Series and Input Bus Voltage

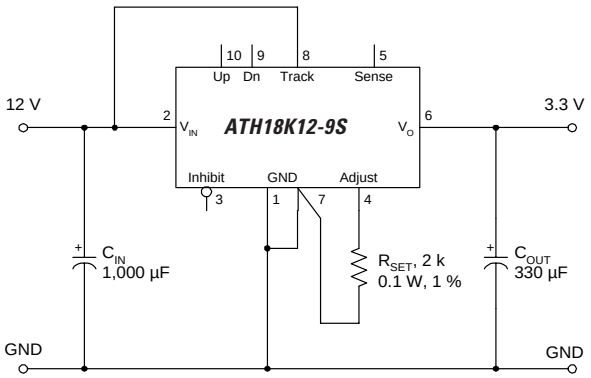
Series	Input Bus	I_{OUT}	Adjust (Trim)	On/Off Inhibit	Over-Current	Pre-Bias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
ATH06	3.3 V / 5 V	6 A	•	•	•	•	•			
	12 V	6 A	•	•	•		•			
ATH10	3.3 V / 5 V	10 A	•	•	•	•	•	•	•	
	12 V	10 A	•	•	•		•	•	•	
ATH12/15	3.3 V / 5 V	15 A	•	•	•	•	•	•	•	
	12 V	12 A	•	•	•		•	•	•	
ATH18/22	3.3 V / 5 V	22 A	•	•	•	•	•	•	•	•
	12 V	18 A	•	•	•		•	•	•	•
ATH26/30	3.3 V / 5 V	30 A	•	•	•	•	•	•	•	•
	12 V	26 A	•	•	•	•	•	•	•	•

For simple point-of-use applications, the ATH06K12 (6 A) provides operating features such as an on/off inhibit, output voltage trim, and over-current protection. The ATH10K12 (10 A), and ATH12K12 (12 A) include an output voltage sense, and margin up/down controls. Then the higher output current, ATH18K12 (18 A) and ATH26K12 (26 A) products incorporate over-temperature shutdown protection. All of the products referenced in Table 3-1 include Auto-Track™. This is a feature unique to the ATH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

Soft-Start Power Up

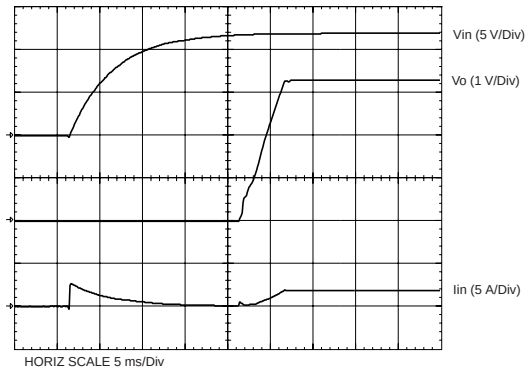
The Auto-Track™ feature allows the power-up of multiple ATH modules to be directly controlled from the *Track* pin. However in a stand-alone configuration, or when the Auto-Track™ feature is not being used, the *Track* pin should be directly connected to the input voltage, V_{in} (see Figure 3-1).

Figure 3–1



When the *Track* pin is connected to the input voltage the Auto-Track™ function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

Figure 3–2



From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 5 ms-10 ms) before allowing the output voltage to rise. The output then progressively rises to the module's set-point voltage. Figure 3-2 shows the soft-start power-up characteristic of the 18-A output product (ATH18K12), operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track™ feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 15 ms.

Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Over-Temperature Protection (OTP)

The ATH18K12 and ATH26K12 of products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

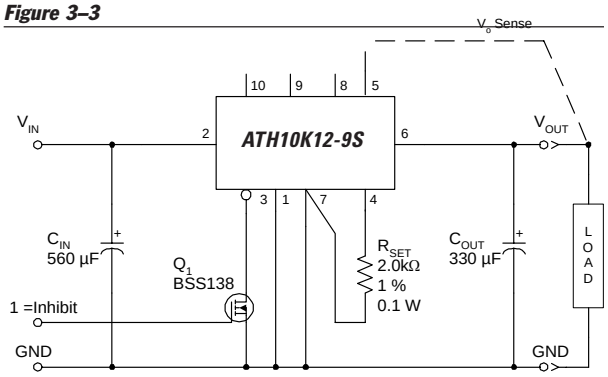
Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the ATH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to *GND*.

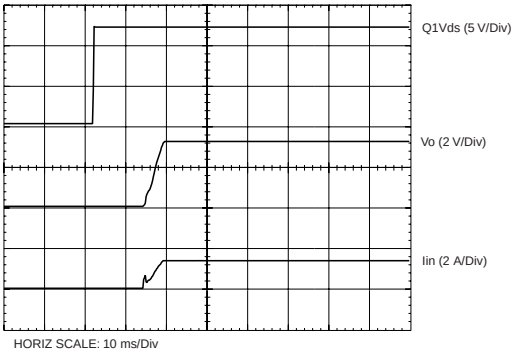
Figure 3-3 shows the typical application of the inhibit function. Note the discrete transistor (Q_1). The *Inhibit* input has its own internal pull-up to V_{in} potential (12 V). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Figure 3–3



Turning Q_1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q_1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 msec. Figure 3-4 shows the typical rise in both the output voltage and input current, following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 5-A constant current load.

Figure 3–4



Auto-Track™ Function

The Auto-Track™ function is unique to the ATH family, and is available with the all "Point-of-Load Alliance" (POLA) products. Auto-Track™ was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

How Auto-Track™ Works

Auto-Track™ works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. For convenience the Track control incorporates an internal RC charge circuit. This operates off the module's input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track™ allows for simultaneous voltage sequencing of a number of Auto-Track™ compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q_1 in Figure 3-5.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the circuit's On/Off Control turns Q_1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q_1 is on.

10 ms after a valid input voltage has been applied to the modules, Q_1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-6 shows the output voltage waveforms from the circuit of Figure 3-5 after the On/Off Control is set from a high to a low-level voltage. The waveforms, Vo_1 and Vo_2 represent the output voltages from the two power modules, U_1 (3.3 V) and U_2 (2 V) respectively. Vo_1 and Vo_2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q_1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 1 V/ms. The components R_1 and C_1 in Figure 3-5 limit the rate at which Q_1 can pull down the Track control voltage. The values of 100 k-ohm and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-7 shows the power-down waveforms. As the Track™ control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track™ control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track™ function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absloute maximum voltage that may be applied to the Track pin is the input voltage V_{in}.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore startup into an output prebias cannot be supported when a module is under Auto-Track™ control. *Note: A pre-bias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.*
6. The Auto-Track™ function can be disabled by connecting the *Track* pin to the input voltage (V_{in}). When Auto-Track™ is disabled, the output voltage will rise at a quicker and more linear rate after input power is applied.

***Auto-Track is a trademark of Texas Intruments, Inc.*

Figure 3–5; Sequenced Power Up & Power Down Using Auto-Track

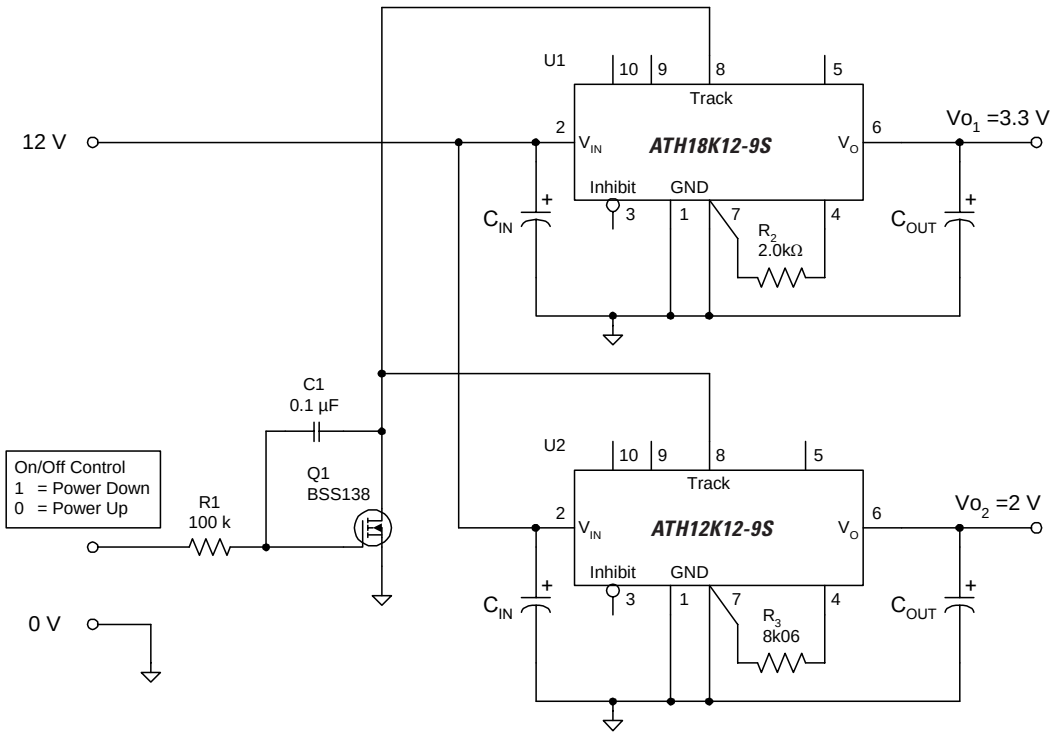


Figure 3–6; Simultaneous Power Up with Auto-Track™ Control

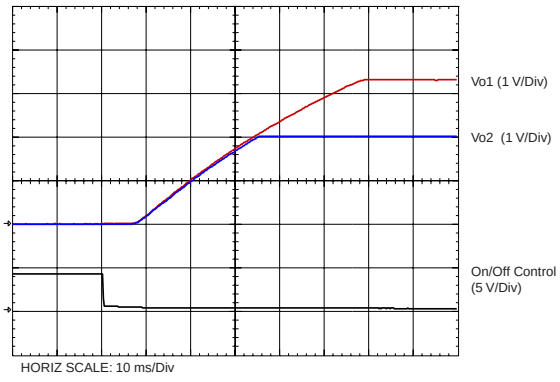
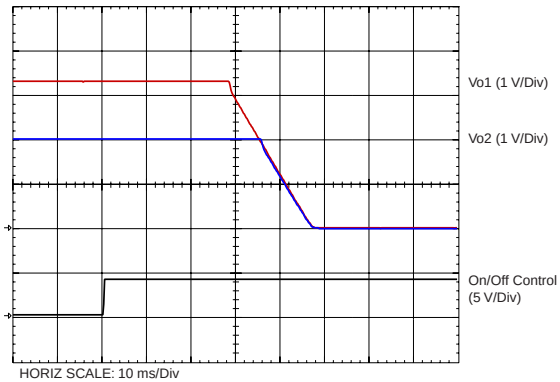


Figure 3–7; Simultaneous Power Down with Auto-Track™ Control



Margin Up/Down Controls

The ATH10K12, ATH12K12, ATH18K12, and ATH26K12 products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5 % change is applied to the adjusted output voltage, as set by the external resistor, R_{set} at the *V_o Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5 %, series resistors are required (See R_D and R_U in Figure 3-8). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formulas is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

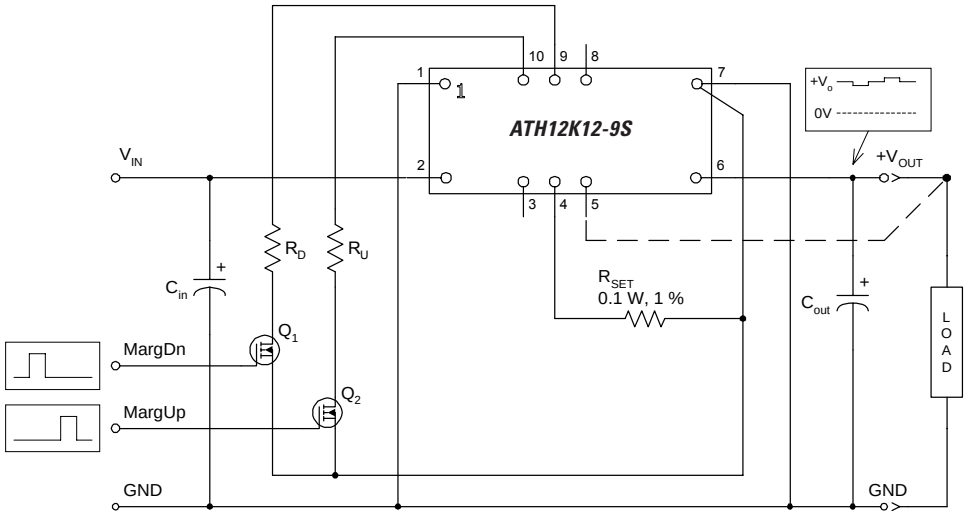
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the ATH06). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q_1 and Q_2 should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Table 3-2; Margin Up/Down Resistor Values

% Adjust	R_U / R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 3–8; Margin Up/Down Application Schematic



Pre-Bias Startup Capability

The ATH26K12 power module is capable of safely powering up while a voltage is applied to its output from an external source.

A pre-bias startup condition can occur in complex digital systems when current from another power source backfeeds through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. The prebias condition can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

Although the ATH26K12 power module incorporates synchronous rectifiers it will not sink current during startup [1], or whenever the *Inhibit* pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained. [2] Figure 3-9 shows an application circuit that applies an external bias voltage to a ATH26K12 during startup. The supply voltage superviser, U_1, holds the output of the module off via its Inhibit pin until the voltage, V_1 (3.3 V), has first been applied to the ASIC. As V_1 rises, some of the voltage appears at the module's output. The start-up waveforms are shown in Figure 3-10. Note that the output current from the ATH26K12 (I_2) shows no negative current until it raises the output voltage to full regulation (2.5 V).

Note: The pre-bias start-up feature is not compatible with Auto-Track™. When the module is under Auto-Track™ control, it will sink current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off the Auto-Track™ function must either be disabled [3], or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

Notes

1. Startup includes the short delay (approx. 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the *Track* pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the output voltage throughout the power-up and power-down sequence.
3. The Auto-Track™ function can be disabled at power up by immediately applying a voltage to the module's *Track* pin that is greater than its set-point voltage. This can be easily accomplished by connecting the *Track* pin to V_{in}.

Figure 3–10; Pre-Bias Startup Waveforms

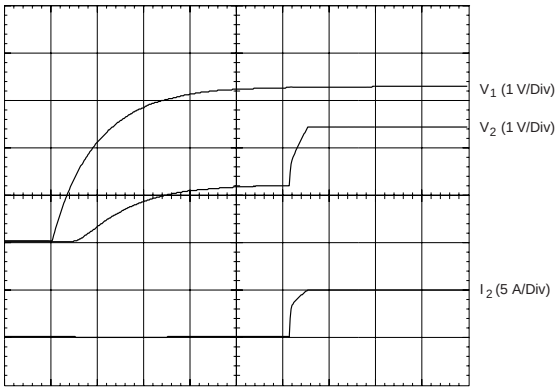
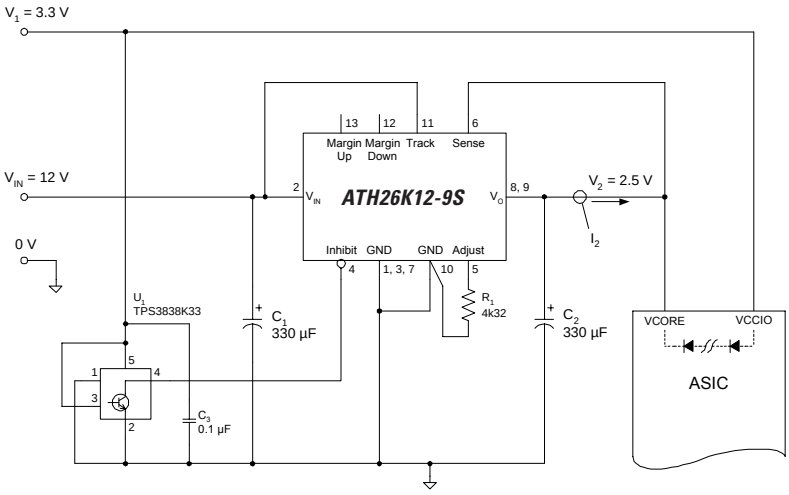


Figure 3–9; Application Circuit Demonstrating Pre-Bias Startup



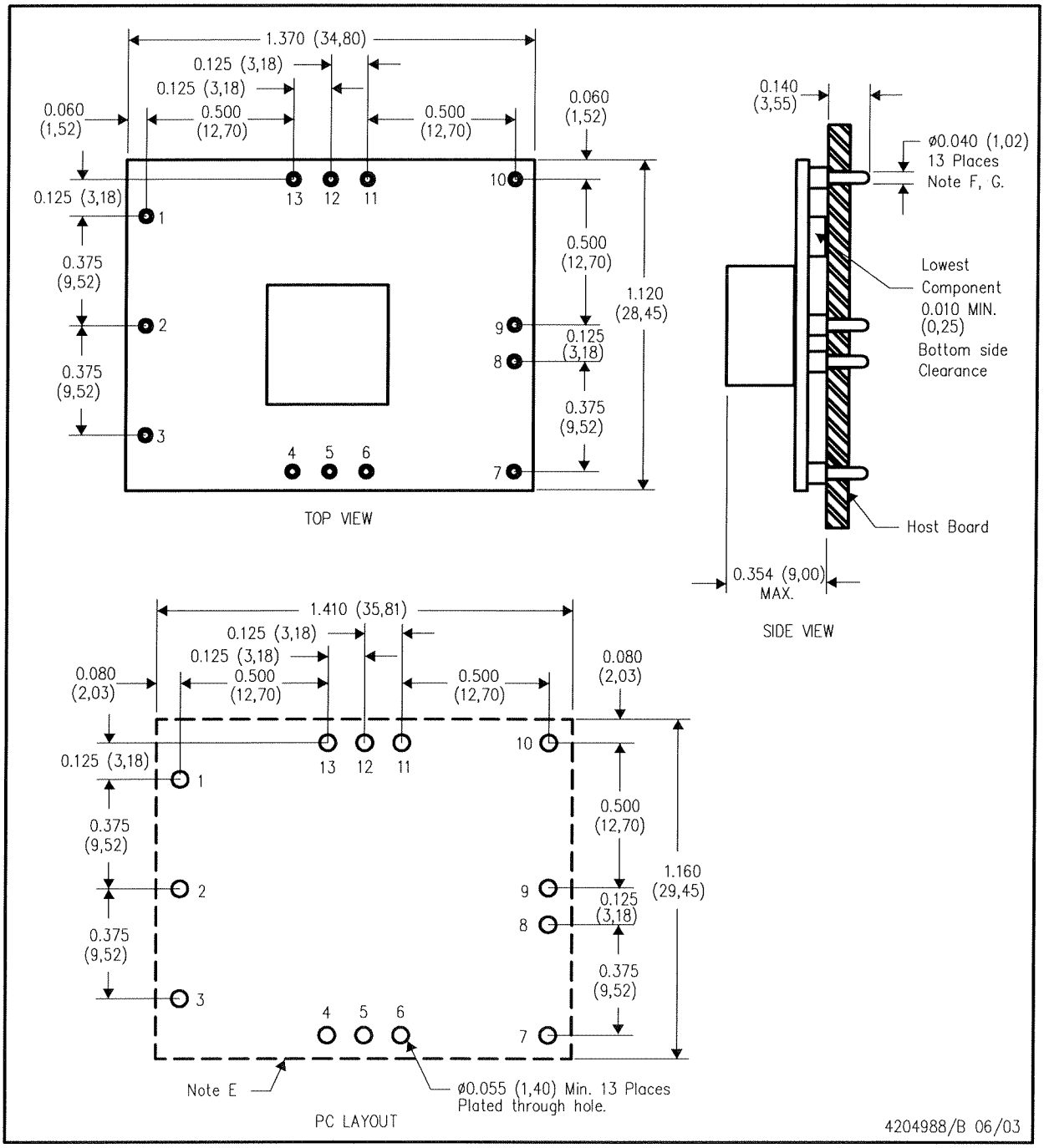
Remote Sense

The ATH10K12, ATH12K12, ATH18K12, and ATH26K12 products incorporate an output voltage sense pin, *V_o Sense*. The *V_o Sense* pin should be connected to V_{out} at the load circuit (see data sheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the *V_o Sense* pin can be left open-circuit. An internal low-value resistor (15-Ω or less) is connected between the *V_o Sense* and V_{out}. This ensures the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and *GND* pins, and that measured from *V_o Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

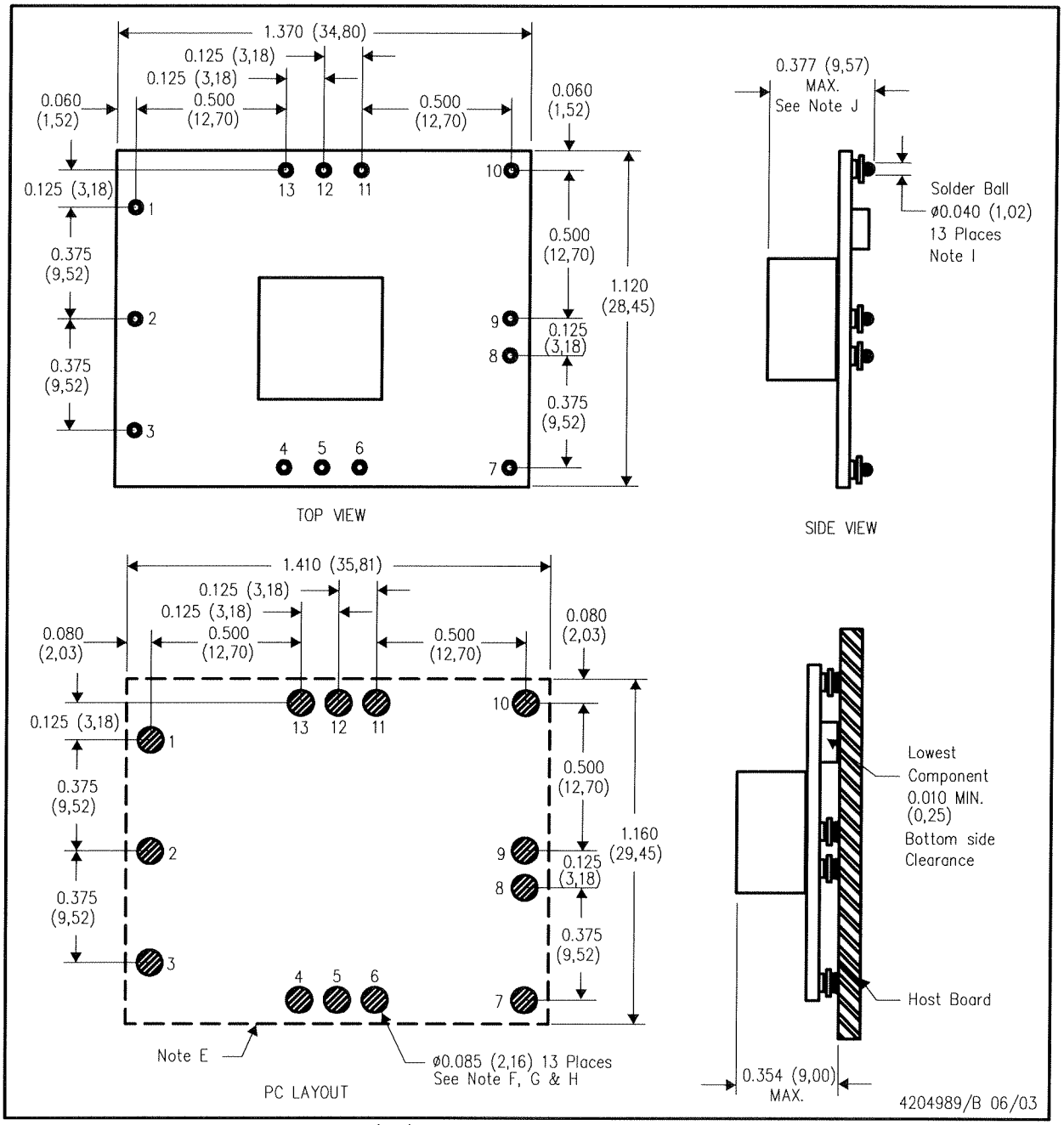
Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

ATH26/30 **THROUGH HOLE TERMINATION**



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

ATH26/30 **SURFACE MOUNT TERMINATION**



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.