AEGIS
SEMICONDUTORES LTDA.

A5N:850.XXH

VOLTAGE RATINGS

Part Number	V_{RRM} , VR (V) Max. rep. peak reverse voltage		V_{RSM} , V_R (V) Max. non-rep. peak reverse voltage
	T_J = 0 to 125°C	T_J = -40 to 0°C	TJ = 25 to 125°C
A5N:850.12H	1200	1200	1300
A5N:850.14H	1400	1400	1500
A5N:850.16H	1600	1600	1700
A5N:850.18H	1800	1800	1900
A5N:850.20H	2000	2000	2100

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T_J Junction Temperature	-40 to 125	°C	-
T_{stg} Storage Temperature	-40 to 150	°C	-
$I_{T(AV)}$ Max. Av. current	850	A	180° half sine wave
$I_{T(AV)}$ @ Max. T_C	75	°C	180° half sine wave
$I_{T(RMS)}$ Nom. RMS current	1320	A	-
I_{TSM} Max. Peak non-rep. surge current	14.80	kA	50 Hz half cycle sine wave; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	16.13		60 Hz half cycle sine wave; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	16.88		50 Hz half cycle sine wave; Initial T_J = 125°C, no voltage applied after surge.
	18.40		60 Hz half cycle sine wave; Initial T_J = 125°C, no voltage applied after surge.
I^2t Max. I^2t capability	1138	kA^2s	t = 10ms; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	1240		t = 8.3 ms; Initial T_J = 125°C, rated V_{RRM} applied after surge.
	1298		t = 10ms; Initial T_J = 125°C, no voltage applied after surge.
	1415		t = 8.3 ms; Initial T_J = 125°C, no voltage applied after surge.
$I^2t^{1/2}$ Max. $I^2t^{1/2}$ capability	15500	$kA^2s^{1/2}$	Initial T_J = 125°C, no voltage applied after surge. I^2t for time $t_x = I^2t^{1/2} * t_x^{1/2}$. (0.1 < tx < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	800	A/ s	T_J = 125°C, $V_D = V_{DRM}$, I_{TM} = 1600A. Gate pulse: 20V, 20 , 10 s, 0.5 s rise time, Max. repetitive di/dt is aproximately 40% of non-repetitive value.
P_GM Max. Peak gate power	16	W	tp < 5 ms
$P_{G(AV)}$ Max. Av. gate power	3	W	-
$+I_{GM}$ Max. Peak gate current	150	mA	tp < 5 ms
$-V_{GM}$ Max. Peak negative gate voltage	2	V	-
F Mounting Force	1550	N.m	-

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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	---	1.75	V	Initial T_J = 25°C, 50-60Hz half sine, I_{peak} = 2670A.
$V_{T(TO)}$ Threshold voltage	---	---	0.908	V	T_J = 125°C Av. power = $V_{T(TO)}$ * $I_{T(AV)}$ +r_T * $[I_{T(RMS)}]^2$, 180° Half Sine.
r_T Slope resistance	---	---	0.348	m	Use low values for I_{TM} < rated $I_{T(AV)}$
I_L Latching current	---	---	400	mA	T_C = 125°C, 12V anode. Gate pulse: 10V, 20 , 100 s.
I_H Holding current	---	---	500	mA	T_C = 25°C, 12V anode. Initial I_T = 15A.
t_d Delay time	---	0.7	1	s	T_C = 25°C, V_D = V_{DRM}, 50A resistive load. Gate pulse: 10V, 20 , 10 s, 1 s rise time.
t_q Turn-off time	---	---	100	s	T_J = 125°C, I_{TM} = 550A, di/dt = 40A/ s, V_R = 50V. dv/dt = 20 V/ s lin. to rated V_{DRM}. Gate: 0V, 100 .
dv/dt Critical rate-of-rise of off-state voltage	---	---	1000	V/ s	T_J = 125°C, Exp. To 67% V_{DRM}, gate open.
I_{RM}, I_{DM} Peak reverse and off-state current	---	30	60	mA	T_J = 125°C, Rated V_{RRM} and V_{DRM}, gate open.
I_{GT} DC gate current to trigger	---	---	360	mA	T_C = -40°C
	---	---	180		T_C = 25°C +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
V_{GT} DC gate voltage to trigger	6	---	---	V	T_C = -40°C
	3	---	---		T_C = 25°C
V_{GD} DC gate voltage not to trigger	---	---	0.3	V	T_C = 25°C, Max. Value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.035	°C/W	DC operation, double side cooled.
	---	---	0.041	°C/W	180° sine wave, double side cooled.
	---	---	0.042	°C/W	120° rectangular wave, double side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.015	°C/W	Mtg. Surface smooth, flat and greased. Double side cooled.
wt Weight	---	255(9.3)	---	g(oz.)	---
Case Style	TO-200AC			JEDEC	---

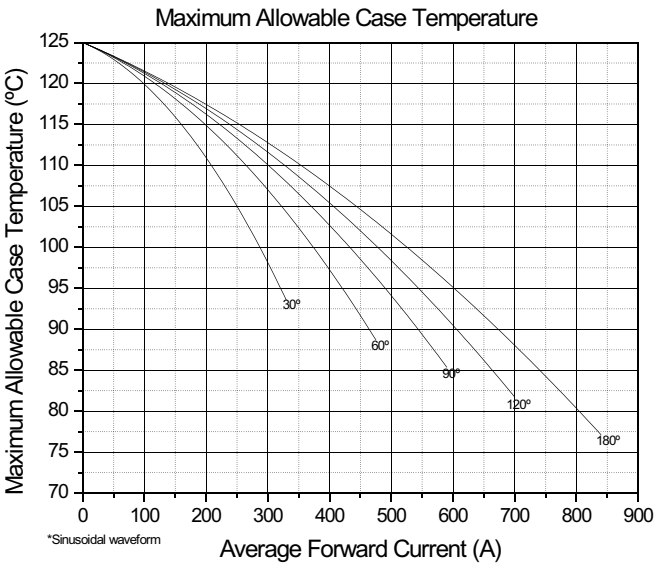

Fig. 1 - Current Ratings Characteristics

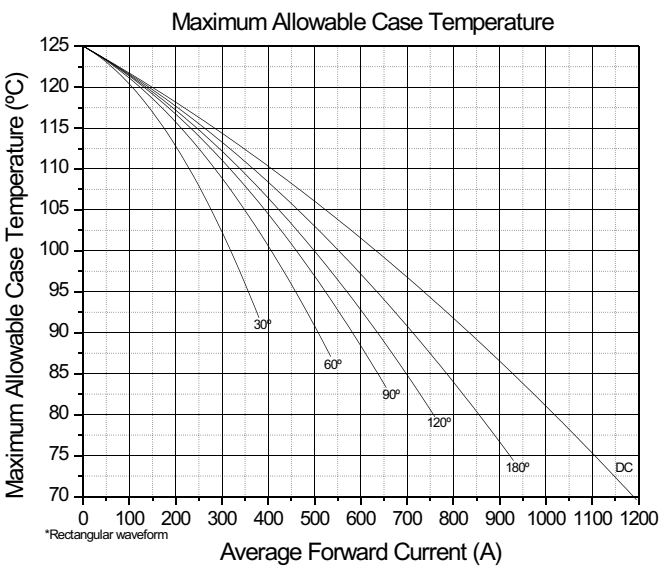

Fig. 2 - Current Ratings Characteristics

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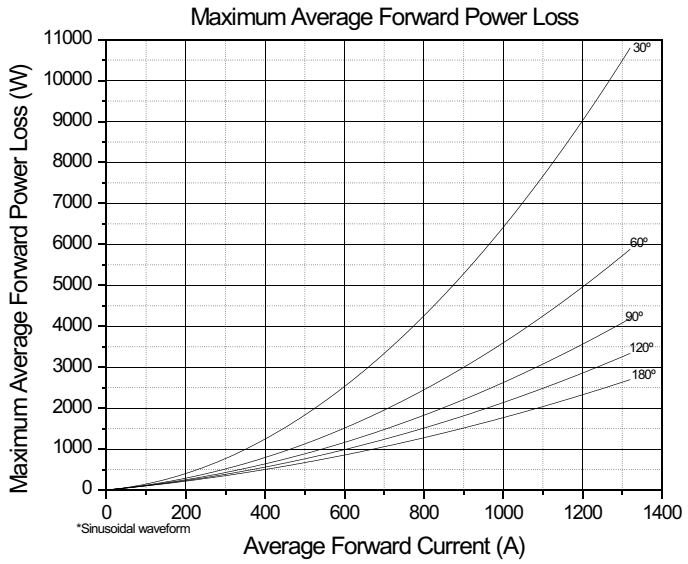

Fig. 3 - Forward Power Loss Characteristics

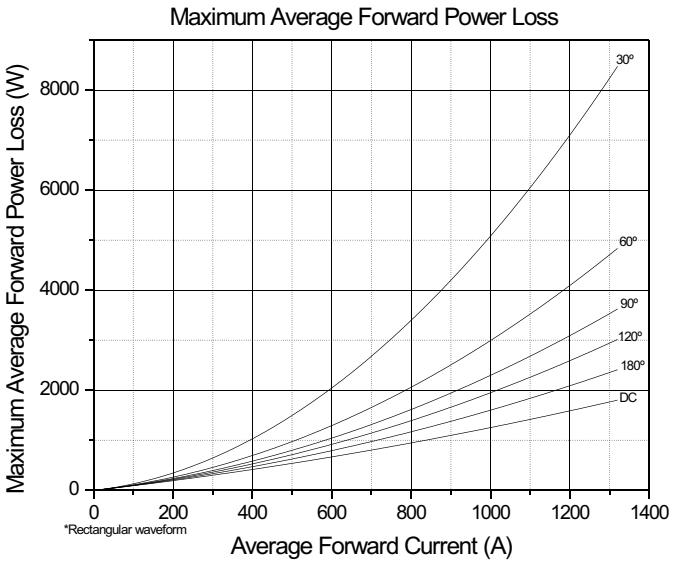

Fig. 4 - Forward Power Loss Characteristics

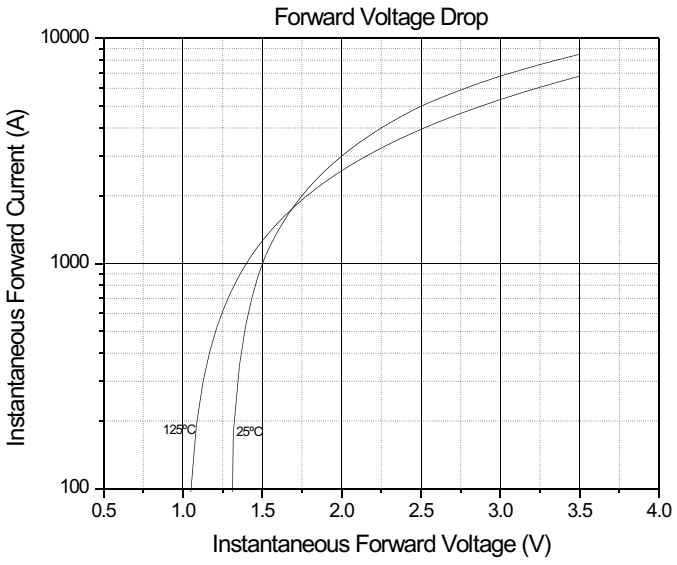

Fig. 5 - Forward Voltage Drop Characteristics

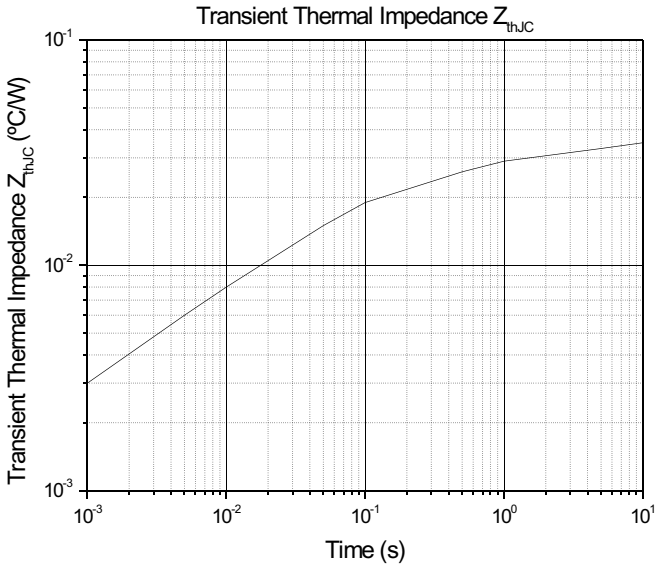

Fig. 6 - Transient Thermal Impedance Characteristics

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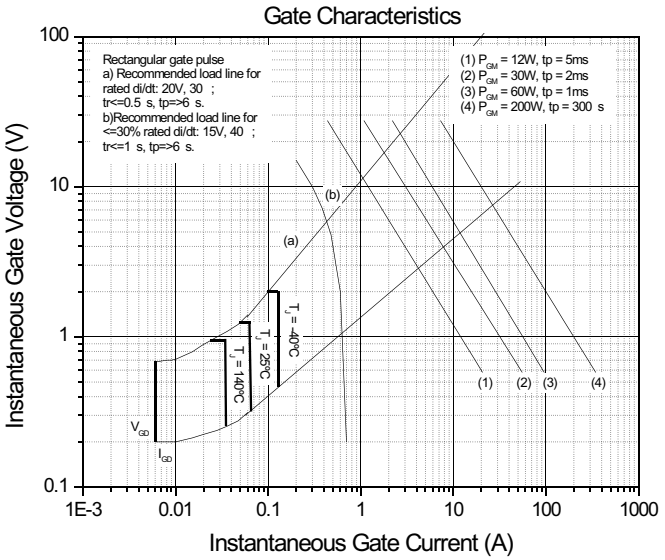

Fig. 7 - Gate Trigger Characteristics

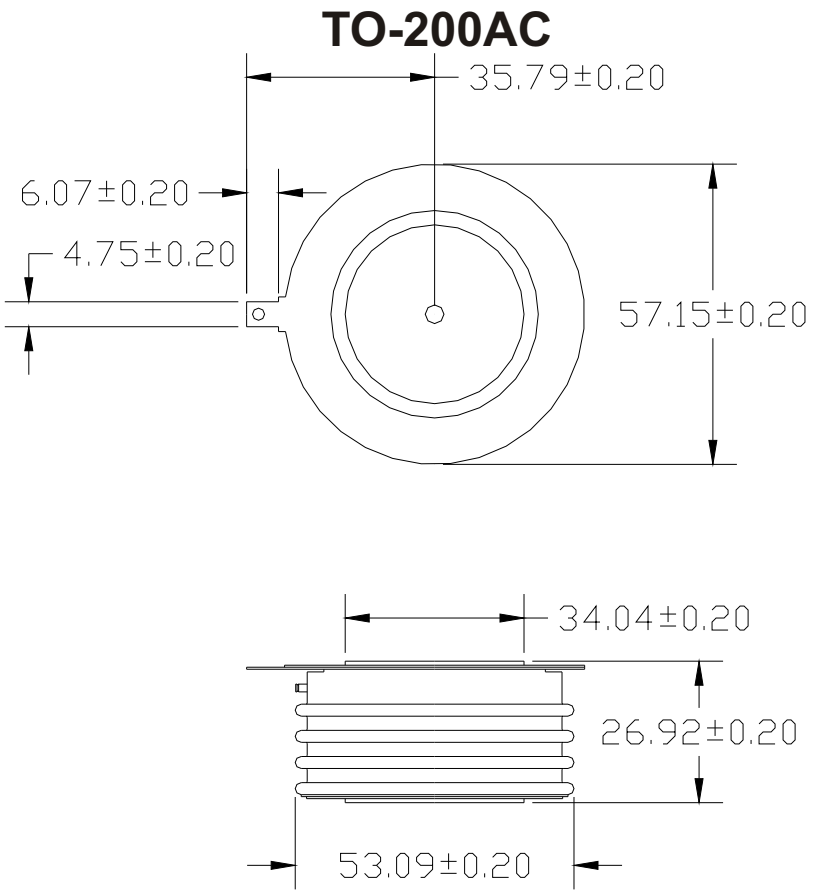

Fig. 8 - Outline Characteristics