

## 8-bit Microcontrollers

CMOS

# F<sup>2</sup>MC-8FX MB95100B Series

**MB95107B/F108BS/F108BW/D108BS/D108BW/  
MB95FV100D-101**

### ■ DESCRIPTION

The MB95100B series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU MICROELECTRONICS Flexible Microcontroller.

### ■ FEATURE

- F<sup>2</sup>MC-8FX CPU core
  - Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instruction
    - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock (for dual clock product)
  - Sub PLL clock (for dual clock product)

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page  
URL : <http://edevic.fujitsu.com/micom/en-support/>

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

# MB95100B Series

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- Timer
  - 8/16-bit compound timer × 2 channels  
Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 16-bit reload timer × 1 channel
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 2 channels
  - Timebase timer × 1 channel
  - Watch prescaler (for dual clock product) × 1 channel
- FRAM
  - 2 K bytes FRAM is loaded (MB95D108BS/MB95D108BW only)
- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- UART/SIO × 1 channel
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- I<sup>2</sup>C\* × 1 channel
  - Built-in wake-up function
- External interrupt × 12channels
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 12channels
  - 8-bit or 10-bit resolution can be selected.
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O port
  - The number of maximum ports
    - Single clock product : 55 ports
    - Dual clock product : 53 ports
  - Port configuration
    - General-purpose I/O ports (N-ch open drain)
      - Other than MB95D108BS/MB95D108BW : 6 ports
      - MB95D108BS/MB95D108BW : 4 ports
    - General-purpose I/O ports (CMOS)
      - Single clock product : 49 ports
      - Dual clock product : 47 ports

\* : Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# MB95100B Series

## ■ PRODUCT LINEUP

Part number		MB95107B	MB95F108BS/ MB95F108BW	MB95D108BS/ MB95D108BW
Parameter				
Type		MASK ROM product	Flash memory product	Flash memory product
ROM capacity		48 K bytes	60 K bytes	60 K bytes
RAM capacity		2 K bytes		
FRAM capacity		No		2 K bytes
Reset output		No		
Option*3	Clock system	Selectable Single/Dual clock*1	Single/Dual clock*2	Single/Dual clock*2
	Low voltage detection reset	No		
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 μs (at machine clock frequency 16.25 MHz)		
Peripheral functions	General purpose I/O ports	<ul style="list-style-type: none"> <li>• Single clock product : 55 ports (N-ch open drain *4 : 4/6 ports, CMOS : 49 ports)</li> <li>• Dual clock product : 53 ports (N-ch open drain *4 : 4/6 ports, CMOS : 47 ports)</li> </ul>		
	Timebase timer (1 channel)	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)		
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms		
	Wild register	Capable of replacing 3 bytes of ROM data		
	I <sup>2</sup> C (1 channel)	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function		
	UART/SIO (1 channel)	Data transfer capable in UART/SIO Full duplex double buffer, Variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable		
	LIN-UART (1 channel)	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.		
8/10-bit A/D converter (12 channels)	8-bit or 10-bit resolution can be selected.			

(Continued)

# MB95100B Series

(Continued)

Part number		MB95107B	MB95F108BS/ MB95F108BW	MB95D108BS/ MB95D108BW
Parameter				
Peripheral functions	16-bit reload timer (1 channel)	Two clock modes and two counter operating modes can be selected. Square wave form output Count clock : 7 internal clocks and external clock can be selected. Counter operating mode : reload mode or one-shot mode can be selected.		
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”. Built-in timer function, PWC function, PWM function, capture function and square wave form output Count clock : 7 internal clocks and external clock can be selected.		
	16-bit PPG (2 channels)	PWM mode or one-shot mode can be selected. Counter operating clock : 8 selectable clock sources Support for external trigger start		
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : 8 selectable clock sources		
	Watch counter (for dual clock product)	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)		
	Watch prescaler (for dual clock product) (1 channel)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)		
	External interrupt (12 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.		
	Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Erase can be performed on each block Boot block configuration Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash		
Standby mode	Sleep, stop, watch (for dual clock product), and timebase timer			

\*1 : Specify clock mode when ordering MASK ROM.

\*2 : MB95F108BS/MB95D108BS is single clock and MB95F108BW/MB95D108BW is dual clock.

\*3 : For details of option, refer to “■ MASK OPTION”.

\*4 : MB95D108BS/D108BW contain 4 general-purpose I/O ports for N-ch open drain. Port number other than MB95D108BS/D108BW has 6 general-purpose I/O ports for N-ch open drain.

Note : Part number of the evaluation products in MB95100B series is MB95FV100D-101. When using it, the MCU board (MB2146-301A) is required.

## ■ SELECT OF OSCILLATION STABILIZATION WAIT TIME (MASK ROM PRODUCT ONLY)

For the MASK ROM product, you can set the mask option when ordering MASK ROM to select the initial value of main clock oscillation stabilization wait time from among the following four values.

Note that the evaluation and Flash memory products are fixed their initial value of main clock oscillation stabilization wait time at the maximum value.

Select of oscillation stabilization wait time	Remarks
$(2^2 - 2) / F_{CH}$	0.5 $\mu$ s (at main oscillation clock 4 MHz)
$(2^{12} - 2) / F_{CH}$	Approx. 1.02 ms (at main oscillation clock 4 MHz)
$(2^{13} - 2) / F_{CH}$	Approx. 2.05 ms (at main oscillation clock 4 MHz)
$(2^{14} - 2) / F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

## ■ PACKAGES AND CORRESPONDING PRODUCTS

Part number Package	MB95107B	MB95F108BS/ MB95F108BW	MB95D108BS/ MB95D108BW	MB95FV100D-101
FPT-64P-M03	○	○	○	×
FPT-64P-M09	○	○	○	×
BGA-96P-M04	○	○	×	×
BGA-224P-M08	×	×	×	○

○ : Available

× : Unavailable

# MB95100B Series

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

### • Notes on Using Evaluation Products

The evaluation product has not only the functions of the MB95100B series but also those of other products to support software development for multiple series and models of the F<sup>2</sup>MC-8FX family. The I/O addresses for peripheral resources not used by the MB95100B series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory and MASK ROM products, do not use these values in the program.

The evaluation product do not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. The evaluation, Flash memory, and MASK ROM products are designed to behave completely the same way in terms of hardware and software.

### • Difference of Memory Spaces

If the amount of memory on the evaluation product is different from that of the Flash memory or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

### • Current Consumption

The current consumption of Flash memory product is greater than for MASK ROM product.  
For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

### • Package

For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

### • Operating voltage

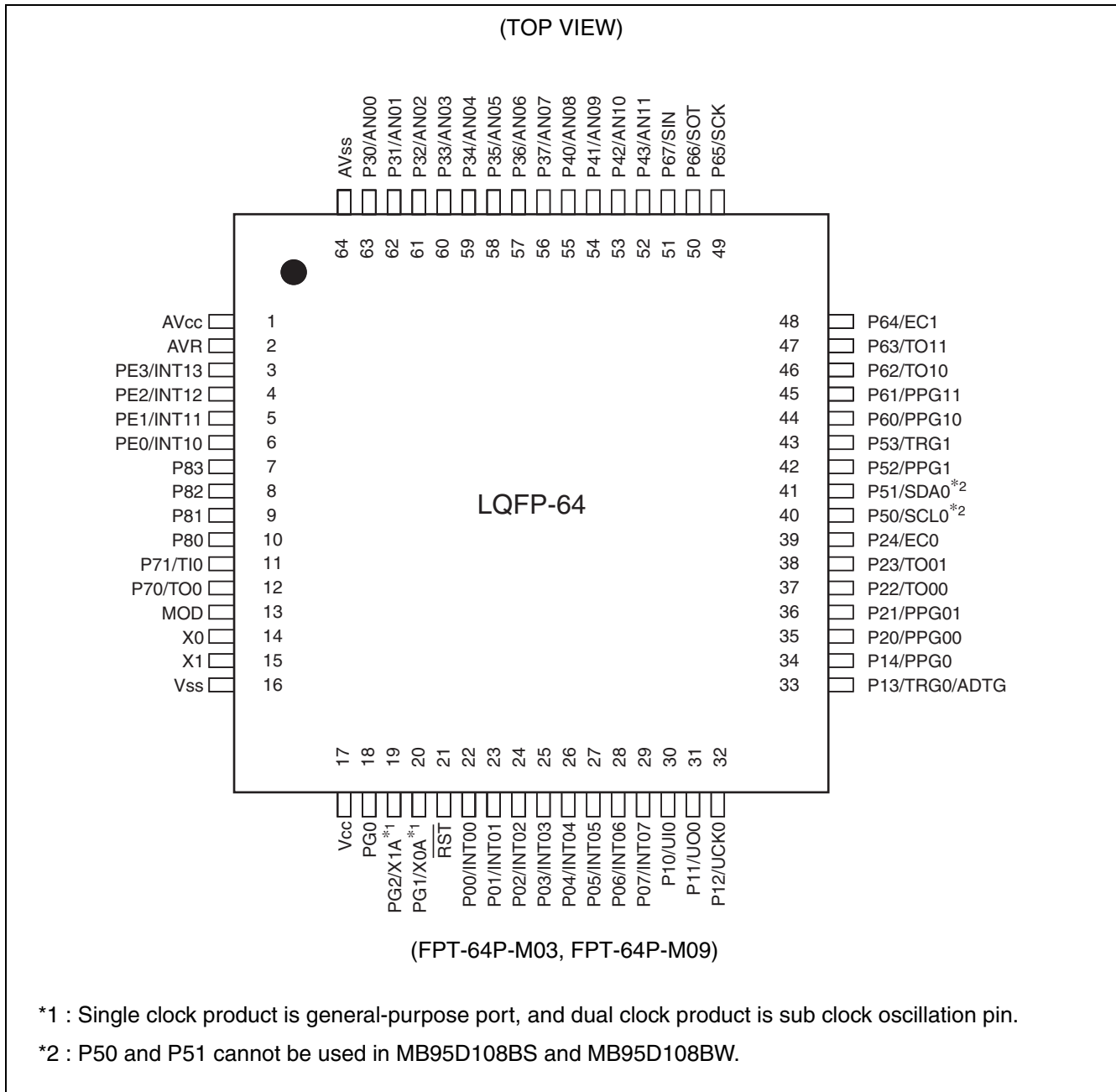
The operating voltage are different among the evaluation, Flash memory, and MASK ROM products.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

### • Difference between $\overline{RST}$ and MOD pins

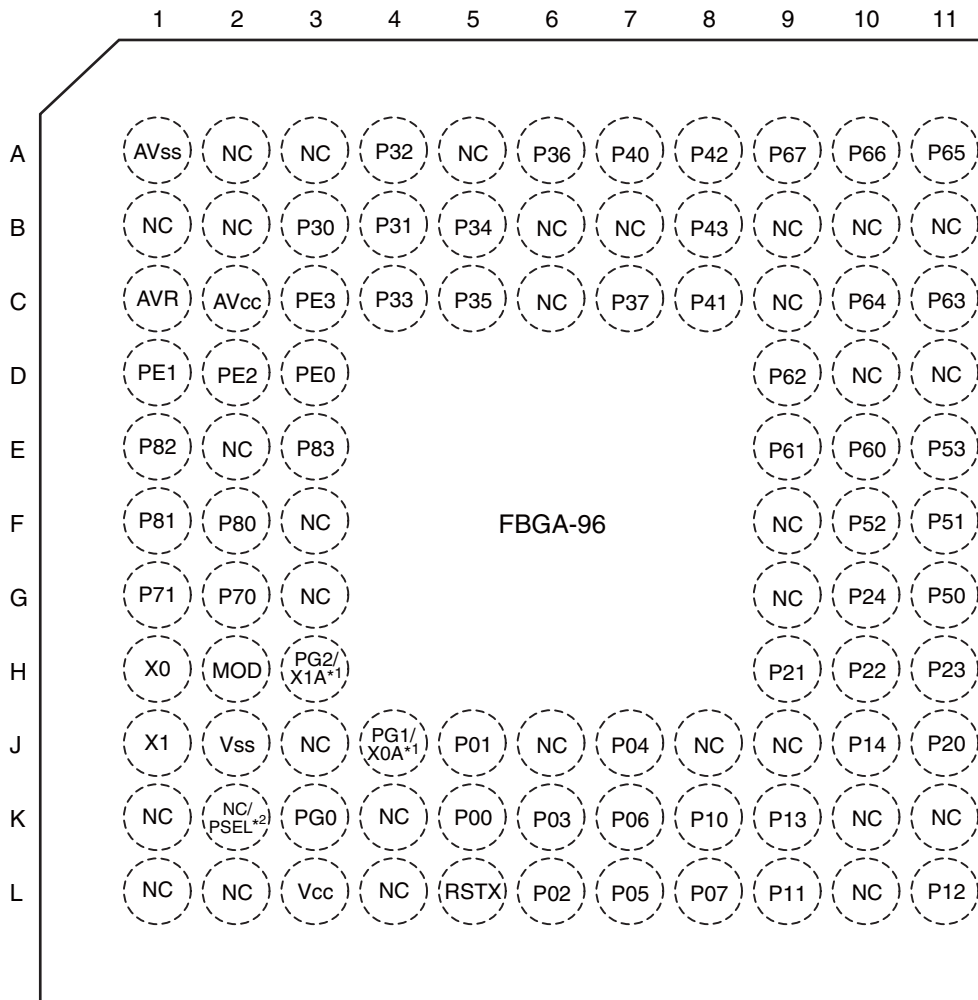
The input type of  $\overline{RST}$  and MOD pins is CMOS input on the Flash memory product. The  $\overline{RST}$  and MOD pins are hysteresis inputs on the MASK ROM product. A pull - down resistor is provided for the MOD pin of the MASK ROM product.

## PIN ASSIGNMENT



# MB95100B Series

(TOP VIEW)



(BGA-96P-M04)

\*1 : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

\*2 : This pin becomes NC in Mask ROM product, and PSEL in flash memory product.  
Connect to Vcc in MB95F108BS and connect to Vss in MB95F108BW.



## ■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
LQFP64*1	FBGA96*2			
1	C2	AV <sub>CC</sub>	—	A/D converter power supply pin
2	C1	AVR	—	A/D converter reference input pin
3	C3	PE3/INT13	P	General-purpose I/O port The pins are shared with the external interrupt input.
4	D2	PE2/INT12		
5	D1	PE1/INT11		
6	D3	PE0/INT10		
7	E3	P83	O	General-purpose I/O port
8	E1	P82		
9	F1	P81		
10	F2	P80		
11	G1	P71/TI0	H	General-purpose I/O port. The pin is shared with 16 - bit reload timer ch.0 input.
12	G2	P70/TO0		General-purpose I/O port. The pin is shared with 16 - bit reload timer ch.0 output.
13	H2	MOD	B	An operating mode designation pin
14	H1	X0	A	Main clock input oscillation pin
15	J1	X1		Main clock input/output oscillation pin
16	J2	V <sub>SS</sub>	—	Power supply pin (GND)
17	L3	V <sub>CC</sub>	—	Power supply pin
18	K3	PG0	H	General-purpose I/O port.
19	H3	PG2/X1A	H/A	Single-system product is general-purpose port (PG2). Dual-system product is sub clock input/output oscillation pin (32 kHz).
20	J4	PG1/X0A		Single-system product is general-purpose port (PG1). Dual-system product is sub clock input oscillation pin (32 kHz).
21	L5	$\overline{\text{RST}}$	B'	Reset pin
22	K5	P00/INT00	C	General-purpose I/O port. The pins are shared with external interrupt input. Large current port.
23	J5	P01/INT01		
24	L6	P02/INT02		
25	K6	P03/INT03		
26	J7	P04/INT04		
27	L7	P05/INT05		
28	K7	P06/INT06		
29	L8	P07/INT07		
30	K8	P10/UI0	G	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data input.

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# MB95100B Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP64*1	FBGA96*2			
31	L9	P11/UO0	H	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data output.
32	L11	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch.0 clock I/O.
33	K9	P13/TRG0/ ADTG		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG).
34	J10	P14/PPG0		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 output.
35	J11	P20/PPG00		General-purpose I/O port.
36	H9	P21/PPG01		The pins are shared with 8/16-bit PPG ch.0 output.
37	H10	P22/TO00		General-purpose I/O port.
38	H11	P23/TO01		The pins are shared with 8/16-bit compound timer ch.0 output.
39	G10	P24/EC0		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.0 clock input.
40	G11	P50/SCL0	I	General-purpose I/O port (Except MB95D108BS and MB95D108BW). The pin is shared with I <sup>2</sup> C ch.0 clock I/O.
41	F11	P51/SDA0		General-purpose I/O port (Except MB95D108BS and MB95D108BW). The pin is shared with I <sup>2</sup> C ch.0 data I/O.
42	F10	P52/PPG1	H	General-purpose I/O port. The pin is shared with 16-bit PPG ch.1 output.
43	E11	P53/TRG1		General-purpose I/O port. The pin is shared with 16-bit PPG ch.1 trigger input.
44	E10	P60/PPG10	K	General-purpose I/O port.
45	E9	P61/PPG11		The pins are shared with 8/16-bit PPG ch.1 output.
46	D9	P62/TO10		General-purpose I/O port.
47	C11	P63/TO11		The pins are shared with 8/16-bit compound timer ch.1 output.
48	C10	P64/EC1		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.1 clock input.
49	A11	P65/SCK		General-purpose I/O port. The pin is shared with LIN-UART clock I/O.
50	A10	P66/SOT		General-purpose I/O port. The pin is shared with LIN-UART data output.

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# MB95100B Series

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP64*1	FBGA96*2			
51	A9	P67/SIN	L	General-purpose I/O port. The pin is shared with LIN-UART data input.
52	B8	P43/AN11	J	General-purpose I/O port. The pins are shared with A/D converter analog input.
53	A8	P42/AN10		
54	C8	P41/AN09		
55	A7	P40/AN08		
56	C7	P37/AN07		
57	A6	P36/AN06		
58	C5	P35/AN05		
59	B5	P34/AN04		
60	C4	P33/AN03		
61	A4	P32/AN02		
62	B4	P31/AN01		
63	B3	P30/AN00		
64	A1	AV <sub>SS</sub>	—	A/D converter power supply pin (GND)
—	K2	NC/PSEL	—	Internally connected pins for MASK ROM products. Be sure to leave it open. Connect V <sub>CC</sub> in MB95F108BS, and V <sub>SS</sub> in MB95F108BW for the Flash memory products.
—	A2, A3, A5, B1, B2, B6,B7, B9, B10,B11, C6, C9,D10, D11,E2, F3, F9,G3, G9, J3,J6, J8, J9,K1, K4, K10,K11, L1, L2,L4, L10	NC	—	Internally connected pins. Be sure to leave it open.

\*1 : FPT-64P-M03, FPT-64P-M09

\*2 : BGA-96P-M04

\*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

# MB95100B Series

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• High-speed side Feedback resistance value : approx. 1 MΩ</li> <li>• Low-speed side Feedback resistance : approx. 24 MΩ (Evaluation product : approx. 10 MΩ) Dumping resistance : approx. 144 kΩ (Evaluation product : without dumping resistance)</li> </ul>
B		<ul style="list-style-type: none"> <li>• Only for input</li> <li>Hysteresis input only for MASK ROM product</li> <li>With pull-down resistor only for MASK ROM product</li> </ul>
B'		Hysteresis input only for MASK ROM product
C		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
G		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>

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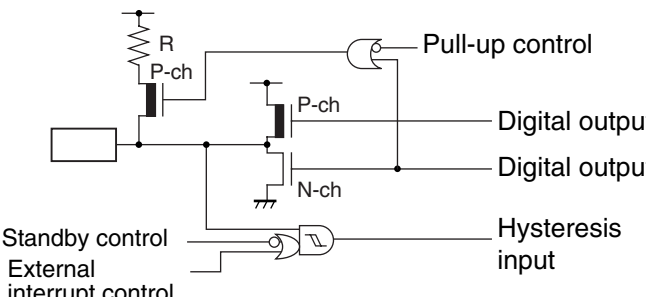
# MB95100B Series

Type	Circuit	Remarks
I	<p>Standby control</p> <p>P-ch</p> <p>N-ch</p> <p>Digital output</p> <p>CMOS input</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• N-ch open drain output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• P-ch transistor is existed in MB95D108BS and MB95D108BW.</li> </ul>
J	<p>R</p> <p>P-ch</p> <p>P-ch</p> <p>N-ch</p> <p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Analog input</p> <p>A/D control</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> <li>• With pull-up control</li> </ul>
K	<p>P-ch</p> <p>N-ch</p> <p>Digital output</p> <p>Digital output</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
L	<p>P-ch</p> <p>N-ch</p> <p>Digital output</p> <p>Digital output</p> <p>Standby control</p> <p>CMOS input</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> </ul>
O	<p>N-ch</p> <p>Digital output</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• N-ch open drain output</li> <li>• Hysteresis input</li> </ul>

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# MB95100B Series

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Type	Circuit	Remarks
P	 <p>The circuit diagram shows a CMOS output stage. It consists of a pull-up resistor (R) connected to a supply rail. The output node is connected to the gates of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to the supply rail, and its drain is connected to the output node. The N-ch MOSFET's source is connected to ground, and its drain is connected to the output node. A pull-up control signal is connected to the gate of the P-ch MOSFET. A hysteresis input signal is connected to the gate of the N-ch MOSFET. The output node is connected to two digital output pins. A standby control signal and an external interrupt control signal are connected to the gates of the P-ch and N-ch MOSFETs, respectively.</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>

## ■ HANDLING DEVICES

- Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage ( $AV_{CC}$ ,  $AVR$ ) and analog input voltage from exceeding the digital power supply voltage ( $V_{CC}$ ) when the analog system power supply is turned on or off.

- Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the  $V_{CC}$  power-supply voltage.

For stabilization, in principle, keep the variation in  $V_{CC}$  ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard  $V_{CC}$  value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

## ■ PIN CONNECTION

- Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage.

Unused input pins should always be pulled up or down through resistance of at least 2 k $\Omega$ . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is an unused output pin, make it open.

- Treatment of Power Supply Pins on A/D Converter

Connect to be  $AV_{CC} = V_{CC}$  and  $AV_{SS} = AVR = V_{SS}$  even if the A/D converter is not in use.

Noise riding on the  $AV_{CC}$  pin may cause accuracy degradation. So, connect approx. 0.1  $\mu$ F ceramic capacitor as a bypass capacitor between  $AV_{CC}$  and  $AV_{SS}$  pins in the vicinity of this device.

- Power Supply Pins

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1  $\mu$ F between  $V_{CC}$  and  $V_{SS}$  pins near this device.

# MB95100B Series

- Mode Pin (MOD)

Connect the MOD pin directly to  $V_{CC}$  or  $V_{SS}$  pins.

To prevent the device unintentionally entering the test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.

- Analog Power Supply

Always set the same potential to  $AV_{CC}$  and  $V_{CC}$  pins. When  $V_{CC} > AV_{CC}$ , the current may flow through the AN00 to AN11 pins.

- Precautions for Use of FRAM

When the device is connected to I<sup>2</sup>C external pins (SCL0 and SDA0), the device with the same slave addresses (1010000<sub>B</sub> to 1010111<sub>B</sub>) as built-in FRAM cannot be used.

When built-in FRAM is used without connecting the device to I<sup>2</sup>C external pins, external pull-up resistor (1.1 k $\Omega$  or more) should be connected to SCL0 and SDA0 pins.

P50 and P51 cannot be used in MB95D108BS and MB95D108BW.



## PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

### Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-64P-M03	TEF110-108F35AP	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-64P-M09	TEF110-108F36AP	
BGA-96P-M04	TEF110-95F108-BGL	

Note : For information on applicable adapter models and parallel programmers, contact the following:  
Flash Support Group, Inc. TEL: +81-53-428-8380

### Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

Flash memory	CPU address	Programmer address*		
SA1 (4K bytes)	1000 <sub>H</sub>	71000 <sub>H</sub>	Lower bank	
	1FFF <sub>H</sub> 2000 <sub>H</sub>	71FFF <sub>H</sub> 72000 <sub>H</sub>		
SA2 (4K bytes)	2FFF <sub>H</sub> 3000 <sub>H</sub>	72FFF <sub>H</sub> 73000 <sub>H</sub>		
	3FFF <sub>H</sub> 4000 <sub>H</sub>	73FFF <sub>H</sub> 74000 <sub>H</sub>		
SA4 (16K bytes)	7FFF <sub>H</sub> 8000 <sub>H</sub>	77FFF <sub>H</sub> 78000 <sub>H</sub>		Upper bank
SA5 (16K bytes)	BFFF <sub>H</sub> C000 <sub>H</sub>	7BFFF <sub>H</sub> 7C000 <sub>H</sub>		
	SA6 (4K bytes)	CFFF <sub>H</sub> D000 <sub>H</sub>		
SA7 (4K bytes)		DFFF <sub>H</sub> E000 <sub>H</sub>		
	SA8 (4K bytes)	EFFF <sub>H</sub> F000 <sub>H</sub>		
SA9 (4K bytes)		FFFF <sub>H</sub>	7FFFF <sub>H</sub>	

\*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.  
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

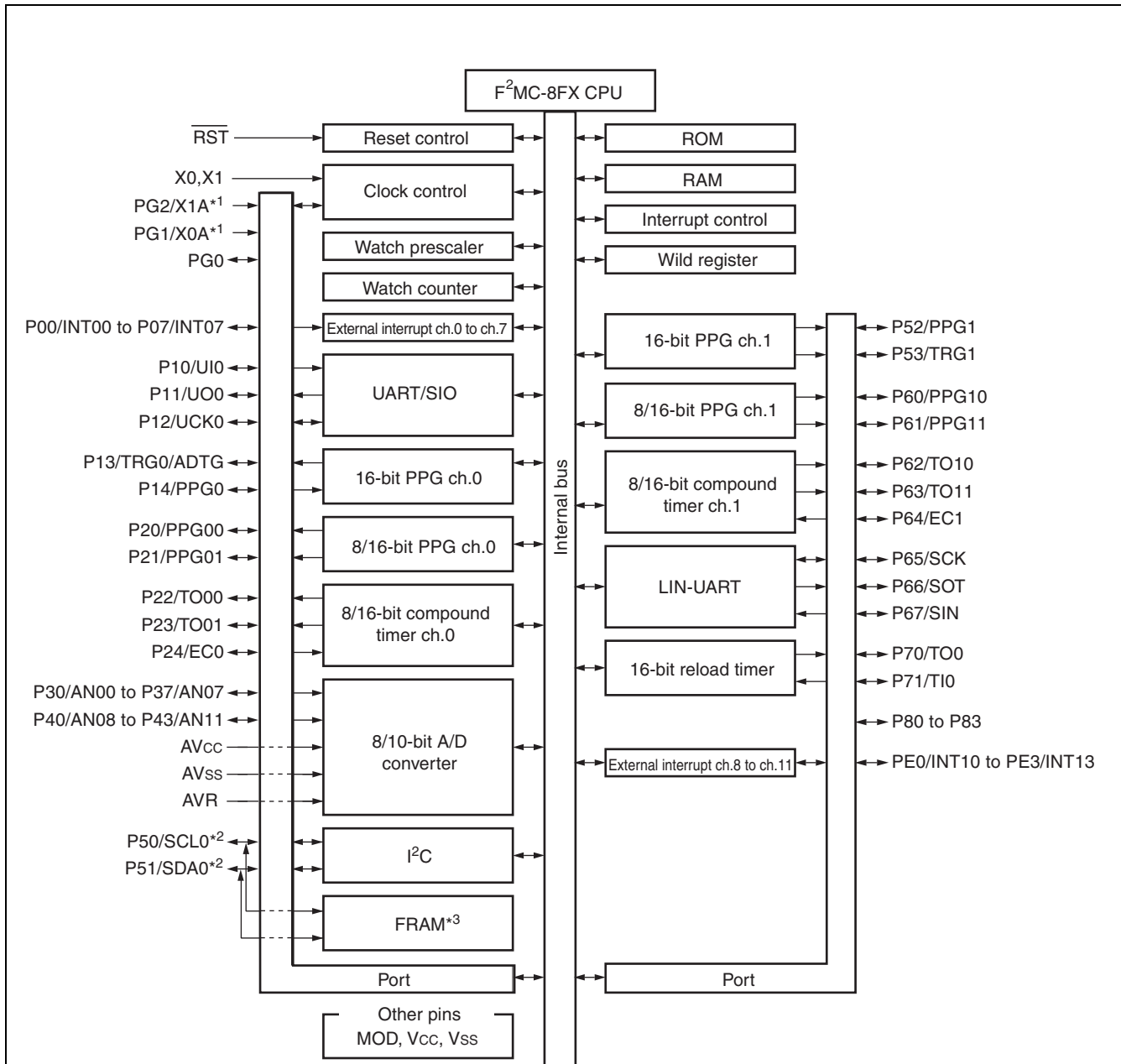
### Programming Method

- 1) Set the type code of the parallel programmer to 17226.
- 2) Load program data to parallel programmer addresses 71000<sub>H</sub> to 7FFFF<sub>H</sub>.

# MB95100B Series

3) Programmed by parallel programmer

## ■ BLOCK DIAGRAM



\*1 : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

\*2 : P50 and P51 cannot be used in MB95D108BS, and MB95D108BW.

\*3 : MB95D108BS and MB95D108BW only

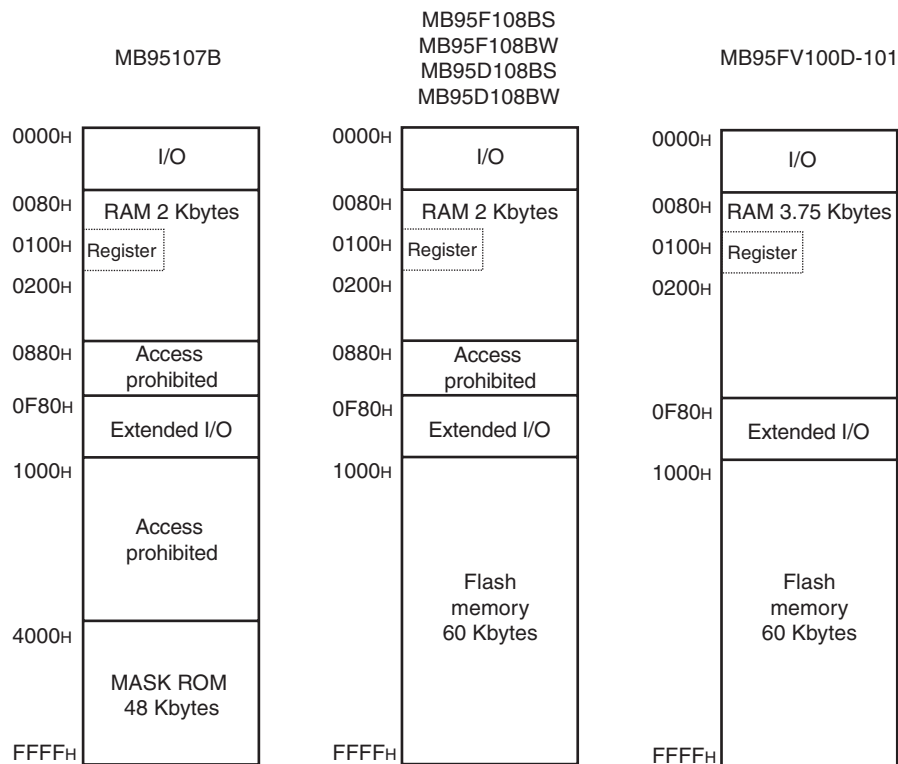
# MB95100B Series

## ■ CPU CORE

### 1. Memory space

Memory space of the MB95100B series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95100B series is shown below.

#### • Memory Map



## 2. Register

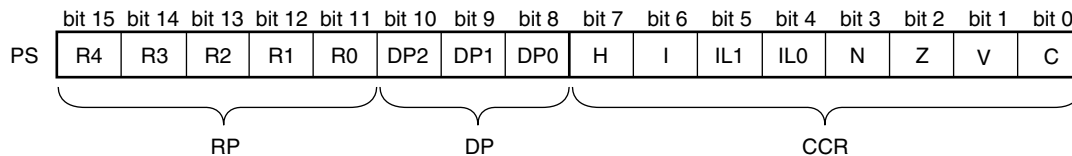
The MB95100B series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored
- Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
- Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer to point to a memory address
- Stack pointer (SP) : A 16-bit register to indicate a stack area
- Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register

16-bit		Initial Value
PC	: Program counter	FFFD <sub>H</sub>
A	: Accumulator	0000 <sub>H</sub>
T	: Temporary accumulator	0000 <sub>H</sub>
IX	: Index register	0000 <sub>H</sub>
EP	: Extra pointer	0000 <sub>H</sub>
SP	: Stack pointer	0000 <sub>H</sub>
PS	: Program status	0030 <sub>H</sub>

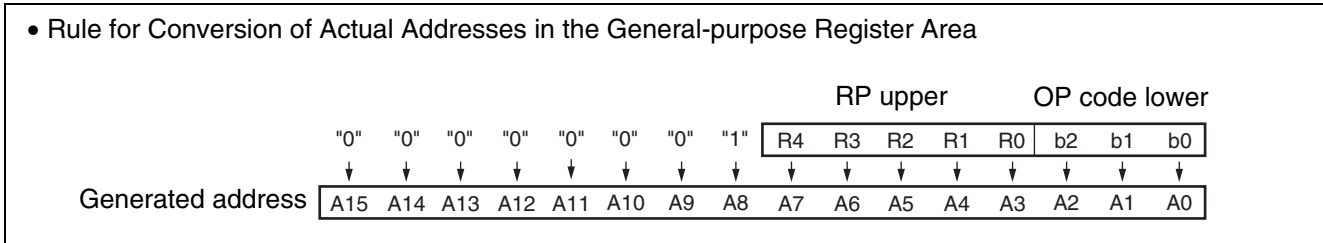
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (Refer to the diagram below.)

### • Structure of the program status



# MB95100B Series

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080H to 00FFH.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX <sub>B</sub> (no effect to mapping)	0000 <sub>H</sub> to 007F <sub>H</sub>	0000 <sub>H</sub> to 007F <sub>H</sub> (without mapping)
000 <sub>B</sub> (initial value)	0080 <sub>H</sub> to 00FF <sub>H</sub>	0080 <sub>H</sub> to 00FF <sub>H</sub> (without mapping)
001 <sub>B</sub>		0100 <sub>H</sub> to 017F <sub>H</sub>
010 <sub>B</sub>		0180 <sub>H</sub> to 01FF <sub>H</sub>
011 <sub>B</sub>		0200 <sub>H</sub> to 027F <sub>H</sub>
100 <sub>B</sub>		0280 <sub>H</sub> to 02FF <sub>H</sub>
101 <sub>B</sub>		0300 <sub>H</sub> to 037F <sub>H</sub>
110 <sub>B</sub>		0380 <sub>H</sub> to 03FF <sub>H</sub>
111 <sub>B</sub>		0400 <sub>H</sub> to 047F <sub>H</sub>

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is cleared to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High ↑ ↓ Low = no interruption
0	1	1	
1	0	2	
1	1	3	

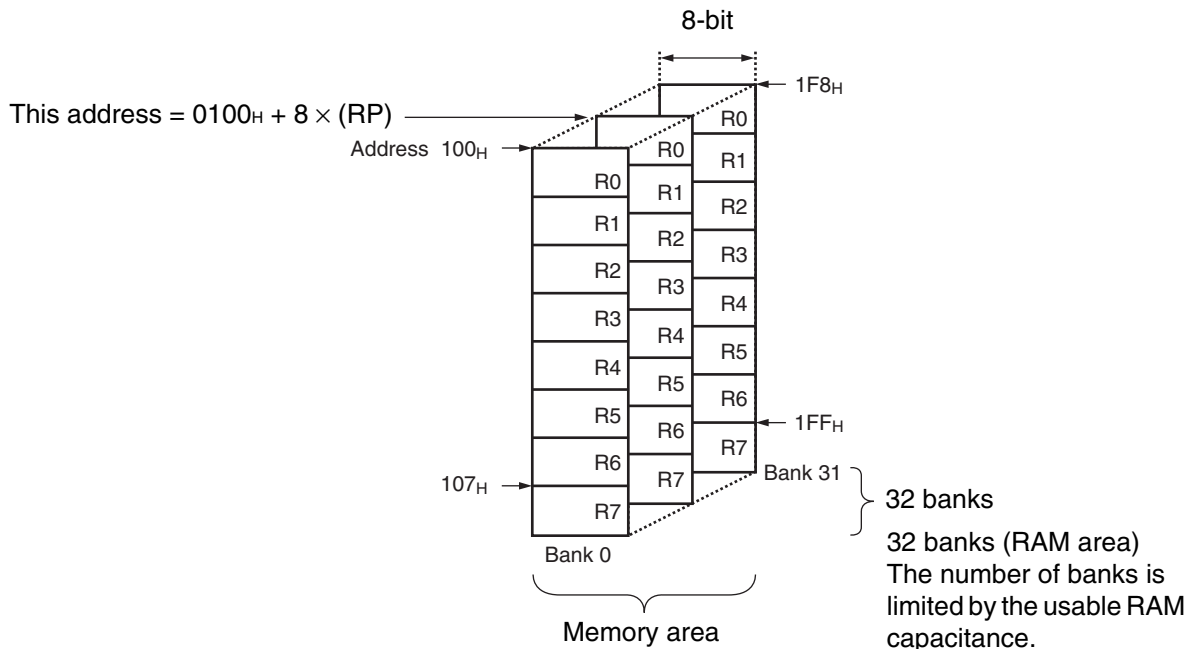
- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95100B series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



# MB95100B Series

## ■ FRAM

### • Slave address of FRAM

FRAM operates as one of the slave devices connected to the I<sup>2</sup>C, and the I<sup>2</sup>C is used to read from or write to FRAM. When data is transferred by the I<sup>2</sup>C, the slave address of FRAM is shown below.

Slave address (7 bits)				R/W bit (1 bit)
Slave ID (4 bits)		Page select bit* (3 bits)		
1	0	1	0	0 : at write 1 : at read
				000 <sub>B</sub> : page 0 001 <sub>B</sub> : page 1 010 <sub>B</sub> : page 2 011 <sub>B</sub> : page 3 100 <sub>B</sub> : page 4 101 <sub>B</sub> : page 5 110 <sub>B</sub> : page 6 111 <sub>B</sub> : page 7

\* : Page select bit : Set the value corresponding to the accessed page

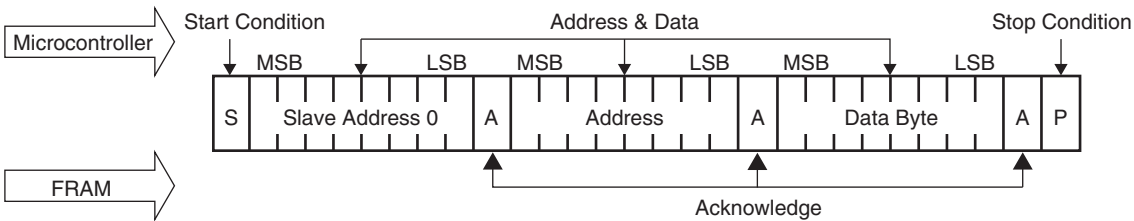
### • Memory configuration of FRAM

The capacitance of the built-in FRAM is 2 Kbytes. The memory configuration of FRAM consists of 8 pages as follows. The capacitance of each page is 256 bytes.

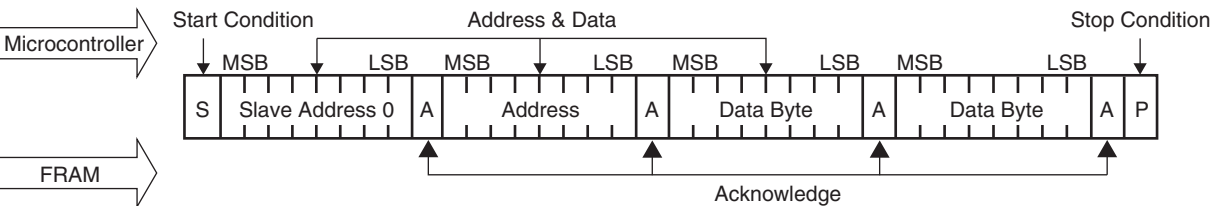
Page	Address	Capacitance
0	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
1	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
2	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
3	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
4	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
5	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
6	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes
7	00 <sub>H</sub> to FF <sub>H</sub>	256 bytes



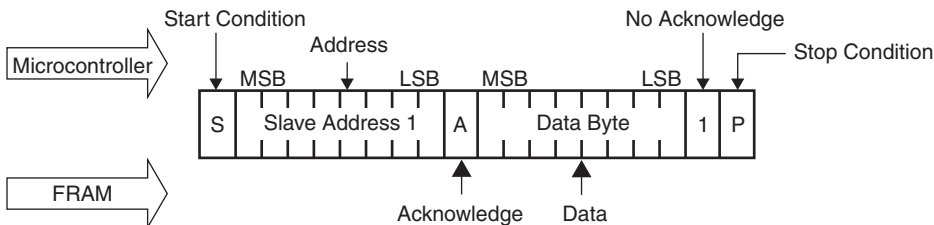
## • Single byte write



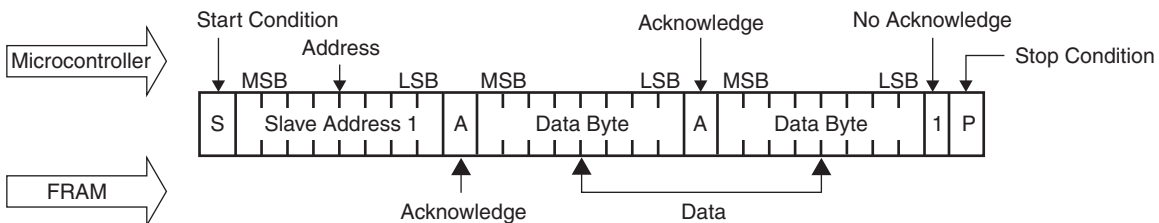
## • Compound byte write



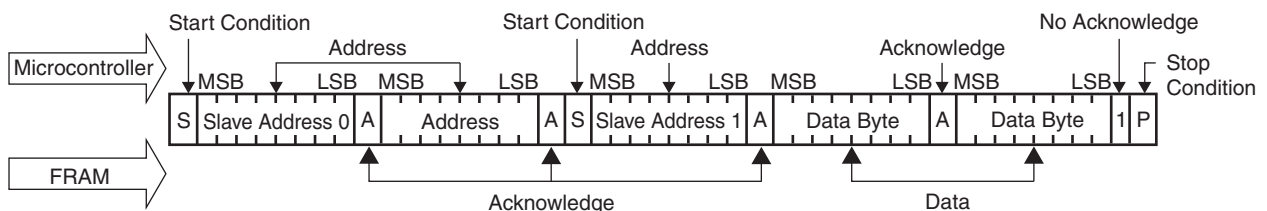
## • Current address read



## • Continuous address read



## • Select (random) read



- Notes :
- When the device is connected to I<sup>2</sup>C external pins (SCL0 and SDA0), the device with the same addresses (1010000<sub>B</sub> to 1010111<sub>B</sub>) as built-in FRAM cannot be used.
  - When FRAM is used without connecting the device built into the pull-up resistor to I<sup>2</sup>C external pins, external pull-up resistor (1.1 kΩ or more) should be connected to SCL0 and SDA0 pins.
  - P50 and P51 cannot be used in MB95D108BS and MB95D108BW.

# MB95100B Series

## ■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Disabled)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	PLLC	PLL control register	R/W	00000000 <sub>B</sub>
0007 <sub>H</sub>	SYCC	System clock control register	R/W	1010X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	00000000 <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R/W	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00000000 <sub>B</sub>
000D <sub>H</sub>	—	(Disabled)	—	—
000E <sub>H</sub>	PDR2	Port 2 data register	R/W	00000000 <sub>B</sub>
000F <sub>H</sub>	DDR2	Port 2 direction register	R/W	00000000 <sub>B</sub>
0010 <sub>H</sub>	PDR3	Port 3 data register	R/W	00000000 <sub>B</sub>
0011 <sub>H</sub>	DDR3	Port 3 direction register	R/W	00000000 <sub>B</sub>
0012 <sub>H</sub>	PDR4	Port 4 data register	R/W	00000000 <sub>B</sub>
0013 <sub>H</sub>	DDR4	Port 4 direction register	R/W	00000000 <sub>B</sub>
0014 <sub>H</sub>	PDR5	Port 5 data register	R/W	00000000 <sub>B</sub>
0015 <sub>H</sub>	DDR5	Port 5 direction register	R/W	00000000 <sub>B</sub>
0016 <sub>H</sub>	PDR6	Port 6 data register	R/W	00000000 <sub>B</sub>
0017 <sub>H</sub>	DDR6	Port 6 direction register	R/W	00000000 <sub>B</sub>
0018 <sub>H</sub>	PDR7	Port 7 data register	R/W	00000000 <sub>B</sub>
0019 <sub>H</sub>	DDR7	Port 7 direction register	R/W	00000000 <sub>B</sub>
001A <sub>H</sub>	PDR8	Port 8 data register	R/W	00000000 <sub>B</sub>
001B <sub>H</sub>	DDR8	Port 8 direction register	R/W	00000000 <sub>B</sub>
001C <sub>H</sub> to 0025 <sub>H</sub>	—	(Disabled)	—	—
0026 <sub>H</sub>	PDRE	Port E data register	R/W	00000000 <sub>B</sub>
0027 <sub>H</sub>	DDRE	Port E direction register	R/W	00000000 <sub>B</sub>
0028 <sub>H</sub> , 0029 <sub>H</sub>	—	(Disabled)	—	—
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>

(Continued)

# MB95100B Series

Address	Register abbreviation	Register name	R/W	Initial value
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	—	(Disabled)	—	—
002D <sub>H</sub>	PUL1	Port 1 pull - up register	R/W	00000000 <sub>B</sub>
002E <sub>H</sub>	PUL2	Port 2 pull - up register	R/W	00000000 <sub>B</sub>
002F <sub>H</sub>	PUL3	Port 3 pull - up register	R/W	00000000 <sub>B</sub>
0030 <sub>H</sub>	PUL4	Port 4 pull - up register	R/W	00000000 <sub>B</sub>
0031 <sub>H</sub>	PUL5	Port 5 pull - up register	R/W	00000000 <sub>B</sub>
0032 <sub>H</sub>	PUL7	Port 7 pull - up register	R/W	00000000 <sub>B</sub>
0033 <sub>H</sub>	—	(Disabled)	—	—
0034 <sub>H</sub>	PULE	Port E pull - up register	R/W	00000000 <sub>B</sub>
0035 <sub>H</sub>	PULG	Port G pull - up register	R/W	00000000 <sub>B</sub>
0036 <sub>H</sub>	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000 <sub>B</sub>
0039 <sub>H</sub>	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000 <sub>B</sub>
003A <sub>H</sub>	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000 <sub>B</sub>
003B <sub>H</sub>	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000 <sub>B</sub>
003C <sub>H</sub>	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000 <sub>B</sub>
003D <sub>H</sub>	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000 <sub>B</sub>
003E <sub>H</sub>	TMCSRH0	16-bit reload timer control status register (Upper byte) ch.0	R/W	00000000 <sub>B</sub>
003F <sub>H</sub>	TMCSRL0	16-bit reload timer control status register (Lower byte) ch.0	R/W	00000000 <sub>B</sub>
0040 <sub>H</sub> , 0041 <sub>H</sub>	—	(Disabled)	—	—
0042 <sub>H</sub>	PCNTH0	16-bit PPG control status register (Upper byte) ch.0	R/W	00000000 <sub>B</sub>
0043 <sub>H</sub>	PCNTL0	16-bit PPG control status register (Lower byte) ch.0	R/W	00000000 <sub>B</sub>
0044 <sub>H</sub>	PCNTH1	16-bit PPG control status register (Upper byte) ch.1	R/W	00000000 <sub>B</sub>
0045 <sub>H</sub>	PCNTL1	16-bit PPG control status register (Lower byte) ch.1	R/W	00000000 <sub>B</sub>
0046 <sub>H</sub> , 0047 <sub>H</sub>	—	(Disabled)	—	—
0048 <sub>H</sub>	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000 <sub>B</sub>
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000 <sub>B</sub>
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000 <sub>B</sub>
004C <sub>H</sub>	EIC01	External interrupt circuit control register ch.8/ch.9	R/W	00000000 <sub>B</sub>
004D <sub>H</sub>	EIC11	External interrupt circuit control register ch.10/ch.11	R/W	00000000 <sub>B</sub>

(Continued)

# MB95100B Series

Address	Register abbreviation	Register name	R/W	Initial value
004E <sub>H</sub> , 004F <sub>H</sub>	—	(Disabled)	—	—
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000 <sub>B</sub>
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000 <sub>B</sub>
0058 <sub>H</sub>	SSR0	UART/SIO serial status register ch.0	R/W	00000001 <sub>B</sub>
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register ch.0	R/W	00000000 <sub>B</sub>
005A <sub>H</sub>	RDR0	UART/SIO serial input data register ch.0	R	00000000 <sub>B</sub>
005B <sub>H</sub> to 005F <sub>H</sub>	—	(Disabled)	—	—
0060 <sub>H</sub>	IBCR00	I <sup>2</sup> C bus control register 0 ch.0	R/W	00000000 <sub>B</sub>
0061 <sub>H</sub>	IBCR10	I <sup>2</sup> C bus control register 1 ch.0	R/W	00000000 <sub>B</sub>
0062 <sub>H</sub>	IBSR0	I <sup>2</sup> C bus status register ch.0	R	00000000 <sub>B</sub>
0063 <sub>H</sub>	IDDR0	I <sup>2</sup> C data register ch.0	R/W	00000000 <sub>B</sub>
0064 <sub>H</sub>	IAAR0	I <sup>2</sup> C address register ch.0	R/W	00000000 <sub>B</sub>
0065 <sub>H</sub>	ICCR0	I <sup>2</sup> C clock control register ch.0	R/W	00000000 <sub>B</sub>
0066 <sub>H</sub> to 006B <sub>H</sub>	—	(Disabled)	—	—
006C <sub>H</sub>	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	8/10-bit A/D converter data register (Upper byte)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	8/10-bit A/D converter data register (Lower byte)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub>	WCSR	Watch counter status register	R/W	00000000 <sub>B</sub>
0071 <sub>H</sub>	—	(Disabled)	—	—
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	000X0000 <sub>B</sub>
0073 <sub>H</sub>	SWRE0	Flash memory sector writing control register 0	R/W	00000000 <sub>B</sub>
0074 <sub>H</sub>	SWRE1	Flash memory sector writing control register 1	R/W	00000000 <sub>B</sub>
0075 <sub>H</sub>	—	(Disabled)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>

(Continued)

# MB95100B Series

Address	Register abbreviation	Register name	R/W	Initial value
0078 <sub>H</sub>	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Disabled)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (Upper byte) ch.0	R/W	00000000 <sub>B</sub>
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (Lower byte) ch.0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch.0	R/W	00000000 <sub>B</sub>
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (Upper byte) ch.1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (Lower byte) ch.1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch.1	R/W	00000000 <sub>B</sub>
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (Upper byte) ch.2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (Lower byte) ch.2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch.2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Disabled)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000 <sub>B</sub>
0F98 <sub>H</sub>	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000 <sub>B</sub>
0F99 <sub>H</sub>	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000 <sub>B</sub>
0F9A <sub>H</sub>	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000 <sub>B</sub>
0F9B <sub>H</sub>	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000 <sub>B</sub>
0F9C <sub>H</sub>	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9D <sub>H</sub>	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9E <sub>H</sub>	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111 <sub>B</sub>
0F9F <sub>H</sub>	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111 <sub>B</sub>

(Continued)

# MB95100B Series

Address	Register abbreviation	Register name	R/W	Initial value
0FA0 <sub>H</sub>	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA1 <sub>H</sub>	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA2 <sub>H</sub>	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA3 <sub>H</sub>	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111 <sub>B</sub>
0FA4 <sub>H</sub>	PPGS	8/16-bit PPG start register	R/W	00000000 <sub>B</sub>
0FA5 <sub>H</sub>	REVC	8/16-bit PPG output inversion register	R/W	00000000 <sub>B</sub>
0FA6 <sub>H</sub>	TMRH0/ TMRLRH0	16-bit timer register (Upper byte) ch.0/ 16-bit reload register (Upper byte) ch.0	R/W	00000000 <sub>B</sub>
0FA7 <sub>H</sub>	TMRL0/ TMRLRL0	16-bit timer register (Lower byte) ch.0/ 16-bit reload register (Lower byte) ch.0	R/W	00000000 <sub>B</sub>
0FA8 <sub>H</sub> , 0FA9 <sub>H</sub>	—	(Disabled)	—	—
0FAA <sub>H</sub>	PDCRH0	16-bit PPG down counter register (Upper byte) ch.0	R	00000000 <sub>B</sub>
0FAB <sub>H</sub>	PDCRL0	16-bit PPG down counter register (Lower byte) ch.0	R	00000000 <sub>B</sub>
0FAC <sub>H</sub>	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch.0	R/W	11111111 <sub>B</sub>
0FAD <sub>H</sub>	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch.0	R/W	11111111 <sub>B</sub>
0FAE <sub>H</sub>	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch.0	R/W	11111111 <sub>B</sub>
0FAF <sub>H</sub>	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch.0	R/W	11111111 <sub>B</sub>
0FB0 <sub>H</sub>	PDCRH1	16-bit PPG down counter register (Upper byte) ch.1	R	00000000 <sub>B</sub>
0FB1 <sub>H</sub>	PDCRL1	16-bit PPG down counter register (Lower byte) ch.1	R	00000000 <sub>B</sub>
0FB2 <sub>H</sub>	PCSRH1	16-bit PPG cycle setting buffer register (Upper byte) ch.1	R/W	11111111 <sub>B</sub>
0FB3 <sub>H</sub>	PCSRL1	16-bit PPG cycle setting buffer register (Lower byte) ch.1	R/W	11111111 <sub>B</sub>
0FB4 <sub>H</sub>	PDUTH1	16-bit PPG duty setting buffer register (Upper byte) ch.1	R/W	11111111 <sub>B</sub>
0FB5 <sub>H</sub>	PDUTL1	16-bit PPG duty setting buffer register (Lower byte) ch.1	R/W	11111111 <sub>B</sub>
0FB6 <sub>H</sub> to 0FBB <sub>H</sub>	—	(Disabled)	—	—
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch.0	R/W	00000000 <sub>B</sub>
0FBF <sub>H</sub>	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000 <sub>B</sub>
0FC0 <sub>H</sub> , 0FC1 <sub>H</sub>	—	(Disabled)	—	—
0FC2 <sub>H</sub>	AIDRH	A/D input disable register (Upper byte)	R/W	00000000 <sub>B</sub>
0FC3 <sub>H</sub>	AIDRL	A/D input disable register (Lower byte)	R/W	00000000 <sub>B</sub>

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FC4 <sub>H</sub> to 0FE2 <sub>H</sub>	—	(Disabled)	—	—
0FE3 <sub>H</sub>	WCDR	Watch counter data register	R/W	00111111 <sub>B</sub>
0FE4 <sub>H</sub> to 0FED <sub>H</sub>	—	(Disabled)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub>	WICR	Interrupt pin control register	R/W	01000000 <sub>B</sub>
0FF0 <sub>H</sub> to 0FFF <sub>H</sub>	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable/Writable  
 R : Read only  
 W : Write only

- Initial value symbols

0 : The initial value of this bit is "0".  
 1 : The initial value of this bit is "1".  
 X : The initial value of this bit is undefined.

Note : Do not write to the "(Disabled)". Reading the "(Disabled)" returns an undefined value.

# MB95100B Series

## ■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1 : 0]	<div style="text-align: center;">High</div> <div style="text-align: center;">Low</div>
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1 : 0]	
16-bit reload timer ch.0	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1 : 0]	
I <sup>2</sup> C ch.0	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1 : 0]	
16-bit PPG ch.1	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1 : 0]	
Watch timer/Watch counter	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1 : 0]	
External interrupt ch.8	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1 : 0]	
External interrupt ch.9					
External interrupt ch.10					
External interrupt ch.11					
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1 : 0]	
Flash memory	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1 : 0]	



## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V <sub>CC</sub> AV <sub>CC</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	*2
	AVR	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0		*2
Input voltage*1	V <sub>I1</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	Other than P80 to P83*3
	V <sub>I2</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0		P80 to P83
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	*3
Maximum clamp current	I <sub>CLAMP</sub>	- 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	Σ I <sub>CLAMP</sub>	—	20	mA	Applicable to pins*4
“L” level maximum output current	I <sub>OL1</sub>	—	15	mA	Other than P00 to P07
	I <sub>OL2</sub>		15		P00 to P07
“L” level average current	I <sub>OLAV1</sub>	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OLAV2</sub>		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current	ΣI <sub>OLAV</sub>	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
“H” level maximum output current	I <sub>OH1</sub>	—	- 15	mA	Other than P00 to P07
	I <sub>OH2</sub>		- 15		P00 to P07
“H” level average current	I <sub>OHAV1</sub>	—	- 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OHAV2</sub>		- 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI <sub>OH</sub>	—	- 100	mA	
“H” level total average output current	ΣI <sub>OHAV</sub>	—	- 50	mA	Total average output current = operating current × operating ratio (Total of pins)

(Continued)

# MB95100B Series

(Continued)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power consumption	Pd	—	320	mW	
Operating temperature	T <sub>A</sub>	- 40	+ 85	°C	
Storage temperature	T <sub>STG</sub>	- 55	+ 150	°C	MB95107B, MB95F108BS, MB95F108BW
		- 40	+ 125		MB95D108BS, MB95D108BW

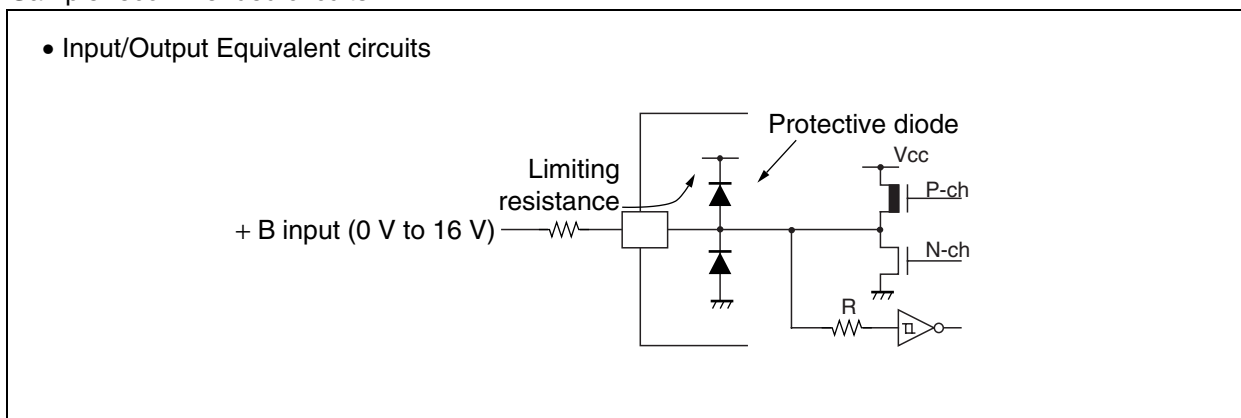
\*1 : The parameter is based on  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ .

\*2 : Apply equal potential to  $AV_{CC}$  and  $V_{CC}$ .  $AVR$  should not exceed  $AV_{CC} + 0.3 \text{ V}$ .

\*3 :  $V_{I1}$  and  $V_o$  should not exceed  $V_{CC} + 0.3 \text{ V}$ .  $V_{I1}$  must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_{I1}$  rating.

\*4 : Applicable to pins : P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71, PE0 to PE3, PG0

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal is an input signal that exceeds  $V_{CC}$  voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Sample recommended circuits :



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB95100B Series

## 2. Recommended Operating Conditions

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply voltage	$V_{CC}, AV_{CC}$	—	1.8*	3.3	V	At normal operating, Flash memory product, $T_A = -10\text{ °C}$ to $+85\text{ °C}$
			1.8*	3.6		At normal operating, MASK ROM product, $T_A = -10\text{ °C}$ to $+85\text{ °C}$
			2.0*	3.3		At normal operating, Flash memory product, $T_A = -40\text{ °C}$ to $+85\text{ °C}$
			2.0*	3.6		At normal operating, MASK ROM product, $T_A = -40\text{ °C}$ to $+85\text{ °C}$
			2.7	3.3		At normal operating, Flash memory product, At FRAM access, $T_A = -40\text{ °C}$ to $+85\text{ °C}$
			2.7	3.6		At normal operating, MASK ROM product, At FRAM access, $T_A = -40\text{ °C}$ to $+85\text{ °C}$
			2.6	3.6		MB95FV100D-101 $T_A = +5\text{ °C}$ to $+35\text{ °C}$
			1.5	3.3		Retain status in stop mode, Flash memory product
			1.5	3.6		Retain status in stop mode, MASK ROM product
			A/D converter reference input voltage	AVR		
Operating temperature	$T_A$		- 40	+ 85	°C	

\* : The values vary with the operating frequency.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB95100B Series

## 3. DC Characteristics

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH1}$	P10, P67	*1	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	At selecting CMOS input level
	$V_{IH2}$	P50, P51	—	$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	At selecting CMOS input level MB95F108BS, MB95F108BW, MB95107B, MB95FV100D-101
					—	$V_{CC} + 0.3$		At selecting CMOS input level MB95D108BS, MB95D108BW
	$V_{IHS1}$	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P60 to P67, P70, P71, PE0 to PE3, PG0, PG1*2, PG2*2	*1	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	$V_{IHS2}$	P80 to P83	*1	$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	Hysteresis input
	$V_{IHS3}$	P50, P51	—	$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	Hysteresis input MB95F108BS, MB95F108BW, MB95107B, MB95FV100D-101
					—	$V_{SS} + 5.0$		Hysteresis input MB95D108BS, MB95D108BW
	$V_{IHM}$	$\overline{\text{RST}}$ , MOD	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input (Flash memory product)
			—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input (MASK ROM product)

(Continued)

# MB95100B Series

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level input voltage	$V_{IL}$	P10, P50, P51, P67	*1	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	At selecting CMOS input level (Hysteresis input)
	$V_{ILS}$	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P80 to P83, PE0 to PE3, PG0, PG1*2, PG2*2	*1	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	$V_{ILM}$	$\overline{RST}$ , MOD	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS input (Flash memory product)
			—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input (MASK ROM product)
Input leakage current (Hi-Z output leakage current)	$I_{LI}$	Port other than P50, P51, P80 to P83	$0.0\text{ V} < V_I < V_{CC}$	-5	—	+5	$\mu\text{A}$	When the pull-up is prohibition setting
“H” level output voltage	$V_{OH1}$	Output pin other than P00 to P07	$I_{OH} = -4.0\text{ mA}$	2.4	—	—	V	
	$V_{OH2}$	P00 to P07	$I_{OH} = -8.0\text{ mA}$	2.4	—	—	V	
“L” level output voltage	$V_{OL1}$	Output pin other than P00 to P07	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P00 to P07	$I_{OL} = 12\text{ mA}$	—	—	0.4	V	
Open-drain output application voltage	$V_{D1}$	P80 to P83	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	$V_{D2}$	P50, P51	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$		MB95F108BS, MB95F108BW, MB95107B
						$V_{CC} + 0.3$		MB95D108BS, MB95D108BW
Open-drain output leakage current	$I_{LIOD}$	P50, P51, P80 to P83	$0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$	—	—	5	$\mu\text{A}$	

(Continued)

# MB95100B Series

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistor	$R_{PULL}$	P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71, PE0 to PE3, PG0, PG1*2, PG2*2	$V_I = 0.0\text{ V}$	25	50	100	k $\Omega$	When the pull-up is permission setting
Pull-down resistor	$R_{MOD}$	MOD	$V_I = V_{CC}$	25	50	100	k $\Omega$	MASK ROM product
Input capacitance	$C_{IN}$	Other than $AV_{CC}$ , $AV_{SS}$ , AVR, $V_{CC}$ , $V_{SS}$	$f = 1\text{ MHz}$	—	5	15	pF	
Power supply current*3	$I_{CC}$	$V_{CC}$ (External clock operation)	$F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main clock mode (divided by 2)	—	11.0	14.0	mA	MB95F108BS, MB95F108BW (at other than Flash memory writing and erasing)
				—	30.0	35.0	mA	MB95F108BS, MB95F108BW (at Flash memory writing and erasing)
				—	7.3	10.0	mA	MB95107B
			$F_{CH} = 32\text{ MHz}$ $F_{MP} = 16\text{ MHz}$ Main clock mode (divided by 2)	—	17.6	22.4	mA	MB95F108BS, MB95F108BW (at other than Flash memory writing and erasing)
				—	38.1	44.9	mA	MB95F108BS, MB95F108BW (at Flash memory writing and erasing)
				—	11.7	16.0	mA	MB95107B
			$F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main clock mode (divided by 2) When FRAM read and write ( $f_{SCL} = 400\text{ kHz}$ )	—	11.1	15.0	mA	MB95D108BS, MB95D108BW (at other than Flash memory writing and erasing)
				—	30	35	mA	MB95D108BS, MB95D108BW (at Flash memory write and erase)

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# MB95100B Series

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I <sub>CC</sub>	V <sub>CC</sub> (External clock operation)	F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main clock mode (divided by 2) When FRAM read and write (f <sub>SCL</sub> = 400 kHz)	—	17.7	22.5	mA	MB95D108BS, MB95D108BW (at other than Flash memory writing and erasing)
			—	38.1	44.9	mA	MB95D108BS, MB95D108BW (at Flash memory write and erase)	
	I <sub>CCS</sub>		F <sub>CH</sub> = 20 MHz F <sub>MP</sub> = 10 MHz Main Sleep mode (divided by 2)	—	4.5	6.0	mA	
			F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main Sleep mode (divided by 2)	—	7.2	9.6	mA	
	I <sub>CCCL</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Sub clock mode (divided by 2), T <sub>A</sub> = +25 °C	—	25	35	μA	
	I <sub>CCLS</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Sub sleep mode (divided by 2), T <sub>A</sub> = +25 °C	—	7	15	μA	
	I <sub>CCCT</sub>		F <sub>CL</sub> = 32 kHz Watch mode	—	2	10	μA	Flash memory product
			Main stop mode T <sub>A</sub> = +25 °C	—	1	5	μA	MASK ROM product
	I <sub>CCMPLL</sub>		F <sub>CH</sub> = 4 MHz F <sub>MP</sub> = 10 MHz Main PLL mode (multiplied by 2.5)	—	10	14	mA	Flash memory product
			—	—	6.7	10.0	mA	MASK ROM product
F <sub>CH</sub> = 6.4 MHz F <sub>MP</sub> = 16 MHz Main PLL mode (multiplied by 2.5)		—	16.0	22.4	mA	Flash memory product		
—		—	10.8	16.0	mA	MASK ROM product		

(Continued)

# MB95100B Series

(Continued)

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I <sub>CCSPLL</sub>	V <sub>CC</sub> (External clock operation)	F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 128 kHz Sub PLL mode (multiplied by 4), T <sub>A</sub> = +25 °C	—	190	250	μA	
	I <sub>CTS</sub>		F <sub>CH</sub> = 10 MHz Timebase timer mode T <sub>A</sub> = +25 °C	—	0.4	0.5	mA	
	I <sub>CCH</sub>		Sub stop mode T <sub>A</sub> = +25 °C	—	1	5	μA	
	I <sub>A</sub>	AV <sub>CC</sub>	F <sub>CH</sub> = 10 MHz At operating of A/D conversion	—	1.3	2.2	mA	
	I <sub>AH</sub>		F <sub>CH</sub> = 10 MHz At stopping of A/D conversion T <sub>A</sub> = +25 °C	—	1	5	μA	

\*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR).

\*2 : Single clock product only

\*3 : Power supply current is regulated by external clock.

- Refer to “4. AC Characteristics (1) Clock Timing” for F<sub>CH</sub> and F<sub>CL</sub>.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F<sub>MP</sub> and F<sub>MPL</sub>.



## 4. AC Characteristics

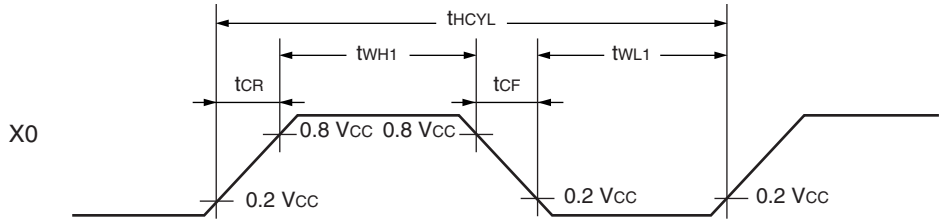
### (1) Clock Timing

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	$F_{CH}$	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	$F_{CL}$	X0A, X1A	—	—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL Flash memory product : $V_{CC} = 2.3\text{ V}$ to $3.3\text{ V}$ MASK ROM product : $V_{CC} = 2.3\text{ V}$ to $3.6\text{ V}$
Clock cycle time	$t_{HCYL}$	X0, X1	—	61.5	—	1000	ns	When using main oscillation circuit
				30.8	—	1000	ns	When using external clock
	$t_{LCYL}$	X0A, X1A		—	30.5	—	$\mu\text{s}$	When using sub oscillation circuit, When using external clock
Input clock pulse width	$t_{WH1}$ $t_{WL1}$	X0	—	61.5	—	—	ns	When using external clock, duty ratio is about 30% to 70%.
	$t_{WH2}$ $t_{WL2}$	X0A		—	15.2	—	$\mu\text{s}$	
Input clock rise time and fall time	$t_{CR}$ $t_{CF}$	X0, X0A	—	—	10	ns	When using external clock	

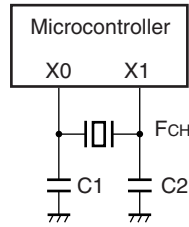
# MB95100B Series

- Input wave form for using external clock (main clock)

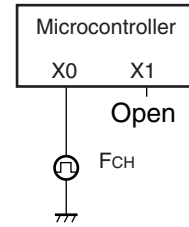


- Figure of main clock Input port external connection

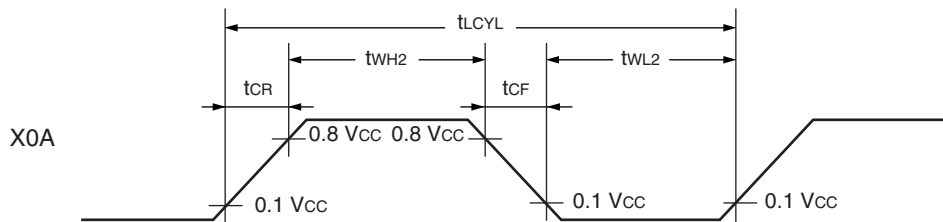
When using a crystal or ceramic oscillator



When using external clock

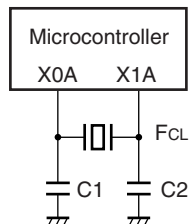


- Input wave form for using external clock (sub clock)

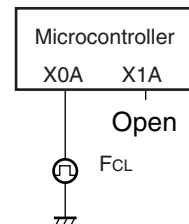


- Figure of sub clock input port external connection

When using a crystal or ceramic oscillator



When using external clock



## (2) Source Clock/Machine Clock

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Sym- bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before setting division)	t <sub>SCLK</sub>	—	61.5	—	2000	ns	When using main clock Min : F <sub>CH</sub> = 8.125 MHz, PLL multiplied by 2 Max : F <sub>CH</sub> = 1 MHz, divided by 2
			7.6	—	61.0	μs	When using sub clock Min : F <sub>CL</sub> = 32 kHz, PLL multiplied by 4 Max : F <sub>CL</sub> = 32 kHz, divided by 2
Source clock frequency	F <sub>SP</sub>	—	0.5	—	16.25	MHz	When using main clock
	F <sub>SPL</sub>	—	16.384	—	131.072	kHz	When using sub clock
Machine clock cycle time*2 (Minimum instruction execution time)	t <sub>MCLK</sub>	—	61.5	—	32000	ns	When using main clock Min : F <sub>SP</sub> = 16.25 MHz, no division Max : F <sub>SP</sub> = 0.5 MHz, divided by 16
			7.6	—	976.5	μs	When using sub clock Min : F <sub>SPL</sub> = 131 kHz, no division Max : F <sub>SPL</sub> = 16 kHz, divided by 16
Machine clock frequency	F <sub>MP</sub>	—	0.031	—	16.250	MHz	When using main clock
	F <sub>MPL</sub>	—	1.024	—	131.072	kHz	When using sub clock

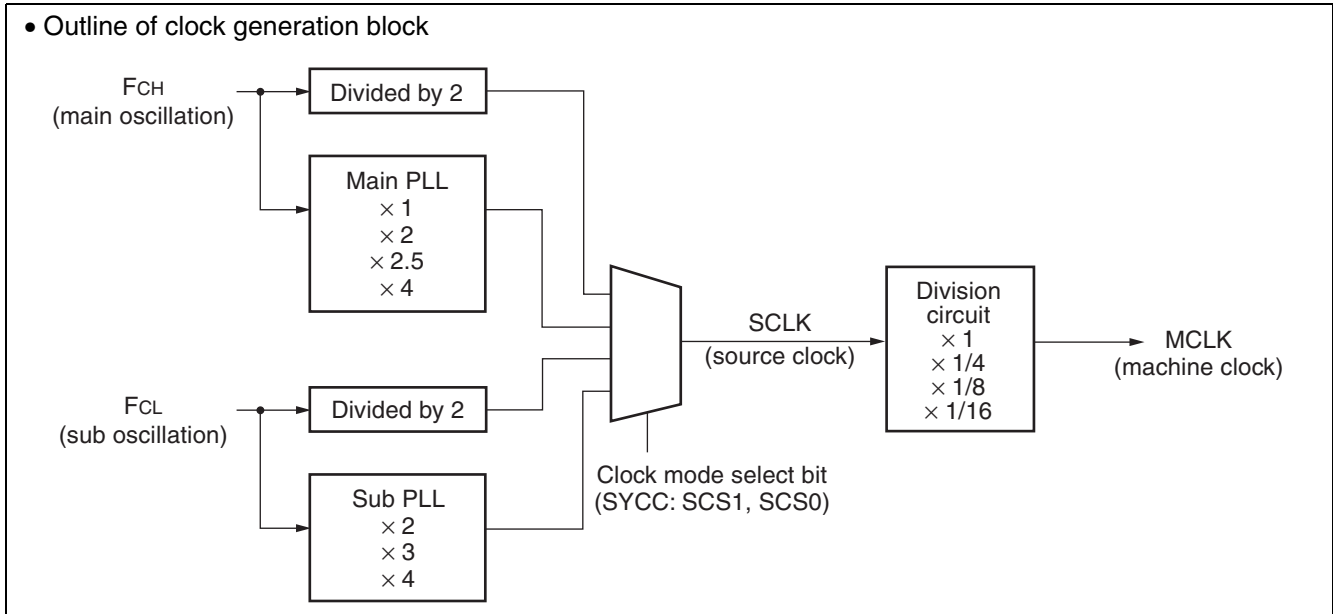
\*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follow.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

\*2 : Operation clock of the microcontroller. Machine clock can be selected as follow.

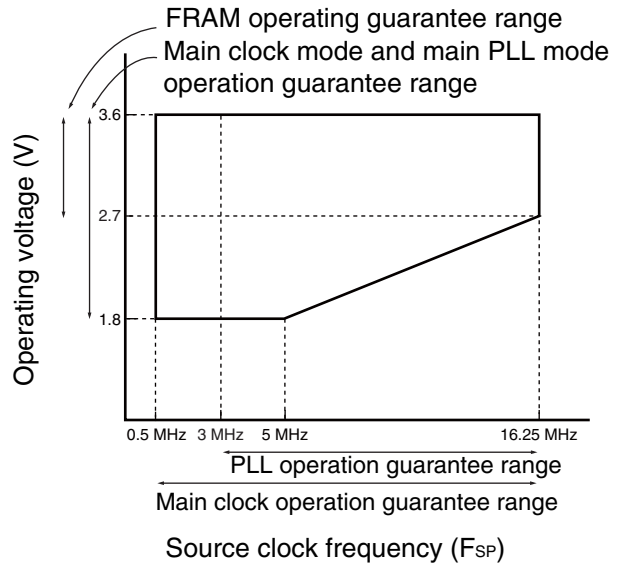
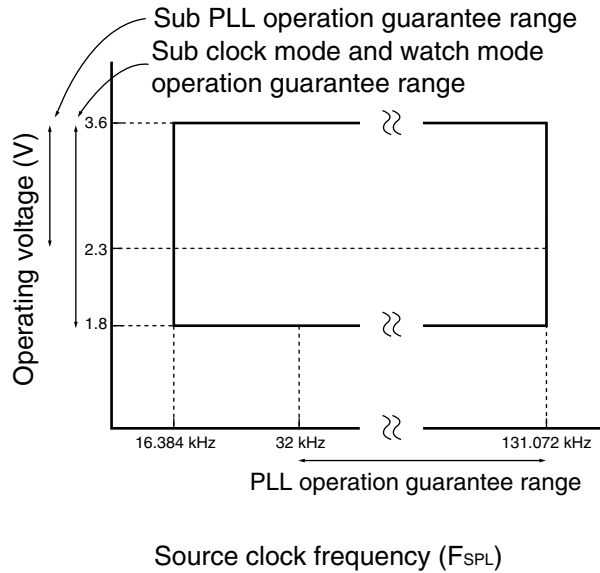
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

# MB95100B Series

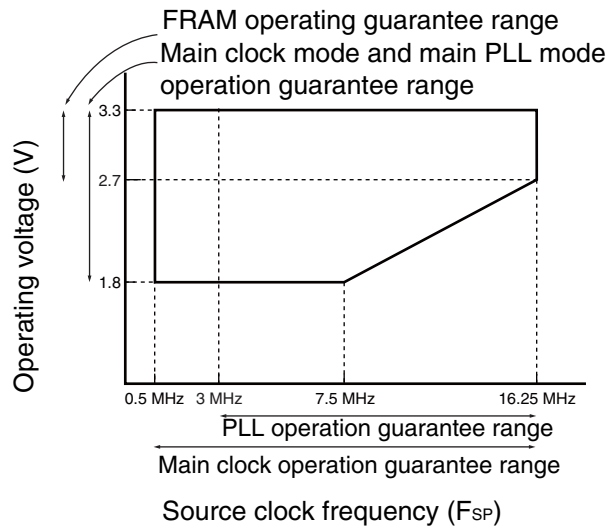
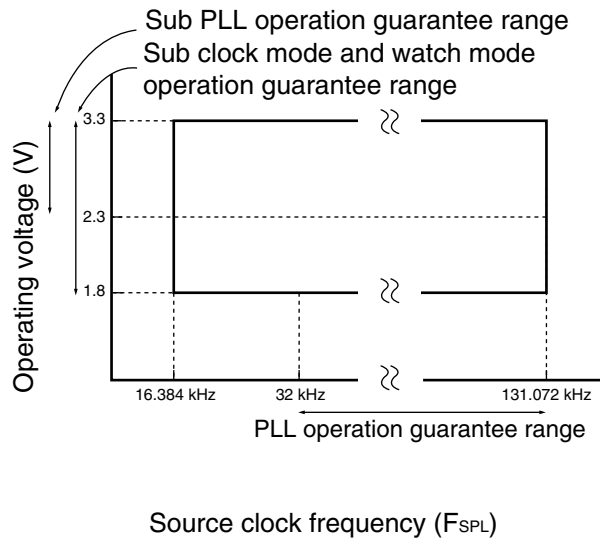


- Operating voltage - Operating frequency (When  $T_A = -10\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

- MB95107B



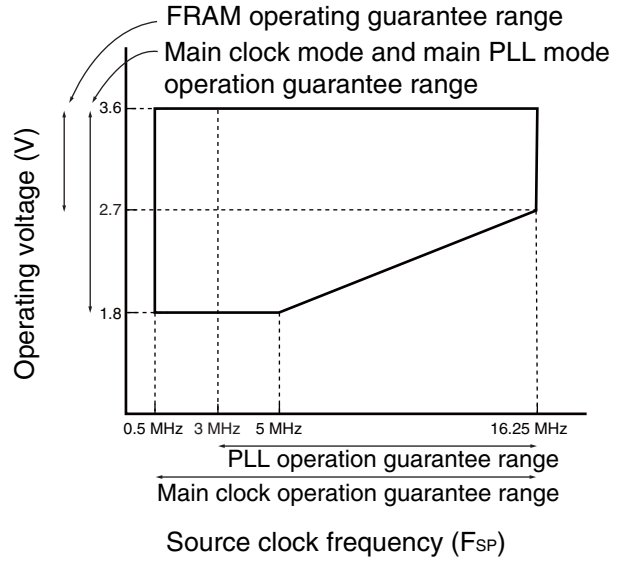
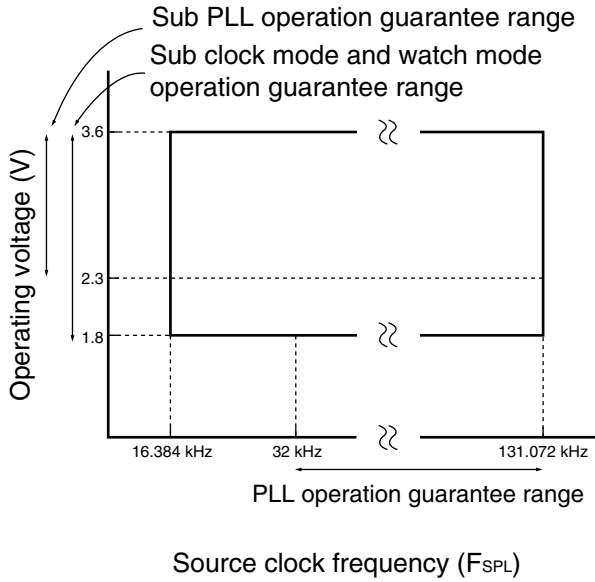
- MB95F108BS, MB95F108BW, MB95D108BS, MB95D108BW



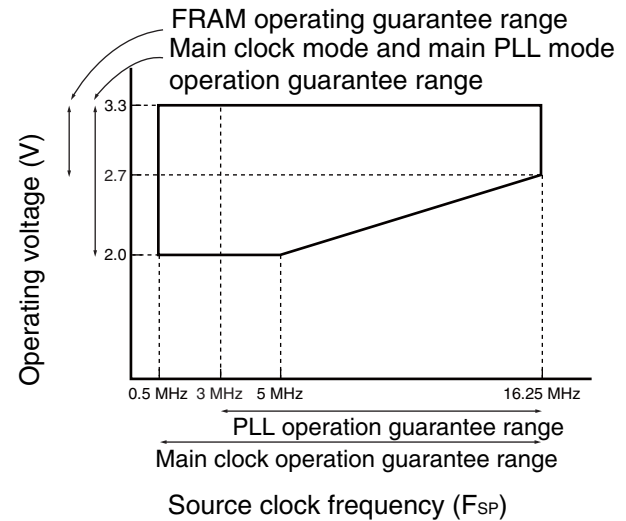
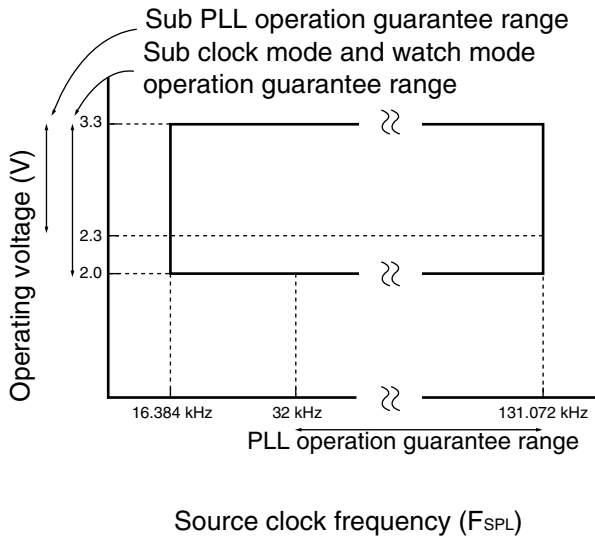
# MB95100B Series

- Operating voltage - Operating frequency (When  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

- MB95107B

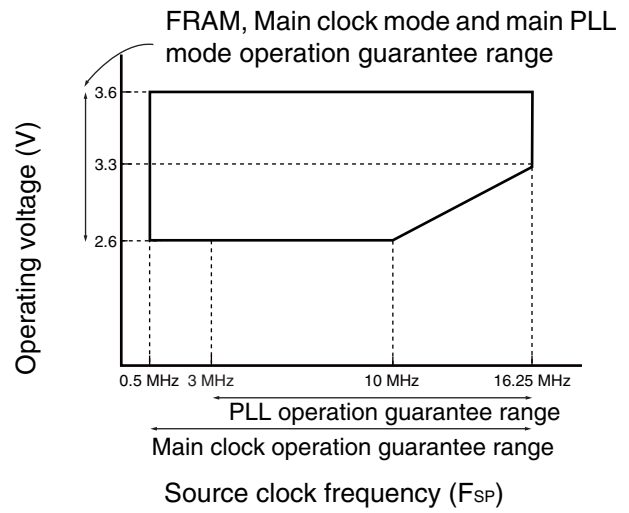
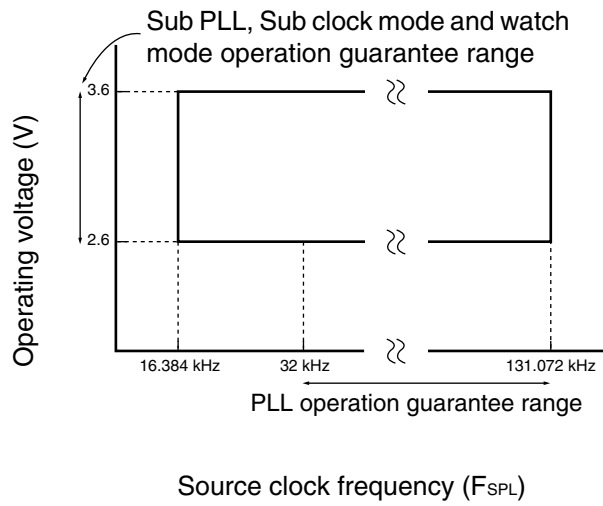


- MB95F108BS, MB95F108BW, MB95D108BS, MB95D108BW



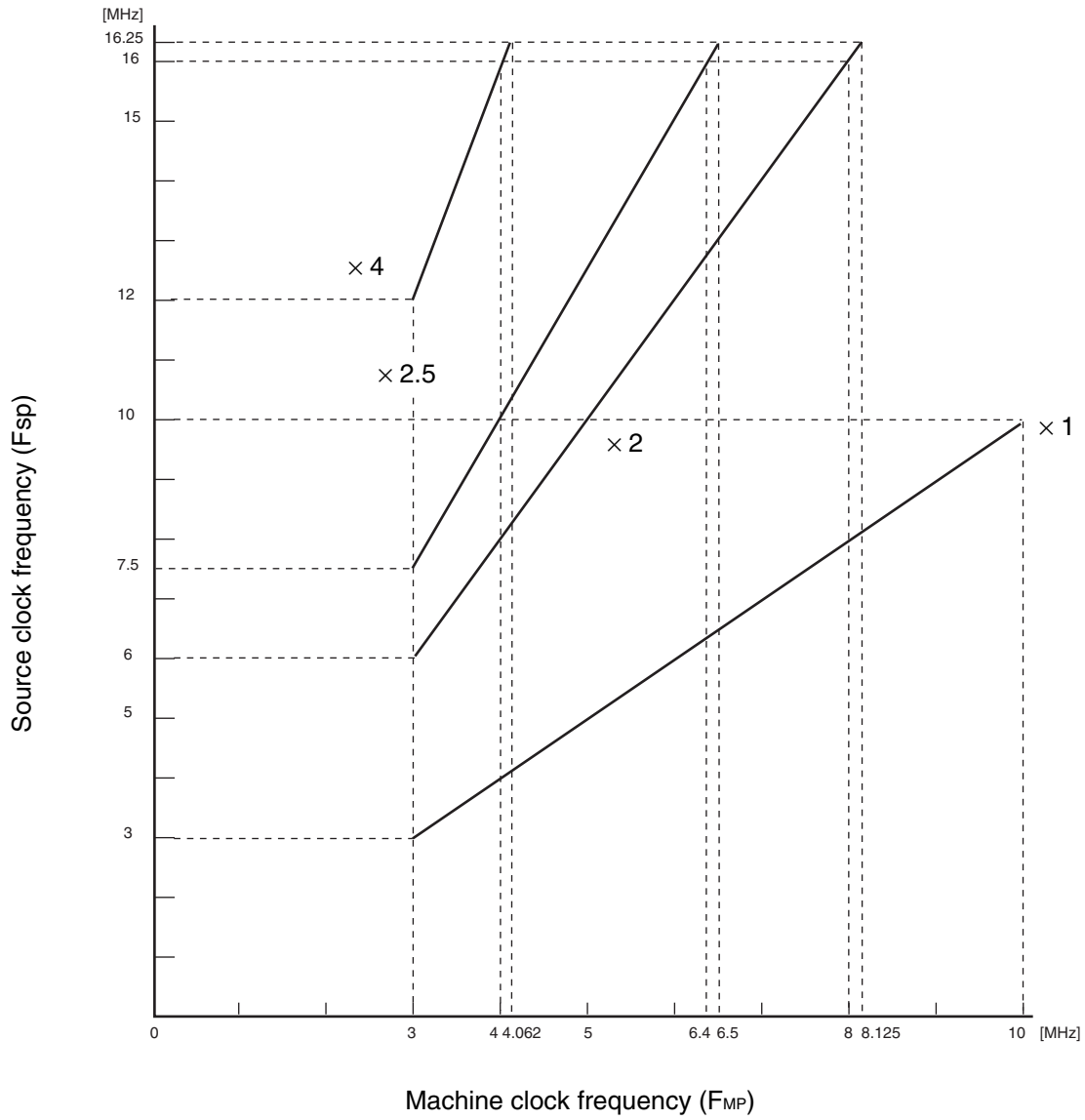
- Operating voltage - Operating frequency ( $T_A = +5\text{ }^\circ\text{C}$  to  $+35\text{ }^\circ\text{C}$ )

- MB95FV100D-101



# MB95100B Series

- Main PLL operation frequency





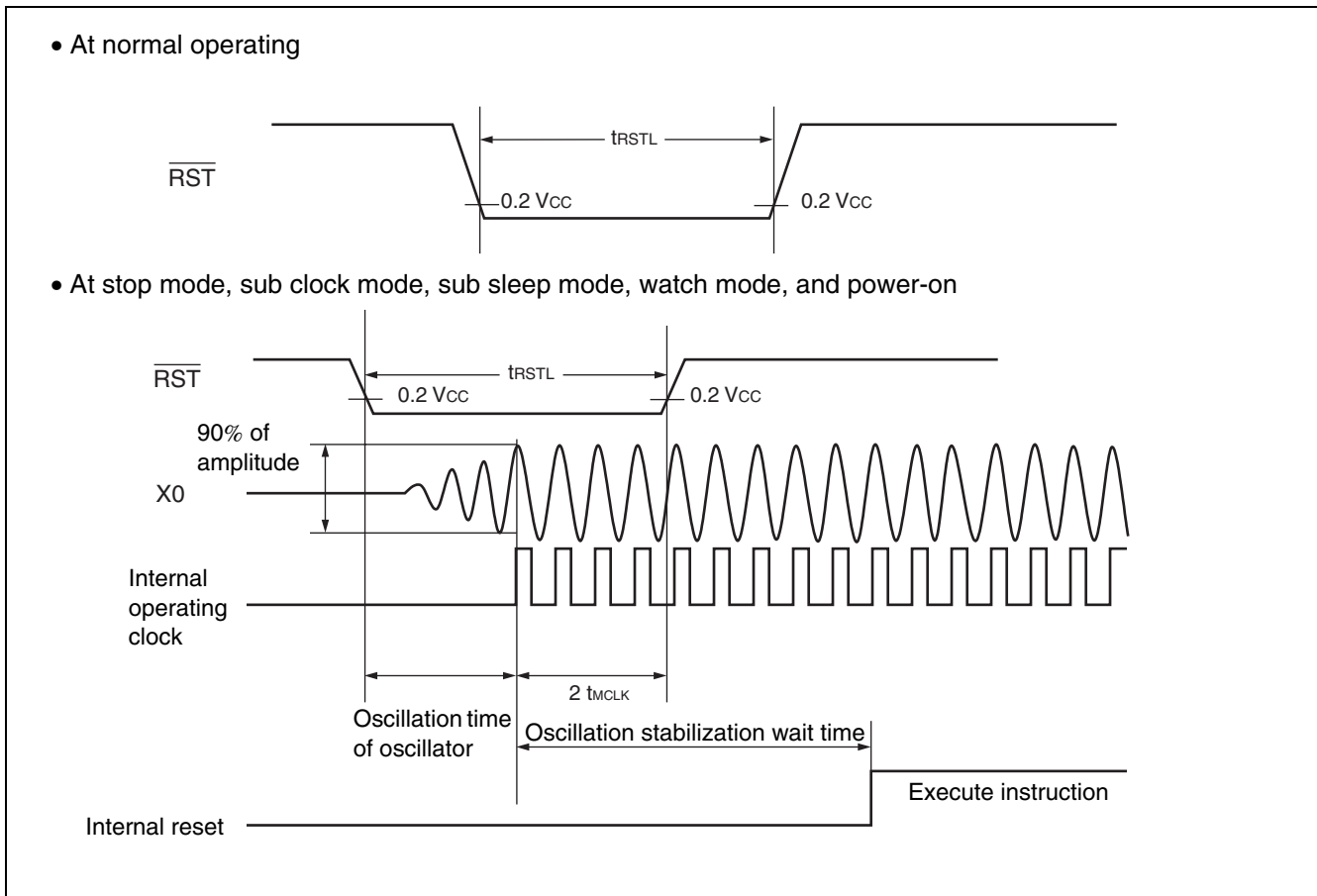
## (3) External Reset

( $V_{CC} = 3.3\text{ V}$ ,  $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{RST}}$ “L” level pulse width	$t_{\text{RSTL}}$	$\overline{\text{RST}}$	—	$2 t_{\text{MCLK}}^{*1}$	—	ns	At normal operating
				Oscillation time of oscillator <sup>*2</sup> $+ 2 t_{\text{MCLK}}^{*1}$	—	ns	At stop mode, sub clock mode, sub sleep mode, and watch mode

\*1 : Refer to “(2) Source Clock/Machine Clock” for  $t_{\text{MCLK}}$ .

\*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  and several ms. In the external clock, the oscillation time is 0 ms.



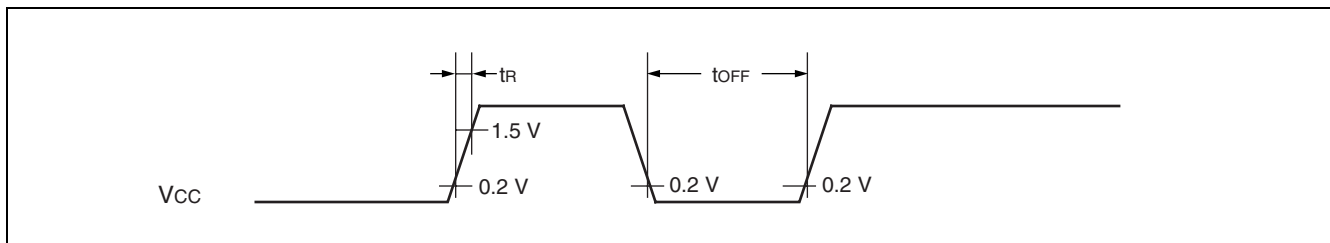
# MB95100B Series

## (4) Power-on Reset

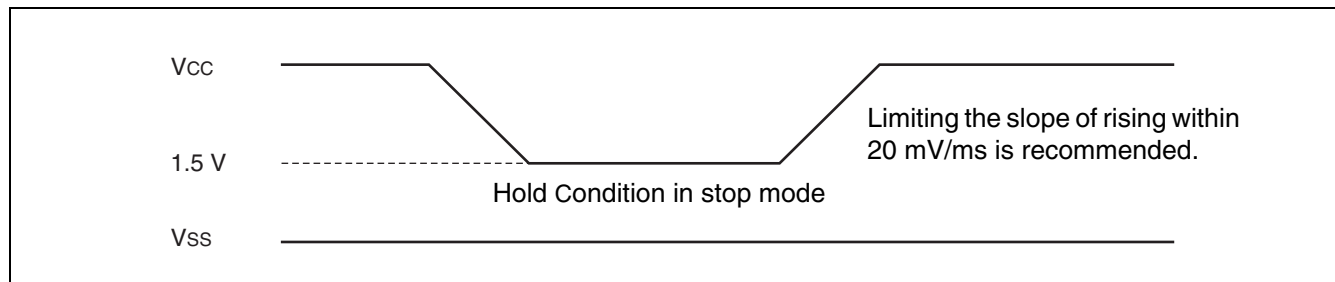
( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	$t_R$	$V_{CC}$	—	—	36	ms	Waiting time until power-on
Power supply cutoff time	$t_{OFF}$			1	—	ms	

Note : The power supply must be turned on within the selected oscillation stabilization time.



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below.

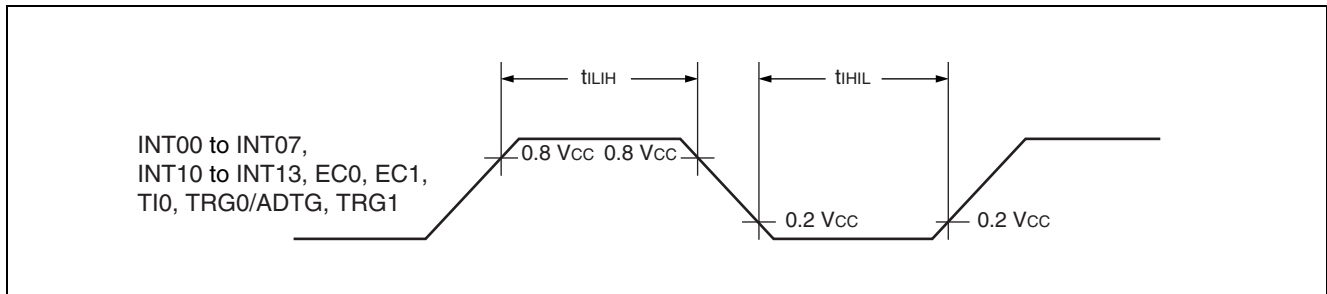


## (5) Peripheral Input Timing

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Peripheral input "H" pulse width	$t_{\text{LIH}}$	INT00 to INT07, INT10 to INT13,	—	$2 t_{\text{MCLK}}^*$	—	ns
Peripheral input "L" pulse width	$t_{\text{HIL}}$	EC0, EC1, TIO, TRG0/ADTG, TRG1		$2 t_{\text{MCLK}}^*$	—	ns

\* : Refer to "(2) Source Clock/Machine Clock" for  $t_{\text{MCLK}}$ .



# MB95100B Series

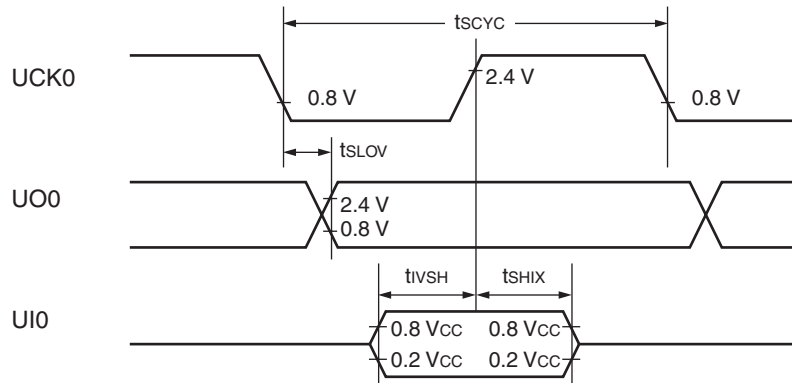
## (6) UART/SIO, Serial I/O Timing

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

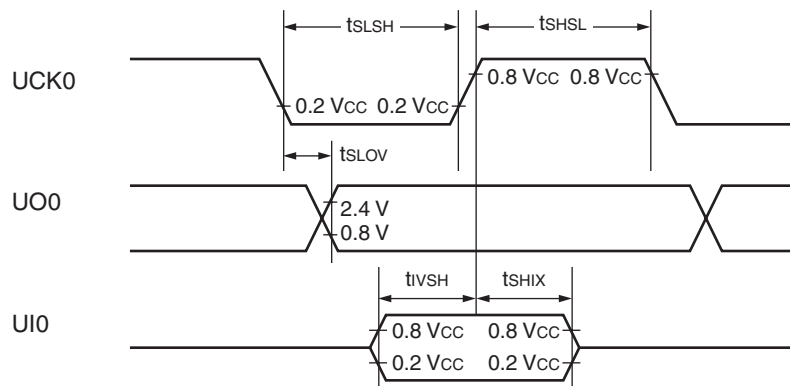
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	UCK0	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{TTL}$ .	$4 t_{MCLK}^*$	—	ns
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		- 190	+ 190	ns
Valid UI → UCK ↑	$t_{IVSH}$	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	UCK0	External clock operation output pin : $C_L = 80\text{ pF} + 1\text{TTL}$ .	$4 t_{MCLK}^*$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	UCK0		$4 t_{MCLK}^*$	—	ns
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		0	190	ns
Valid UI → UCK ↑	$t_{IVSH}$	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0	$2 t_{MCLK}^*$	—	ns	

\* : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

### • Internal shift clock mode



### • External shift clock mode



## (7) LIN-UART Timing

Sampling at the rising edge of sampling clock\*1 and prohibited serial clock delay\*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	5 t <sub>MCLK</sub> *3	—	ns
SCK ↑→ SOT delay time	t <sub>SLOVI</sub>	SCK, SOT		-95	+ 95	ns
Valid SIN→SCK↑	t <sub>IVSHI</sub>	SCK, SIN		t <sub>MCLK</sub> *3 + 190	—	ns
SCK↑→ valid SIN hold time	t <sub>SHIXI</sub>	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK	External clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	3 t <sub>MCLK</sub> *3 - t <sub>R</sub>	—	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK		t <sub>MCLK</sub> *3 + 95	—	ns
SCK ↓→SOT delay time	t <sub>SLOVE</sub>	SCK, SOT		—	2 t <sub>MCLK</sub> *3 + 95	ns
Valid SIN→SCK↑	t <sub>IVSHE</sub>	SCK, SIN		190	—	ns
SCK↑→ valid SIN hold time	t <sub>SHIXE</sub>	SCK, SIN		t <sub>MCLK</sub> *3 + 95	—	ns
SCK fall time	t <sub>F</sub>	SCK		—	10	ns
SCK rise time	t <sub>R</sub>	SCK		—	10	ns

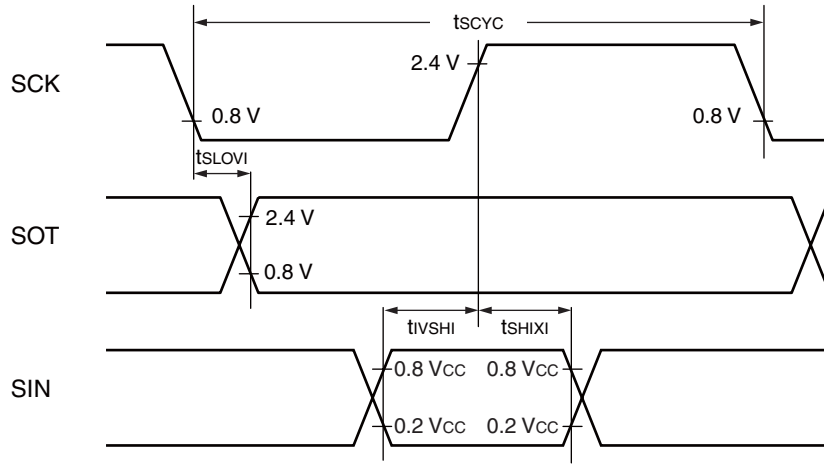
\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

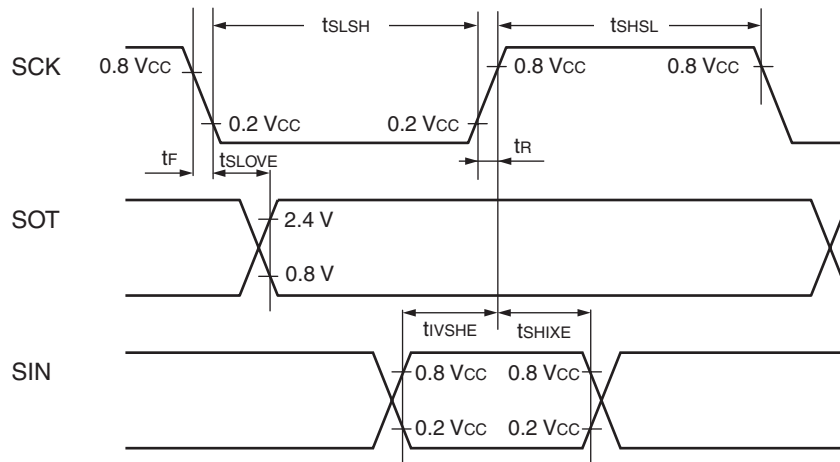
\*3 : Refer to "(2) Source Clock/Machine Clock" for t<sub>MCLK</sub>.

# MB95100B Series

- Internal shift clock mode



- External shift clock mode



# MB95100B Series

**Sampling at the falling edge of sampling clock\*1 and prohibited serial clock delay\*2**  
**(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)**

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5\ t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN→SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3\ t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVE}$	SCK, SOT		—	$2\ t_{MCLK}^{*3} + 95$	ns
Valid SIN→SCK $\downarrow$	$t_{IVSLE}$	SCK, SIN		190	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK	—	10	ns	

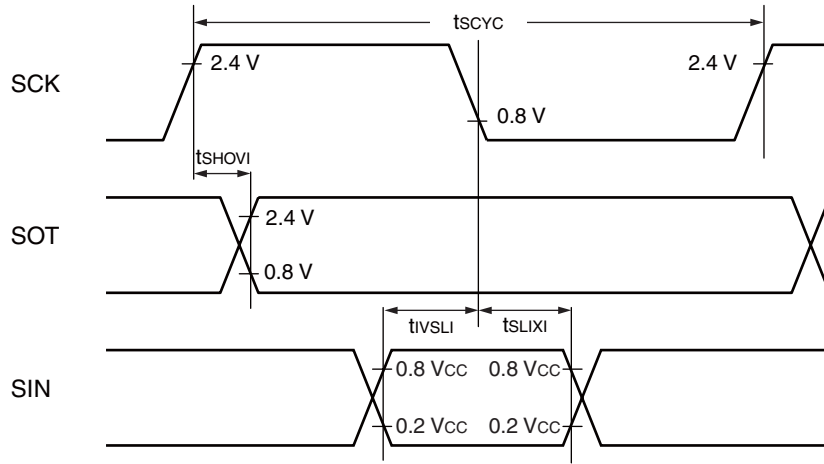
\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

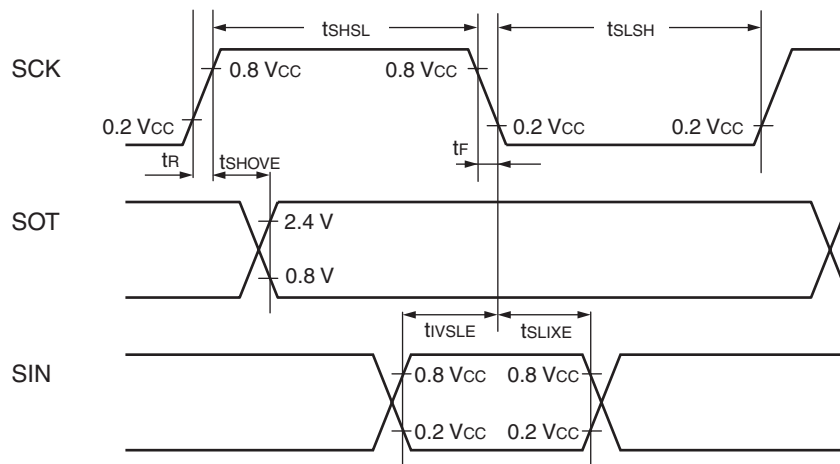
\*3 : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

# MB95100B Series

- Internal shift clock mode



- External shift clock mode





# MB95100B Series

Sampling at the rising edge of sampling clock\*<sup>1</sup> and enabled serial clock delay\*<sup>2</sup>  
 (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

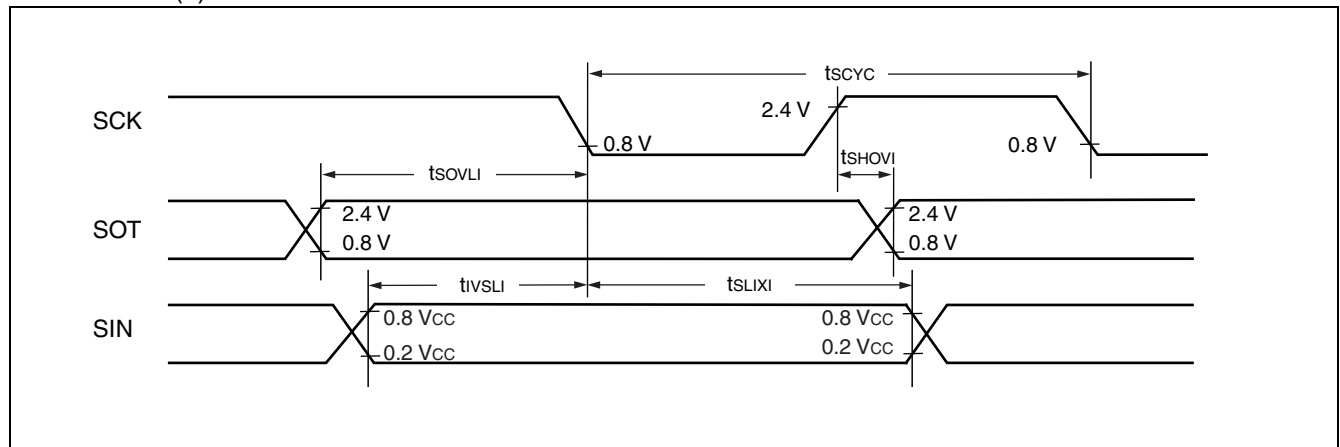
( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL.}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ → SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN→SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
SOT→SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “(2) Source Clock/Machine Clock” for  $t_{MCLK}$ .



# MB95100B Series

Sampling at the falling edge of sampling clock\*1 and enabled serial clock delay\*2  
 (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

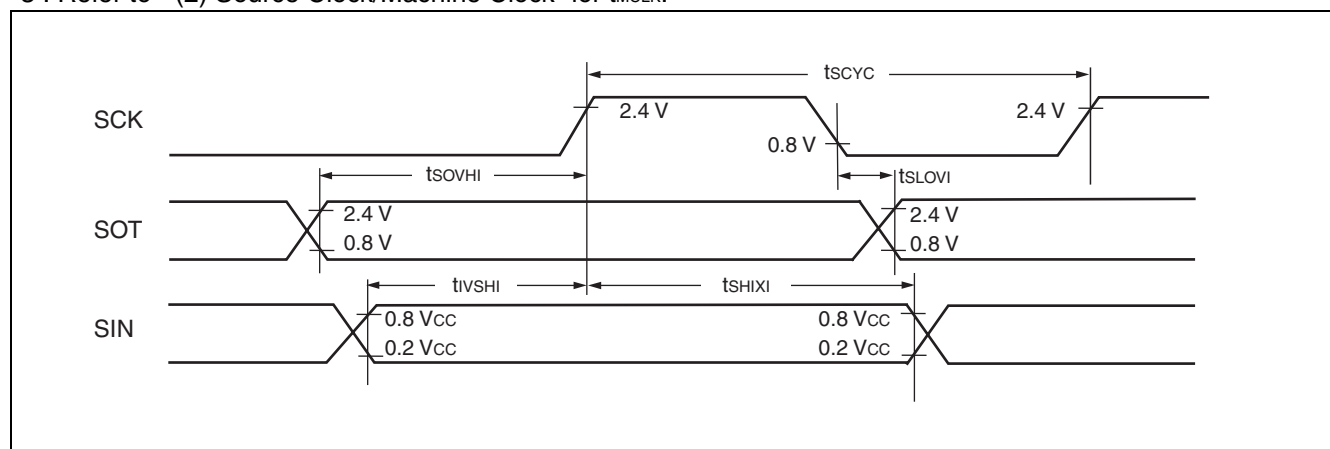
( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operating output pin : $C_L = 80\text{ pF} + 1\text{ TTL.}$	$5 t_{MCLK}^{*3}$	—	ns
SCK↓→SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN→SCK↑	$t_{VSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK↑ → valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
SOT→SCK↑ delay time	$t_{SOVHI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “(2) Source Clock/Machine Clock” for  $t_{MCLK}$ .



## (8) I<sup>2</sup>C Timing

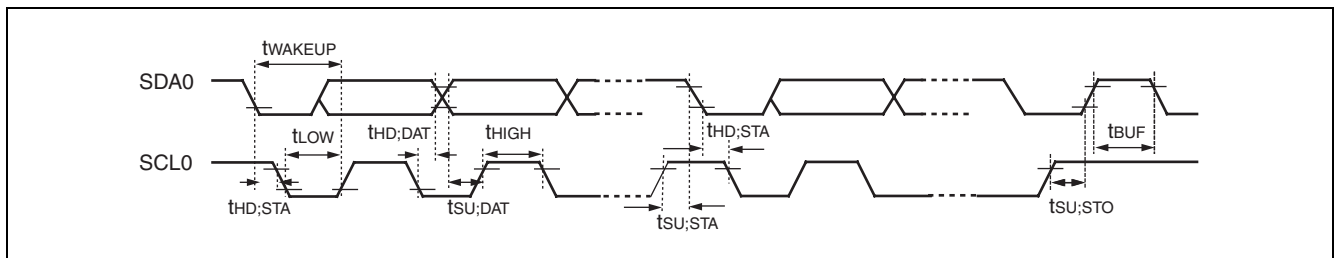
(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	t <sub>HD;STA</sub>	SCL0 SDA0		4.0	—	0.6	—	μs
SCL clock "L" width	t <sub>LOW</sub>	SCL0		4.7	—	1.3	—	μs
SCL clock "H" width	t <sub>HIGH</sub>	SCL0		4.0	—	0.6	—	μs
(Repeat) Start condition set-up time SCL ↑ → SDA ↓	t <sub>SU;STA</sub>	SCL0 SDA0		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HD;DAT</sub>	SCL0 SDA0		0	3.45*2	0	0.9*3	μs
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SU;DAT</sub>	SCL0 SDA0		0.25	—	0.1	—	μs
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SU;STO</sub>	SCL0 SDA0		4	—	0.6	—	μs
Bus free time between stop condition and start condition	t <sub>BUF</sub>	SCL0 SDA0		4.7	—	1.3	—	μs

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HD;DAT</sub> have only to be met if the device dose not stretch the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must then be met.



# MB95100B Series

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL0	R = 1.7 k $\Omega$ , C = 50 pF*1	$(2 + nm / 2) t_{MCLK} - 20$	—	ns	Master mode
SCL clock "H" width	$t_{HIGH}$	SCL0		$(nm / 2) t_{MCLK} - 20$	$(nm / 2) t_{MCLK} + 20$	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0 SDA0		$(-1 + nm / 2) t_{MCLK} - 20$	$(-1 + nm) t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0 SDA0		$(1 + nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0 SDA0		$(1 + nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Master mode
Bus free time between stop condition and start condition	$t_{BUF}$	SCL0 SDA0		$(2 nm + 4) t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		$3 t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		$(-2 + nm / 2) t_{MCLK} - 20$	$(-1 + nm / 2) t_{MCLK} + 20$	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0		$(nm / 2) t_{MCLK} - 20$	$(1 + nm / 2) t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL $\downarrow$ . Maximum value is applied to interrupt at 8th SCL $\downarrow$ .
SCL clock "L" width	$t_{LOW}$	SCL0		$4 t_{MCLK} - 20$	—	ns	At reception
SCL clock "H" width	$t_{HIGH}$	SCL0		$4 t_{MCLK} - 20$	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception

(Continued)

# MB95100B Series

(Continued)

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL0 SDA0	R = 1.7 k $\Omega$ , C = 50 pF*1	$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
Bus free time	$t_{BUF}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		$2 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		$t_{LOW} - 3 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		$t_{MCLK} - 20$	—	ns	At reception
SDA $\downarrow$ →SCL $\uparrow$ (at wakeup function)	$t_{WAKEUP}$	SCL0 SDA0		Oscillation stabilization wait time + $2 t_{MCLK} - 20$	—	ns	

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : • Refer to “(2) Source Clock/Machine Clock” for  $t_{MCLK}$ .

• m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR) .

• n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR) .

• Actual timing of I<sup>2</sup>C is determined by m and n values set by the machine clock ( $t_{MCLK}$ ) and CS4 to CS0 of ICCR0 register.

• Standard-mode :

m and n can be set at the range : 0.9 MHz <  $t_{MCLK}$  (machine clock) < 10 MHz.

Setting of m and n determines the machine clock that can be used below.

(m, n) = (1, 8) : 0.9 MHz <  $t_{MCLK} \leq 1$  MHz

(m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz <  $t_{MCLK} \leq 2$  MHz

(m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz <  $t_{MCLK} \leq 4$  MHz

(m, n) = (1, 98) : 0.9 MHz <  $t_{MCLK} \leq 10$  MHz

• Fast-mode :

m and n can be set at the range : 3.3 MHz <  $t_{MCLK}$  (machine clock) < 10 MHz.

Setting of m and n determines the machine clock that can be used below.

(m, n) = (1, 8) : 3.3 MHz <  $t_{MCLK} \leq 4$  MHz

(m, n) = (1, 22), (5, 4) : 3.3 MHz <  $t_{MCLK} \leq 8$  MHz

(m, n) = (6, 4) : 3.3 MHz <  $t_{MCLK} \leq 10$  MHz

# MB95100B Series

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

( $AV_{CC} = V_{CC} = 1.8 \text{ V to } 3.3 \text{ V}$  [Flash memory product],  $AV_{CC} = V_{CC} = 1.8 \text{ V to } 3.6 \text{ V}$  [MASK ROM product],  
 $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

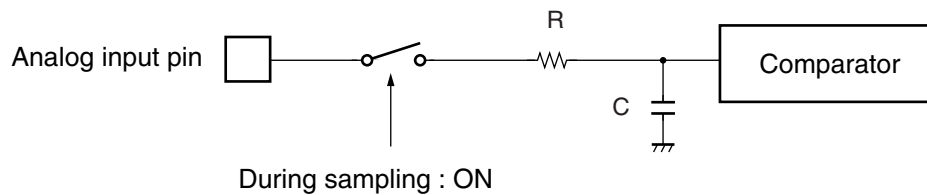
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error			-3.0	—	+3.0	LSB	
Linearity error			-2.5	—	+2.5	LSB	
Differential linear error			-1.9	—	+1.9	LSB	
Zero transition voltage	$V_{OT}$	—	$AV_{SS} - 1.5 \text{ LSB}$	$AV_{SS} + 0.5 \text{ LSB}$	$AV_{SS} + 2.5 \text{ LSB}$	V	Flash memory product : $2.7 \text{ V} \leq AV_{CC} \leq 3.3 \text{ V}$ MASK ROM product : $2.7 \text{ V} \leq AV_{CC} \leq 3.6 \text{ V}$
			$AV_{SS} - 0.5 \text{ LSB}$	$AV_{SS} + 1.5 \text{ LSB}$	$AV_{SS} + 3.5 \text{ LSB}$	V	$1.8 \text{ V} \leq AV_{CC} < 2.7 \text{ V}$
Full-scale transition voltage	$V_{FST}$	—	$AVR - 3.5 \text{ LSB}$	$AVR - 1.5 \text{ LSB}$	$AVR + 0.5 \text{ LSB}$	V	Flash memory product : $2.7 \text{ V} \leq AV_{CC} \leq 3.3 \text{ V}$ MASK ROM product : $2.7 \text{ V} \leq AV_{CC} \leq 3.6 \text{ V}$
			$AVR - 2.5 \text{ LSB}$	$AVR - 0.5 \text{ LSB}$	$AVR + 1.5 \text{ LSB}$	V	$1.8 \text{ V} \leq AV_{CC} < 2.7 \text{ V}$
Compare time	—	—	1.3	—	140	$\mu\text{s}$	Flash memory product : $2.7 \text{ V} \leq AV_{CC} \leq 3.3 \text{ V}$ MASK ROM product : $2.7 \text{ V} \leq AV_{CC} \leq 3.6 \text{ V}$
			20	—	140	$\mu\text{s}$	$1.8 \text{ V} \leq AV_{CC} < 2.7 \text{ V}$
Sampling time	—	—	0.4	—	$\infty$	$\mu\text{s}$	Flash memory product : $2.7 \text{ V} \leq AV_{CC} \leq 3.3 \text{ V}$ MASK ROM product : $2.7 \text{ V} \leq AV_{CC} \leq 3.6 \text{ V}$ external impedance < at 1.8 k $\Omega$
			30	—	$\infty$	$\mu\text{s}$	$1.8 \text{ V} \leq AV_{CC} < 2.7 \text{ V}$ external impedance < at 14.8 k $\Omega$
Analog input current	$I_{AIN}$	—	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage	$V_{AIN}$	—	$AV_{SS}$	—	AVR	V	
Reference voltage	—	—	$AV_{SS} + 1.8$	—	$AV_{CC}$	V	AVR pin
Reference voltage supply current	$I_R$	—	—	400	600	$\mu\text{A}$	AVR pin, During A/D operation
	$I_{RH}$	—	—	—	5	$\mu\text{A}$	AVR pin, At stop mode

## (2) Notes on Using A/D Converter

### • About the external impedance of analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

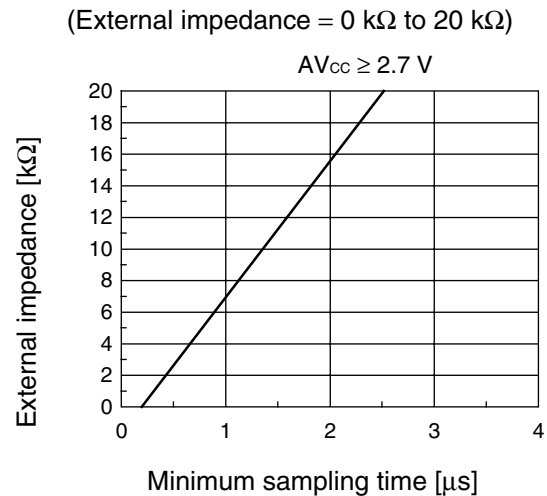
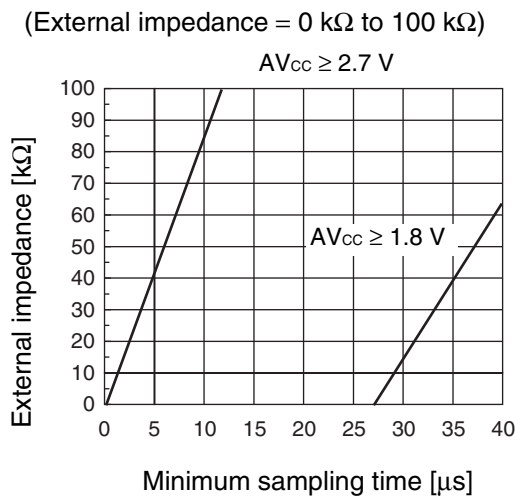
#### • Analog input equivalent circuit



	R	C
$2.7 \text{ V} \leq AV_{CC} \leq 3.6 \text{ V}$	1.7 k $\Omega$ (Max)	14.5 pF (Max)
$1.8 \text{ V} \leq AV_{CC} < 2.7 \text{ V}$	84 k $\Omega$ (Max)	25.2 pF (Max)

Note : The values are reference values.

#### • The relationship between external impedance and minimum sampling time



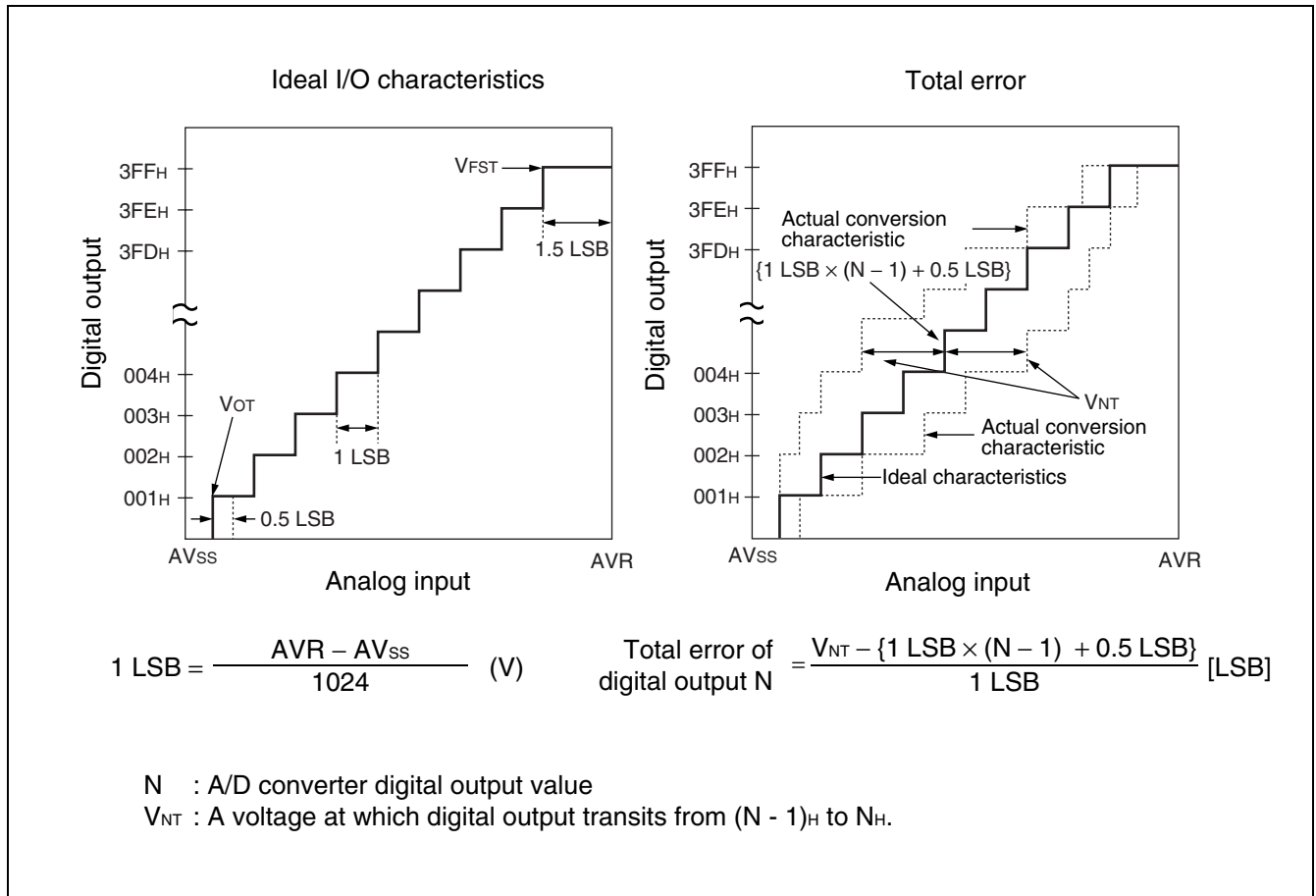
### • About errors

As  $I_{AVR} - AV_{SS}$  becomes smaller, values of relative errors grow larger.

# MB95100B Series

## (3) Definition of A/D Converter Terms

- Resolution  
The level of analog variation that can be distinguished by the A/D converter.  
When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .
- Linearity error (unit : LSB)  
The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)  
Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)  
Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.

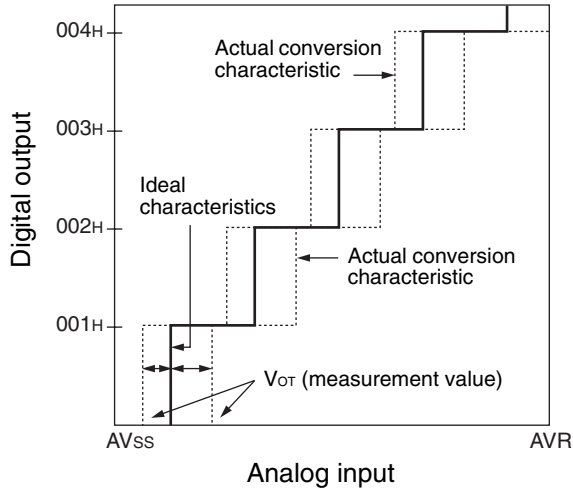


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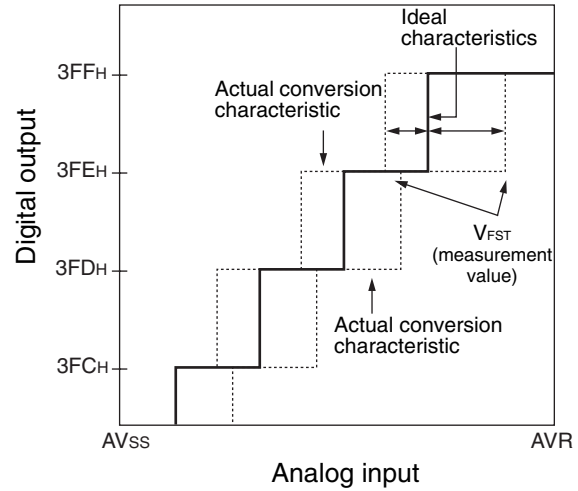


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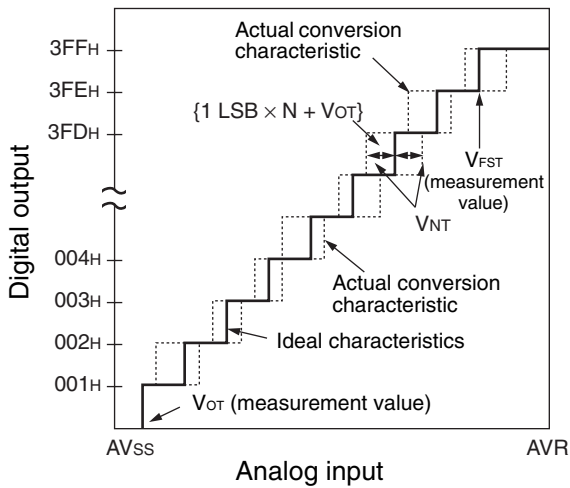
Zero transition error



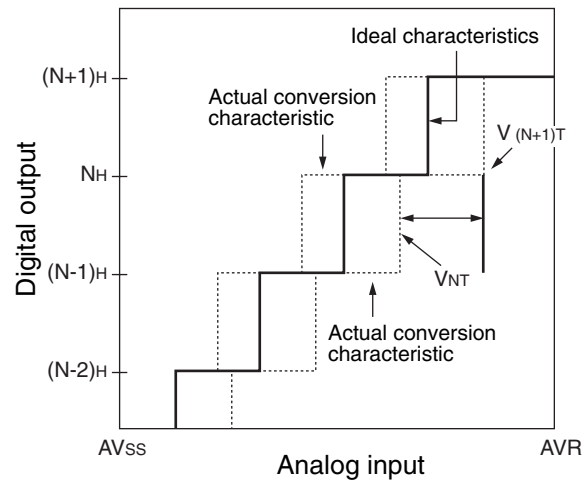
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

- N : A/D converter digital output value
- $V_{NT}$  : A voltage at which digital output transits from (N - 1)<sub>H</sub> to N<sub>H</sub>.
- $V_{OT}$  (Ideal value) =  $AV_{SS} + 0.5 \text{ LSB [V]}$
- $V_{FST}$  (Ideal value) =  $AVR - 1.5 \text{ LSB [V]}$

# MB95100B Series

## 6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4K bytes sector)	—	0.2* <sup>1</sup>	3.0* <sup>2</sup>	s	Excludes 00 <sub>H</sub> programming prior erasure.
Sector erase time (16K bytes sector)	—	0.5* <sup>1</sup>	12.0* <sup>2</sup>	s	Excludes 00 <sub>H</sub> programming prior erasure.
Byte programming time	—	32	3600	μs	Excludes system-level overhead.
Program/erase cycle	10000	—	—	cycle	
Power supply voltage at program/erase	2.7	—	3.3	V	
Flash memory data retention time	20* <sup>3</sup>	—	—	year	Average T <sub>A</sub> = +85 °C

\*1 : T<sub>A</sub> = + 25 °C, V<sub>CC</sub> = 3.0 V, 10000 cycles

\*2 : T<sub>A</sub> = + 85 °C, V<sub>CC</sub> = 2.7 V, 10000 cycles

\*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

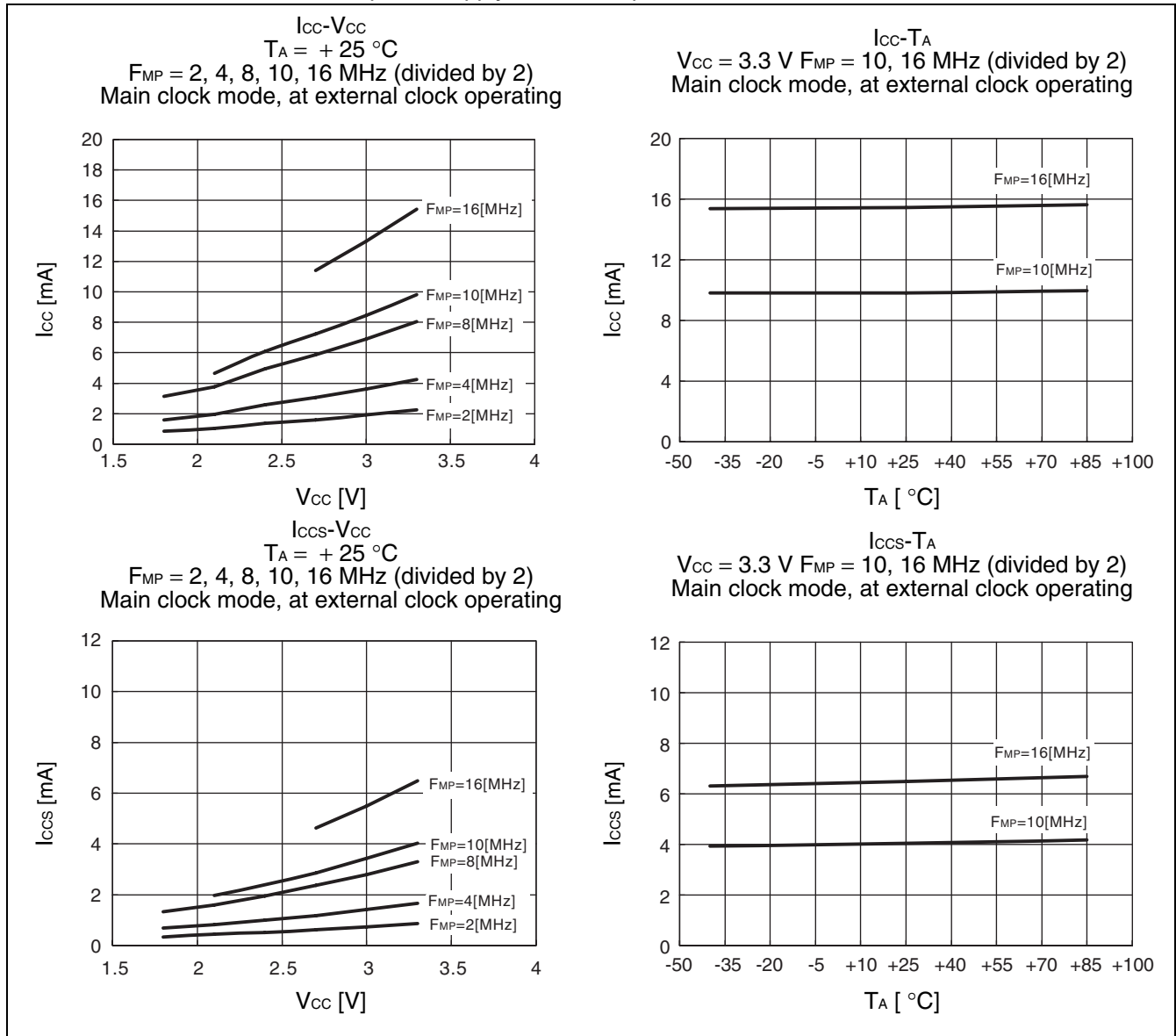
## 7. FRAM Program Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Read/write cycle*	10 <sup>10</sup>	—	—	cycle	
Power supply voltage at read/write	2.7	—	3.6	V	
Data retention time	10	—	—	year	T <sub>A</sub> = 0 °C to +55 °C

\* : Number of data read/write

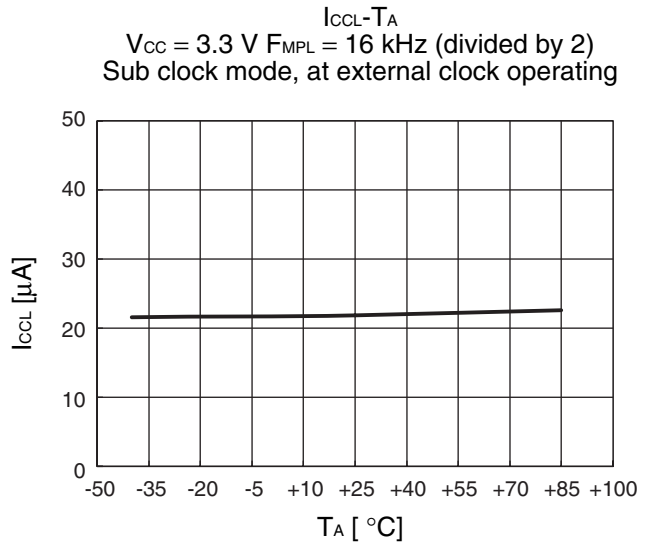
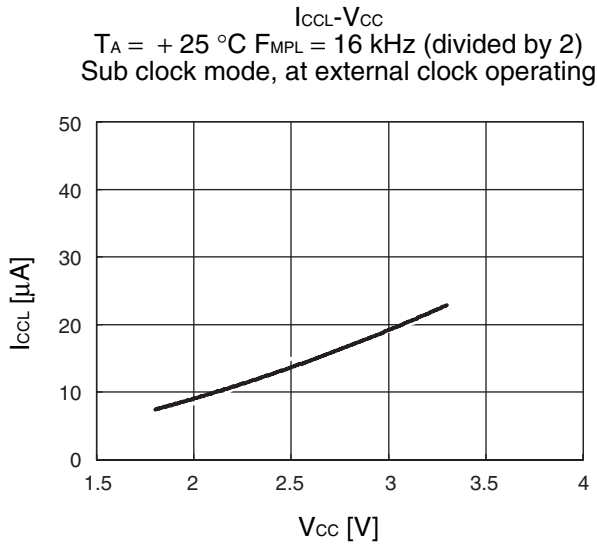
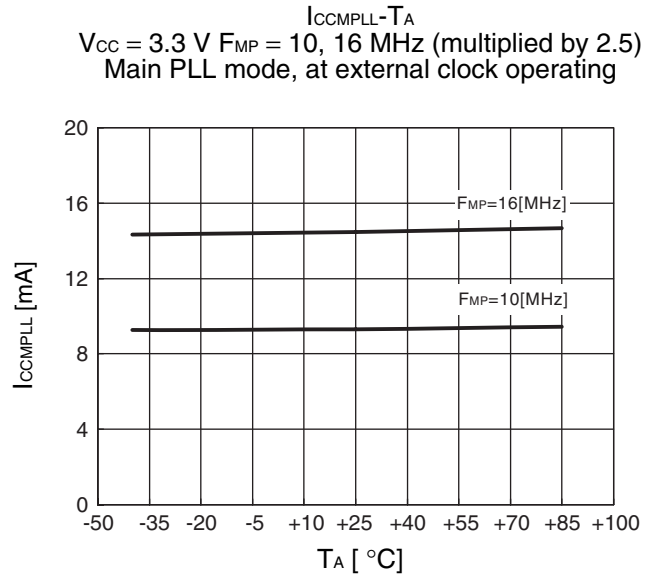
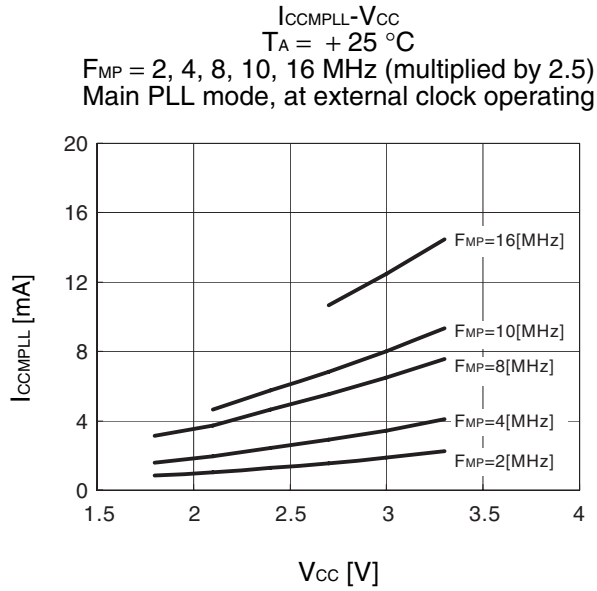
## EXAMPLE CHARACTERISTICS

- MB95F108BS/MB95F108BW power supply current temperature



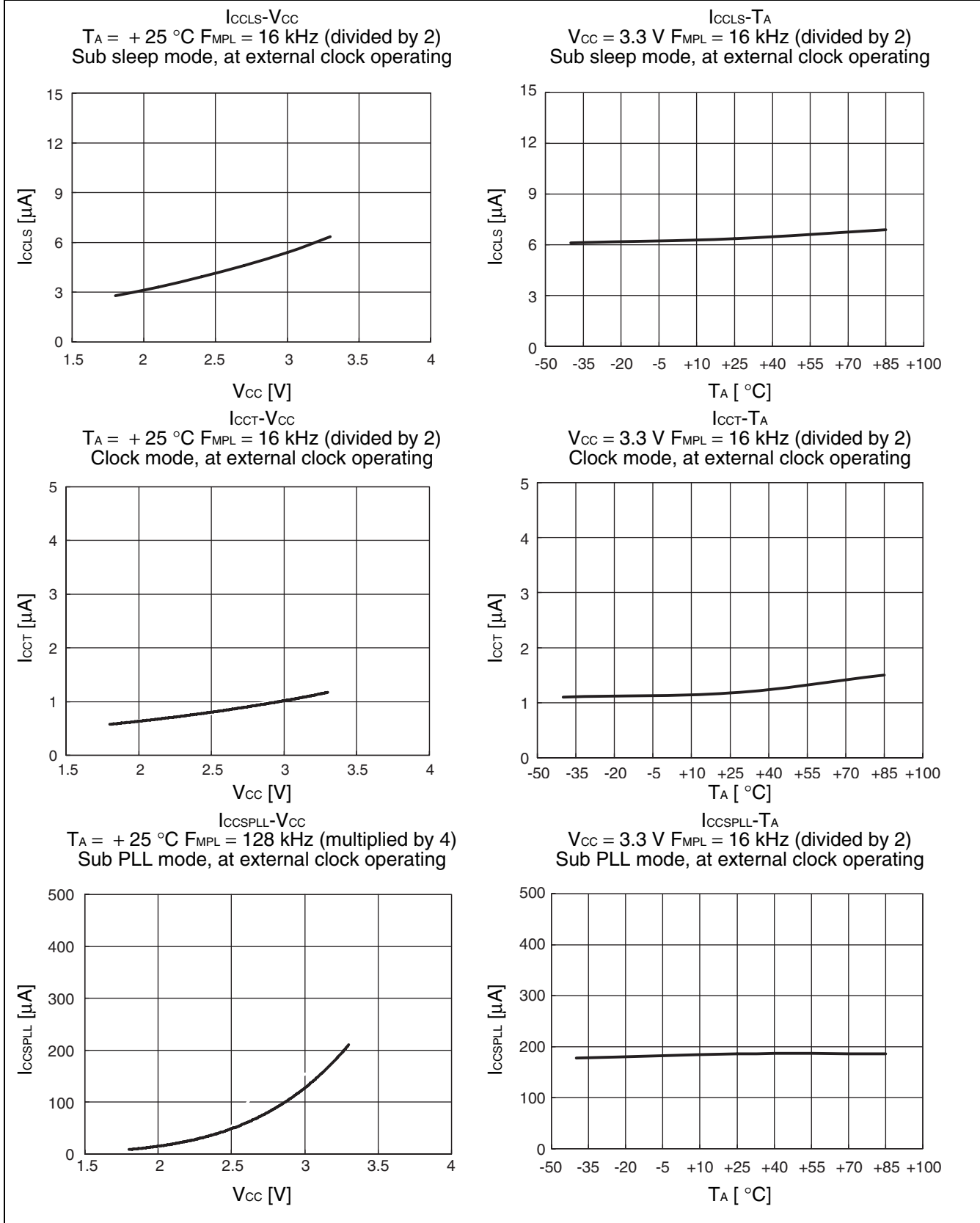
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# MB95100B Series



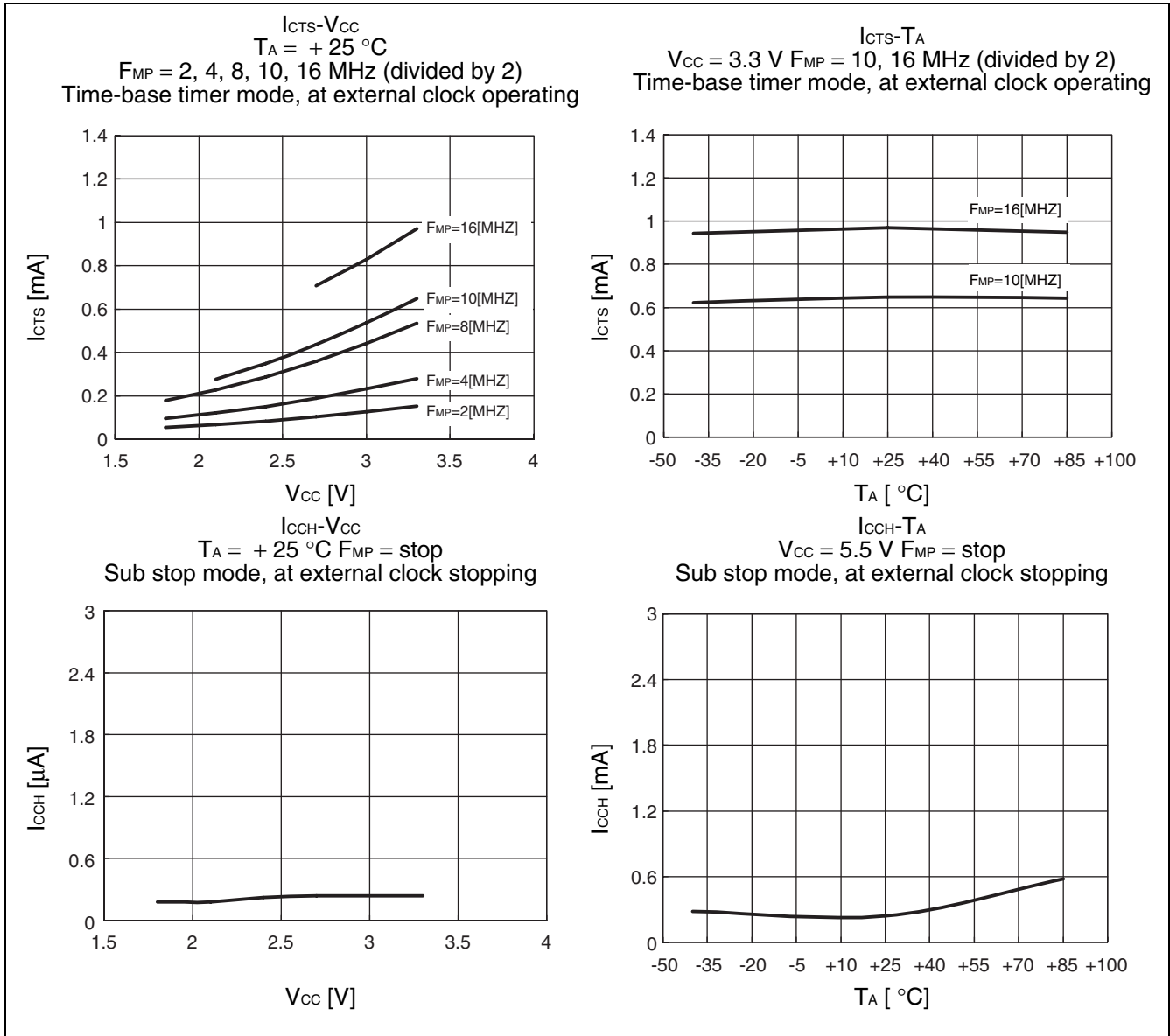
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# MB95100B Series



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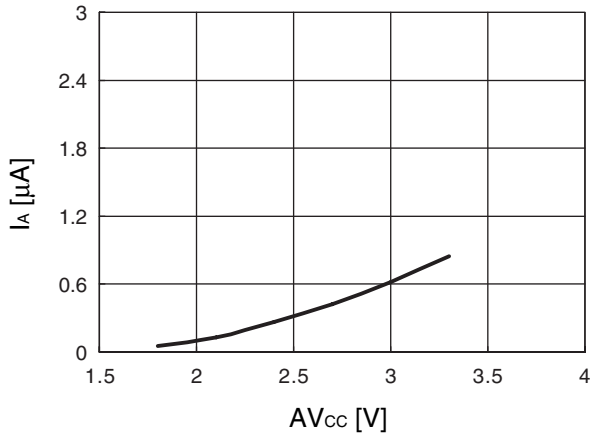
# MB95100B Series



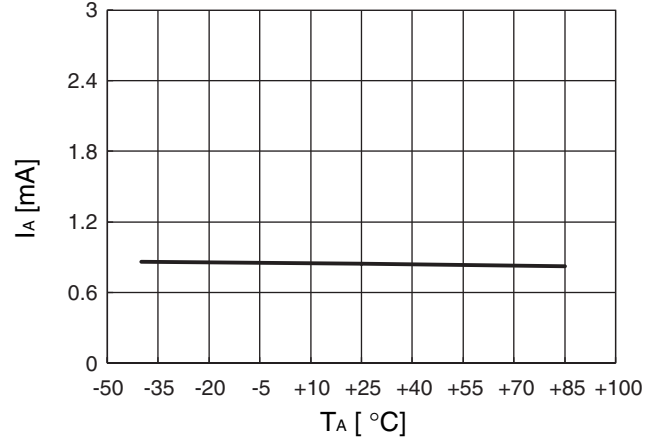
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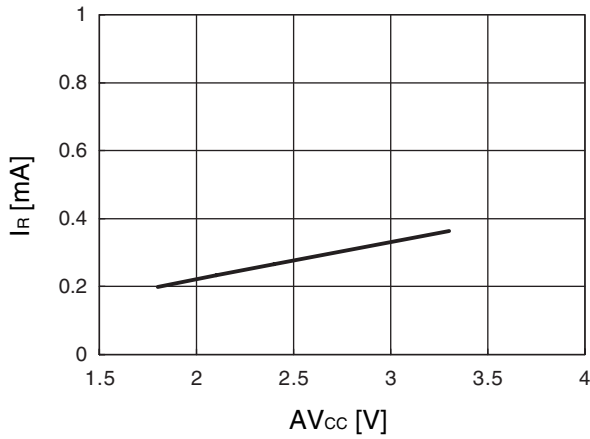
$I_A$ - $AV_{CC}$   
 $T_A = +25\text{ }^\circ\text{C}$   $F_{MP} = 5\text{ MHz}$   
 Operating of A/D conversion,  
 at external clock operating



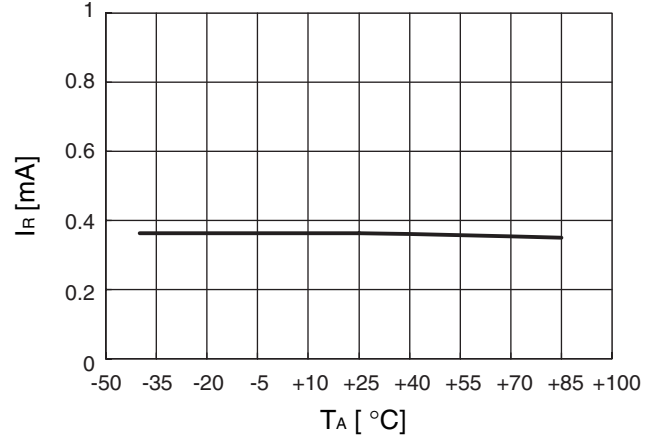
$I_A$ - $T_A$   
 $AV_{CC} = 3.3\text{ V}$   $F_{MP} = 5\text{ MHz}$   
 Operating of A/D conversion,  
 at external clock operating



$I_R$ - $AV_{CC}$   
 $T_A = +25\text{ }^\circ\text{C}$   $F_{MP} = 5\text{ MHz}$   
 Stopping A/D conversion,  
 at external clock operating

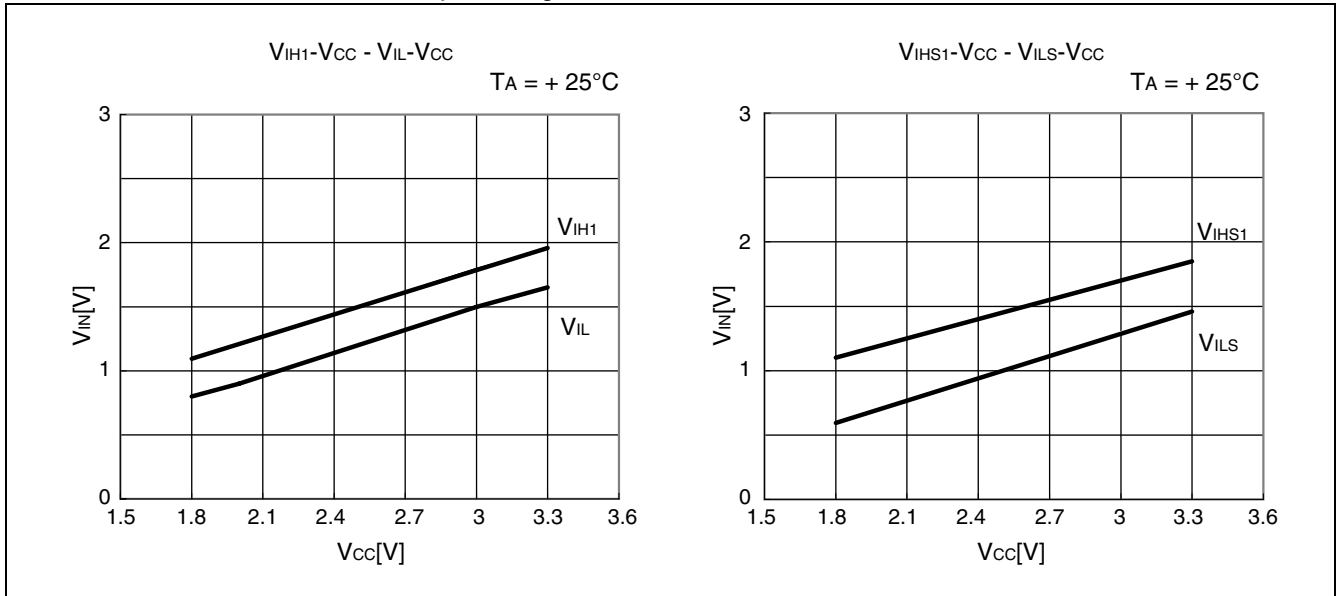


$I_R$ - $T_A$   
 $AV_{CC} = 3.3\text{ V}$   $F_{MP} = 5\text{ MHz}$   
 Stopping A/D conversion,  
 at external clock operating



# MB95100B Series

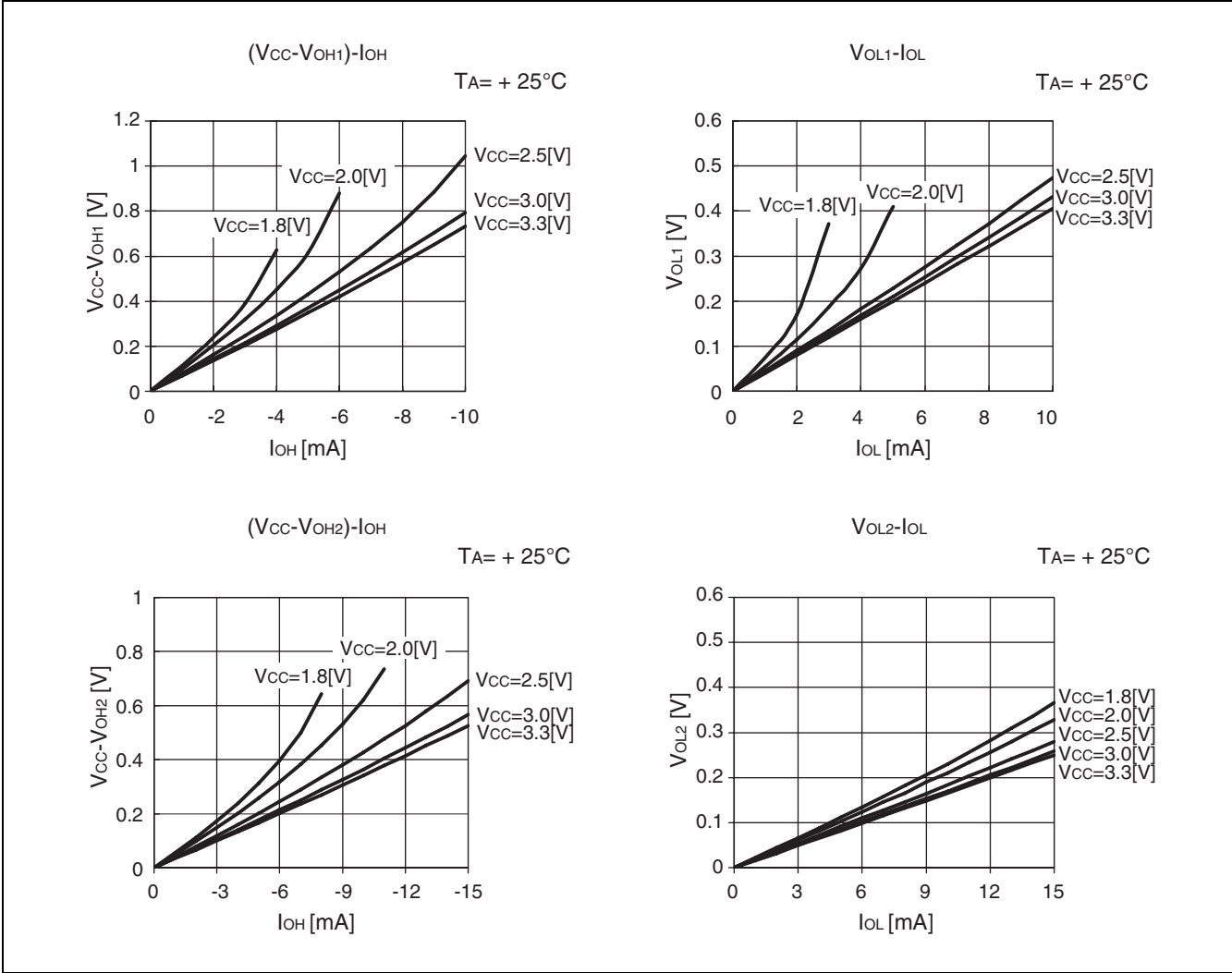
- MB95F108BS/MB95F108BW input voltage characteristics





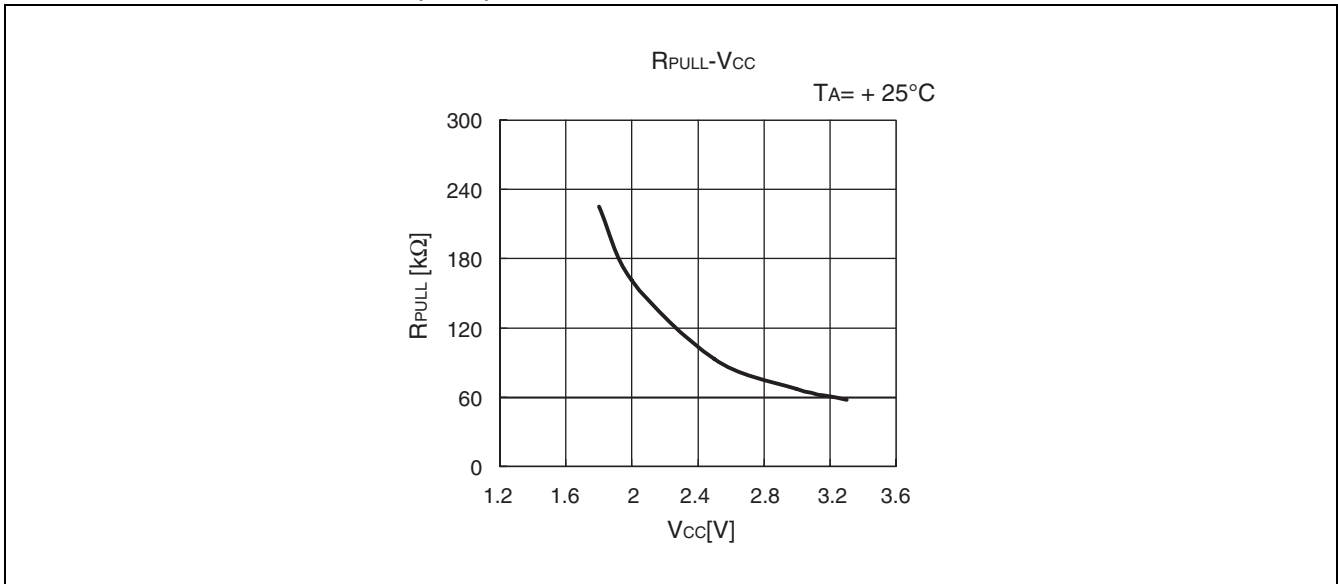
# MB95100B Series

- MB95F108BS/MB95F108BW output voltage characteristics



# MB95100B Series

- MB95F108BS/MB95F108BW pull-up characteristics



## ■ MASK OPTION

No.	Part number	MB95107B	MB95F108BS MB95D108BS	MB95F108BW MB95D108BW	MB95FV100D-101
	Specifying procedure	Specify when ordering MASK	Setting disabled	Setting disabled	Setting disabled
1	Clock mode select* <sup>1</sup> • Single-system clock mode • Dual-system clock mode	Selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	FRAM* <sup>1</sup> • With load of FRAM • Without load of FRAM	No	Specify by part number	Specify by part number	No
3	Low voltage detection reset* <sup>2</sup> • With low voltage detection reset • Without low voltage detection reset	No	No	No	No
4	Clock supervisor* <sup>2</sup> • With clock supervisor • Without clock supervisor	No	No	No	No
5	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Selectable 1 : $(2^2 - 2) / F_{CH}$ 2 : $(2^{12} - 2) / F_{CH}$ 3 : $(2^{13} - 2) / F_{CH}$ 4 : $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$

\*1 : Refer to table below about clock mode select and load of FRAM.

\*2 : Low voltage detection reset and clock supervisor are options of 5-V products.

Part number	Clock mode select	Load of FRAM
MB95107B	Single-system	No
	Dual-system	No
MB95F108BS	Single-system	No
MB95D108BS		Yes
MB95F108BW	Dual-system	No
MB95D108BW		Yes
MB95FV100D-101	Single-system	No
	Dual-system	No

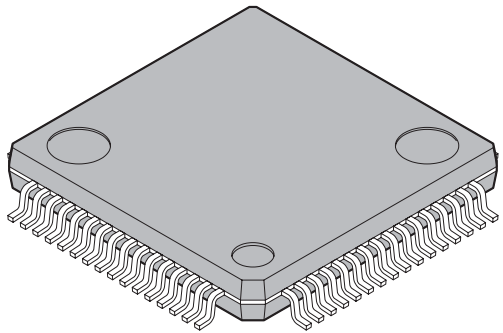
# MB95100B Series

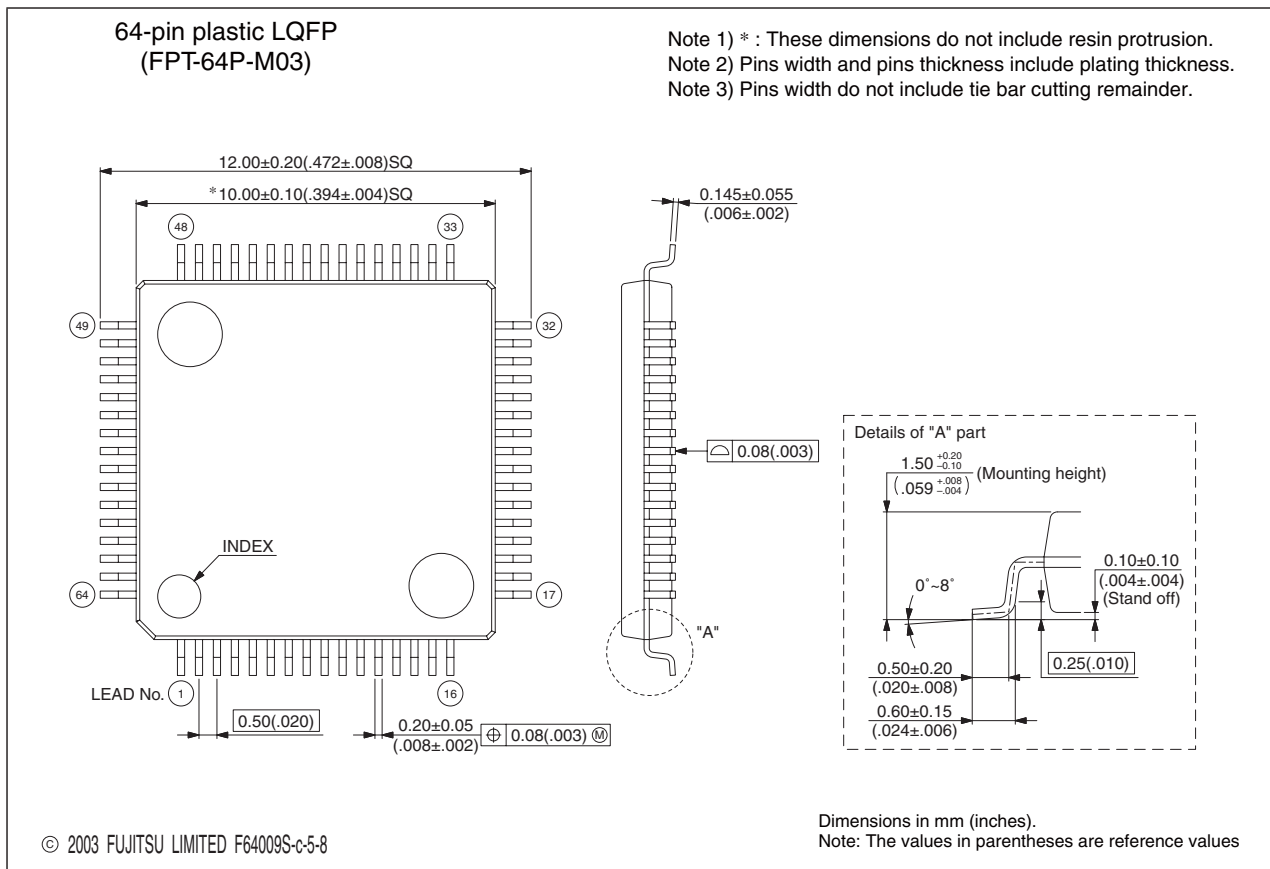
## ■ ORDERING INFORMATION

Part number	Package
MB95107BPFV MB95F108BSPFV MB95F108BWPFV MB95D108BSPFV MB95D108BWPFV	64-pin plastic LQFP (FPT-64P-M03)
MB95107BPFM MB95F108BSPFM MB95F108BWPFM MB95D108BSPFM MB95D108BWPFM	64-pin plastic LQFP (FPT-64P-M09)
MB95107BBGL MB95F108BSBGL MB95F108BWBGL	96-pin plastic FBGA (BGA-96P-M04)
MB2146-301A (MB95FV100D-101PBT)	MCU board ( 224-pin plastic PFBGA ) (BGA-224P-M08)

# MB95100B Series

## ■ PACKAGE DIMENSIONS

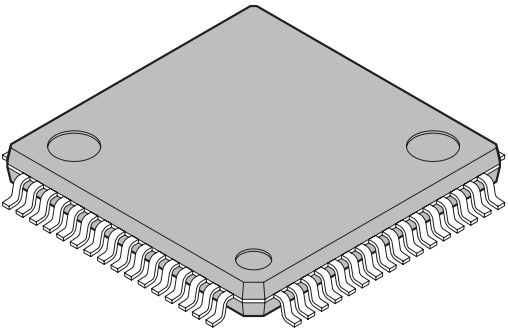
<p>64-pin plastic LQFP</p>  <p>(FPT-64P-M03)</p>	Lead pitch	0.50 mm
	Package width package length	10.0 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32g
	Code (Reference)	P-LFQFP64-10 10-0.50



Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/package/en-search/>

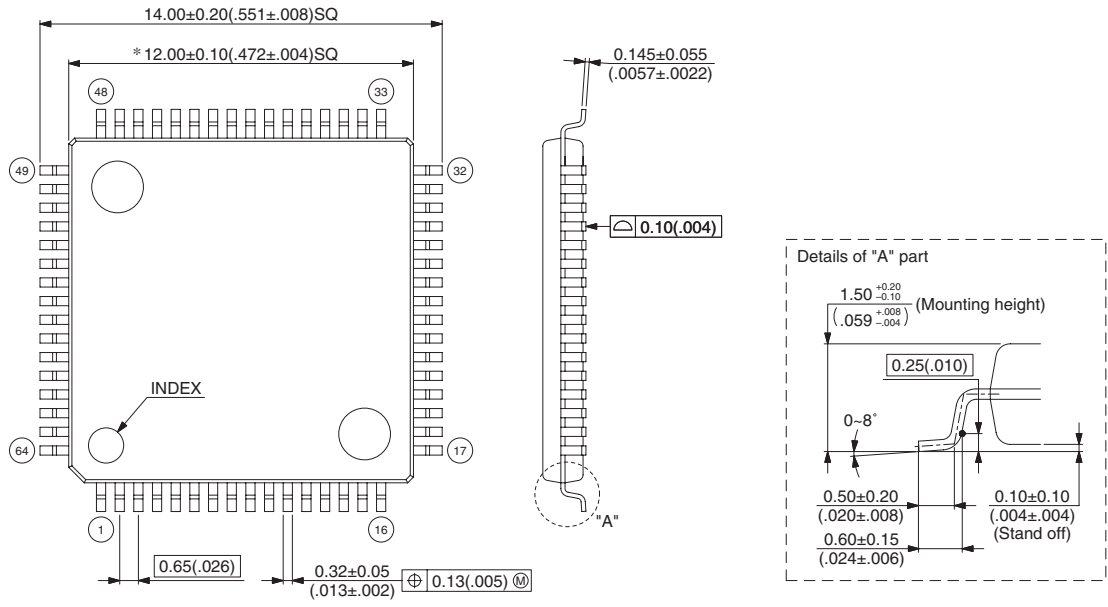
(Continued)

# MB95100B Series

<p>64-pin plastic LQFP</p>  <p>(FPT-64P-M09)</p>	Lead pitch	0.65 mm
	Package width package length	12 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP64-12 12-0.65

64-pin plastic LQFP  
(FPT-64P-M09)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



Top view dimensions:  
 Overall width:  $14.00 \pm 0.20$  ( $.551 \pm .008$ ) SQ  
 Pin pitch:  $0.65$  ( $.026$ )  
 Pin width:  $0.32 \pm 0.05$  ( $.013 \pm .002$ )  
 Pin thickness:  $0.13$  ( $.005$ )  
 INDEX

Side view dimensions:  
 Lead height:  $0.145 \pm 0.055$  ( $.0057 \pm .0022$ )  
 Lead thickness:  $0.10$  ( $.004$ )

Details of "A" part:  
 Mounting height:  $1.50$  ( $.059$ )  
 Lead thickness:  $0.25$  ( $.010$ )  
 Lead angle:  $0 \sim 8^\circ$   
 Stand off:  $0.10 \pm 0.10$  ( $.004 \pm .004$ )  
 Pin width:  $0.50 \pm 0.20$  ( $.020 \pm .008$ )  
 Pin thickness:  $0.60 \pm 0.15$  ( $.024 \pm .006$ )

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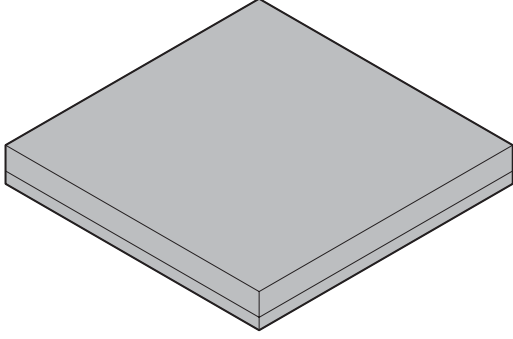
Dimensions in mm (inches).  
 Note: The values in parentheses are reference values.

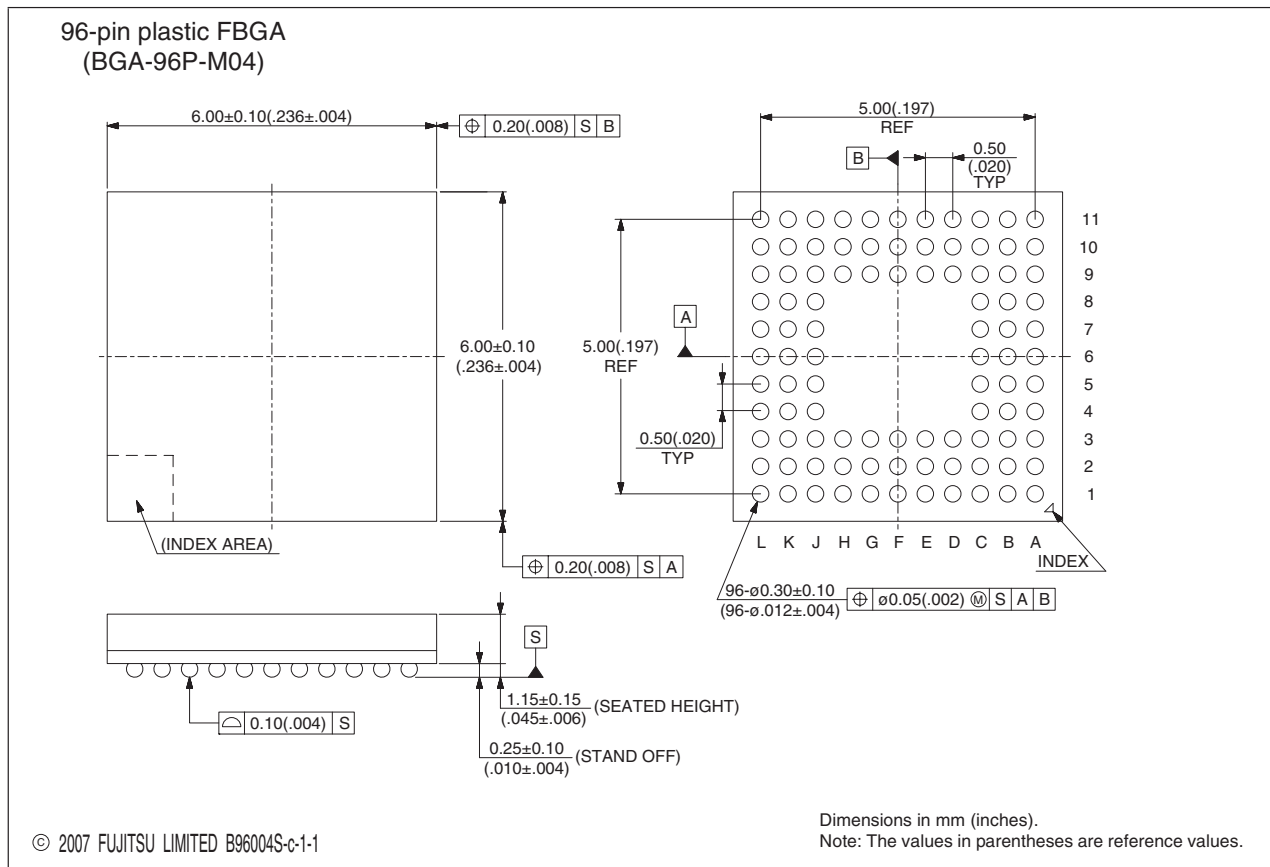
Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/package/en-search/>

(Continued)

# MB95100B Series

(Continued)

 <p>96-pin plastic FBGA</p> <p>(BGA-96P-M04)</p>	Lead pitch	0.50 mm
	Package width package length	6.00 mm 6.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.30 mm MAX
	Weight	0.075 g



Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/package/en-search/>

# MB95100B Series

## ■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the part numbers (MB95R107B).
26	■ I/O MAP	Changed the item “R/W” of Reset source register. R → R/W
43	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (2) Source Clock/Machine Clock	Verified the Min value in the section of “When using main clock” of “Machine clock cycle time (Minimum instruction execution time)”; 100 → 61.5

The vertical lines marked in the left side of the page show the changes.



**MEMO**

**MEMO**

**MEMO**

# MB95100B Series

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