

4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2V–3.6V and 4.5V–5.5V
- Ultra low standby power
 - Typical Standby current: 1 μ A
 - Maximum Standby current: 7 μ A
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-pin TSOP II package

Functional Description

The CY62146ESL is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby

mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The input and output pins (IO₀ through IO₁₅) are placed in a high impedance state when:

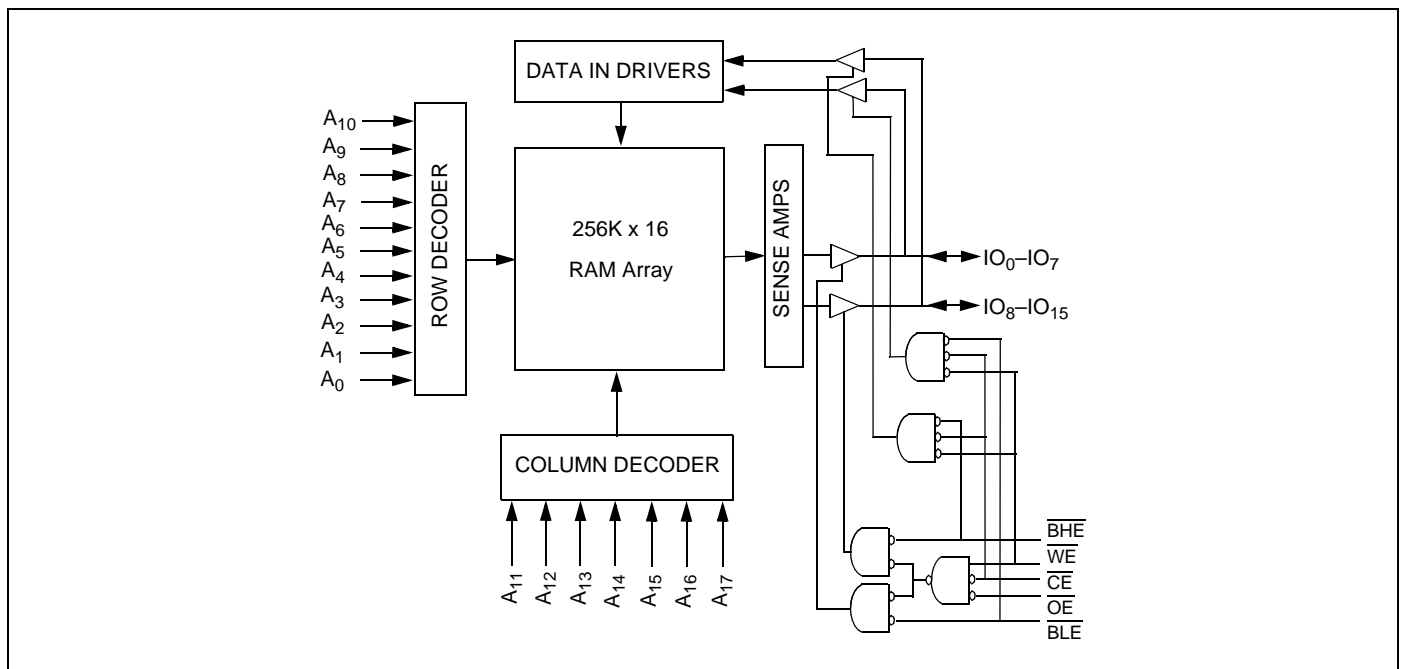
- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (\overline{CE} LOW and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO₀ through IO₇) is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on IO₀ to IO₇. If Byte High Enable (BHE) is LOW, then data from memory appears on IO₈ to IO₁₅. See the "Truth Table" on page 10 for a complete description of read and write modes.

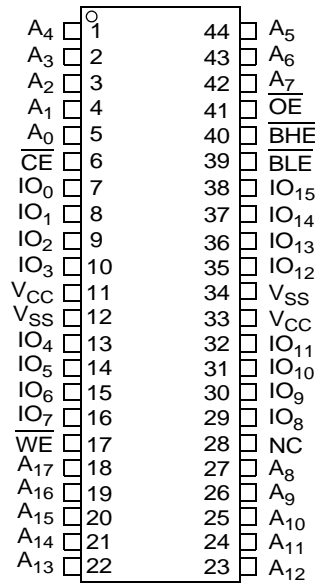
For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Logic Block Diagram



Pin Configuration

Figure 1. 44-Pin TSOP II (Top View) [1]



Product Portfolio

| Product | Range | V _{CC} Range (V) [2] | Speed (ns) | Power Dissipation | | | | | |
|------------|------------|-------------------------------|------------|--------------------------------|-----|----------------------|-----|--------------------------------|-----|
| | | | | Operating I _{CC} (mA) | | | | Standby, I _{SB2} (μA) | |
| | | | | f = 1MHz | | f = f _{max} | | | |
| | | | | Typ [3] | Max | Typ [3] | Max | Typ [3] | Max |
| CY62146ESL | Industrial | 2.2V–3.6V and 4.5V–5.5V | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6V to 4.5V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3V, and V_{CC} = 5V, T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| | |
|---|-----------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied | -55°C to +125°C |
| Supply Voltage to Ground Potential..... | -0.5V to 6.0V |
| DC Voltage Applied to Outputs in High-Z State ^[4, 5] | -0.5V to 6.0V |
| DC Input Voltage ^[4, 5] | -0.5V to 6.0V |

| | |
|--|-----------------------------------|
| Output Current into Outputs (LOW)..... | 20 mA |
| Static Discharge Voltage..... | >2001V (MIL-STD-883, Method 3015) |
| Latch up Current..... | >200 mA |

Operating Range

| Device | Range | Ambient Temperature | V _{CC} ^[6] |
|------------|------------|---------------------|--------------------------------|
| CY62146ESL | Industrial | -40°C to +85°C | 2.2V–3.6V, and 4.5V–5.5V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns | | | Unit | |
|------------------|---|--|--------------------------------------|--------------------|-----------------------|------|----|
| | | | Min | Typ ^[3] | Max | | |
| V _{OH} | Output HIGH Voltage | 2.2 ≤ V _{CC} ≤ 2.7 | I _{OH} = -0.1 mA | 2.0 | | V | |
| | | 2.7 ≤ V _{CC} ≤ 3.6 | I _{OH} = -1.0 mA | 2.4 | | | |
| | | 4.5 ≤ V _{CC} ≤ 5.5 | I _{OH} = -1.0 mA | 2.4 | | | |
| V _{OL} | Output LOW Voltage | 2.2 ≤ V _{CC} ≤ 2.7 | I _{OL} = 0.1 mA | | 0.4 | V | |
| | | 2.7 ≤ V _{CC} ≤ 3.6 | I _{OL} = 2.1mA | | 0.4 | | |
| | | 4.5 ≤ V _{CC} ≤ 5.5 | I _{OL} = 2.1mA | | 0.4 | | |
| V _{IH} | Input HIGH Voltage | 2.2 ≤ V _{CC} ≤ 2.7 | | 1.8 | V _{CC} + 0.3 | V | |
| | | 2.7 ≤ V _{CC} ≤ 3.6 | | 2.2 | V _{CC} + 0.3 | | |
| | | 4.5 ≤ V _{CC} ≤ 5.5 | | 2.2 | V _{CC} + 0.5 | | |
| V _{IL} | Input LOW Voltage | 2.2 ≤ V _{CC} ≤ 2.7 | | -0.3 | 0.6 | V | |
| | | 2.7 ≤ V _{CC} ≤ 3.6 | | -0.3 | 0.8 | | |
| | | 4.5 ≤ V _{CC} ≤ 5.5 | | -0.5 | 0.8 | | |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | | -1 | +1 | μA | |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | | -1 | +1 | μA | |
| I _{CC} | V _{CC} Operating Supply Current | f = f _{max} = 1/t _{RC} | V _{CC} = V _{CCmax} | | 15 | 20 | mA |
| | | f = 1 MHz | I _{OUT} = 0 mA, CMOS levels | | 2 | 2.5 | |
| I _{SB1} | Automatic CE Power down Current — CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (\overline{OE} , \overline{BHE} , \overline{BLE} and \overline{WE}), V _{CC} = V _{CC(max)} | | | 1 | 7 | μA |
| I _{SB2} | Automatic CE Power down Current — CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = V _{CC(max)} | | | 1 | 7 | μA |

Notes

- V_{IL}(min) = -2.0V for pulse durations less than 20 ns.
- V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

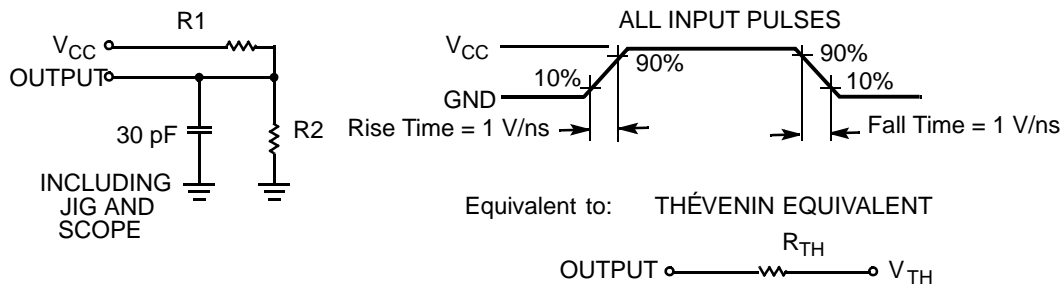
| Parameter | Description | Test Conditions | Max | Unit |
|------------------|--------------------|---|-----|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | TSOP II | Unit |
|-----------------|--|--|---------|------|
| Θ _{JA} | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 77 | °C/W |
| Θ _{JC} | Thermal Resistance (Junction to Case) | | 13 | °C/W |

AC Test Loads and Waveforms



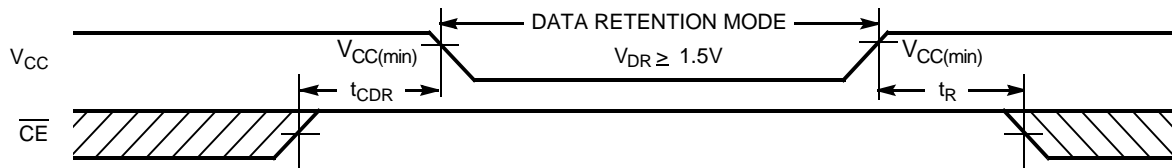
| Parameters | 2.5V | 3.0V | 5.0V | Unit |
|-----------------|-------|------|------|------|
| R1 | 16667 | 1103 | 1800 | Ω |
| R2 | 15385 | 1554 | 990 | Ω |
| R _{TH} | 8000 | 645 | 639 | Ω |
| V _{TH} | 1.20 | 1.75 | 1.77 | V |

Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[3] | Max | Unit |
|---------------------------------|--------------------------------------|--|-----------------|--------------------|-----|------|
| V _{DR} | V _{CC} for Data Retention | | 1.5 | | | V |
| I _{CCDR} | Data Retention Current | $\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 1 | 7 | μA |
| t _{CDR} ^[7] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| t _R ^[8] | Operation Recovery Time | | t _{RC} | | | ns |

Data Retention Waveform



Notes

- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.

Switching Characteristics

Over the Operating Range ^[9]

| Parameter | Description | 45 ns | | Unit |
|-----------------------------------|---|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t _{RC} | Read Cycle Time | 45 | | ns |
| t _{AA} | Address to Data Valid | | 45 | ns |
| t _{OHA} | Data Hold from Address Change | 10 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 45 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 22 | ns |
| t _{LZOE} | \overline{OE} LOW to Low-Z ^[10] | 5 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High-Z ^[10, 11] | | 18 | ns |
| t _{LZCE} | \overline{CE} LOW to Low-Z ^[10] | 10 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High-Z ^[10, 11] | | 18 | ns |
| t _{PU} | \overline{CE} LOW to Power Up | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power Down | | 45 | ns |
| t _{DBE} | $\overline{BLE/BHE}$ LOW to Data Valid | | 22 | ns |
| t _{LZBE} | $\overline{BLE/BHE}$ LOW to Low-Z ^[10] | 5 | | ns |
| t _{HZBE} | $\overline{BLE/BHE}$ HIGH to High-Z ^[10, 11] | | 18 | ns |
| Write Cycle^[12] | | | | |
| t _{WC} | Write Cycle Time | 45 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 35 | | ns |
| t _{AW} | Address Setup to Write End | 35 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | ns |
| t _{SA} | Address Setup to Write Start | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 35 | | ns |
| t _{BW} | $\overline{BLE/BHE}$ LOW to Write End | 35 | | ns |
| t _{SD} | Data Setup to Write End | 25 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | ns |
| t _{HZWE} | \overline{WE} LOW to High-Z ^[10, 11] | | 18 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low-Z ^[10] | 10 | | ns |

Notes

9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified I_{OL}/I_{OH} as shown in the [AC Test Loads and Waveforms on page 4](#).
10. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 2. Read Cycle No.1: Address Transition Controlled. [13, 14]

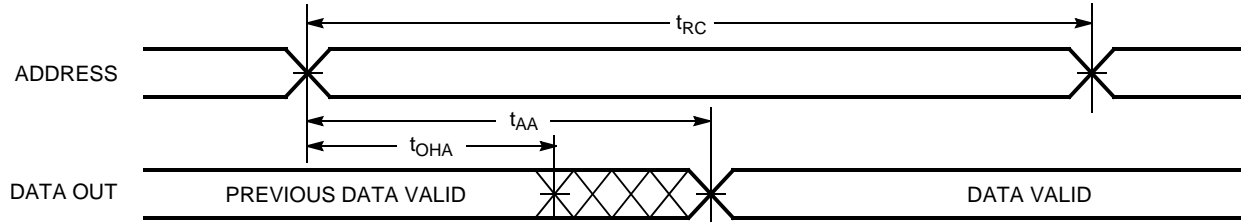
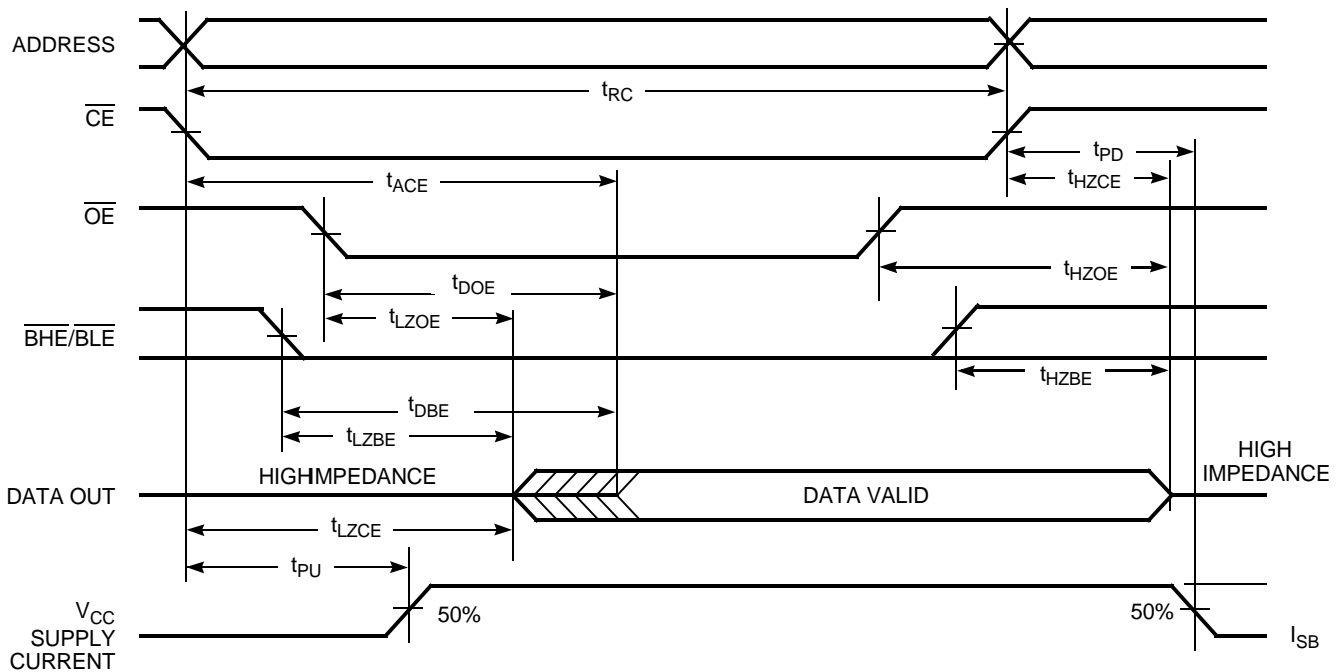


Figure 3. Read Cycle No. 2: $\overline{\text{OE}}$ Controlled [14, 15]



Notes

13. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$ = V_{IL} , $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} .
14. $\overline{\text{WE}}$ is HIGH for read cycle.
15. Address valid before or similar to $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)

Figure 4. Write Cycle No 1: $\overline{\text{WE}}$ Controlled [12, 16, 17]

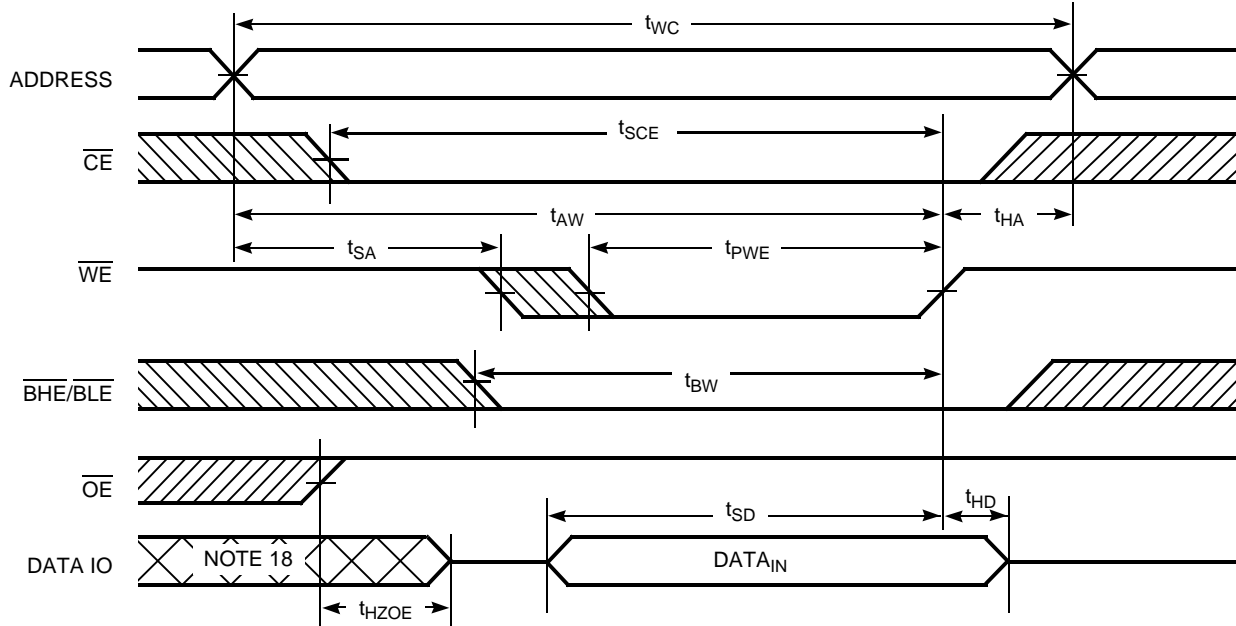
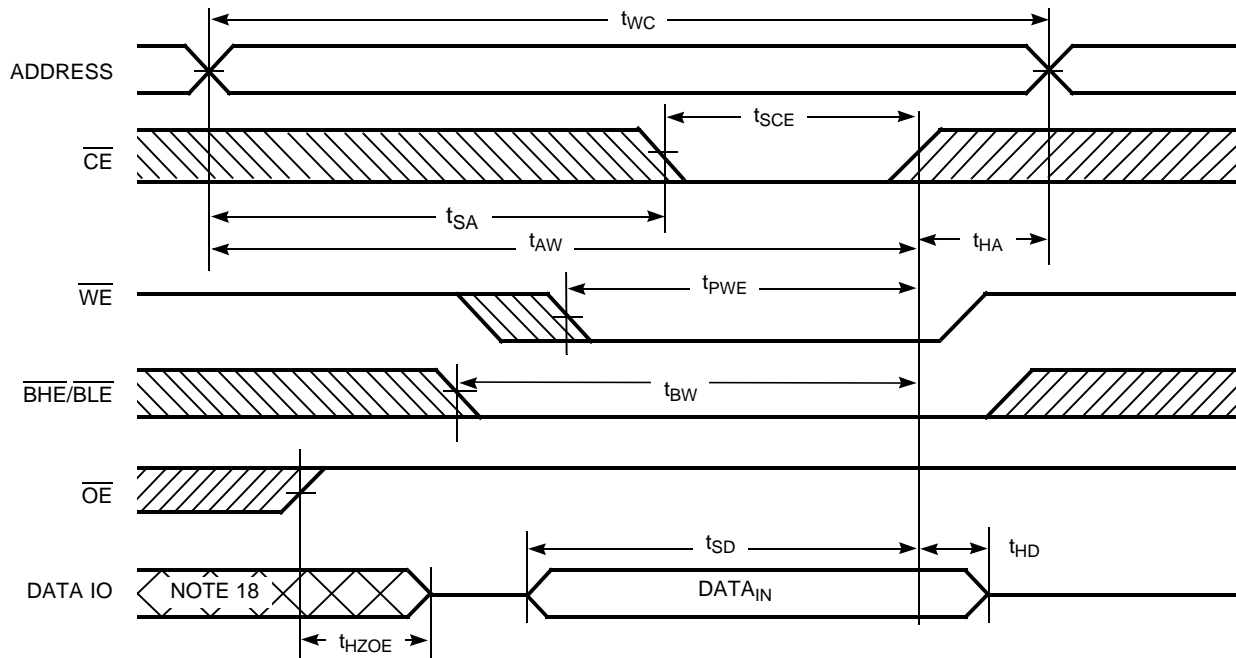


Figure 5. Write Cycle 2: $\overline{\text{CE}}$ Controlled [12, 16, 17]



Notes

- 16. Data IO is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\text{WE} = V_{IH}$, the output remains in a high impedance state.
- 18. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle 3: \overline{WE} controlled, \overline{OE} LOW ^[17]

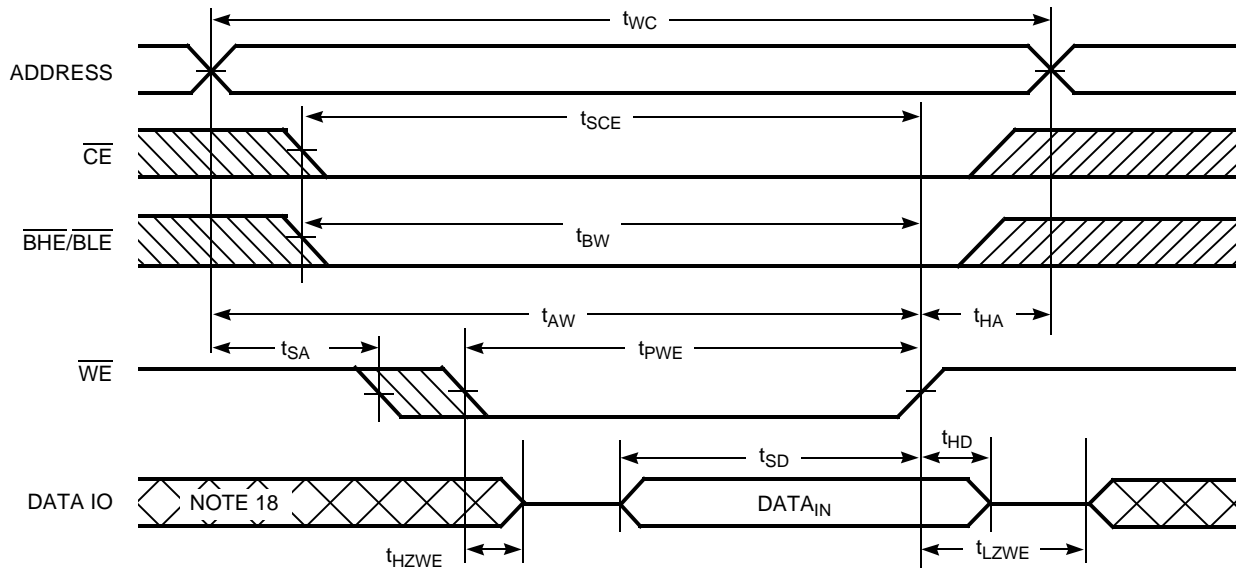
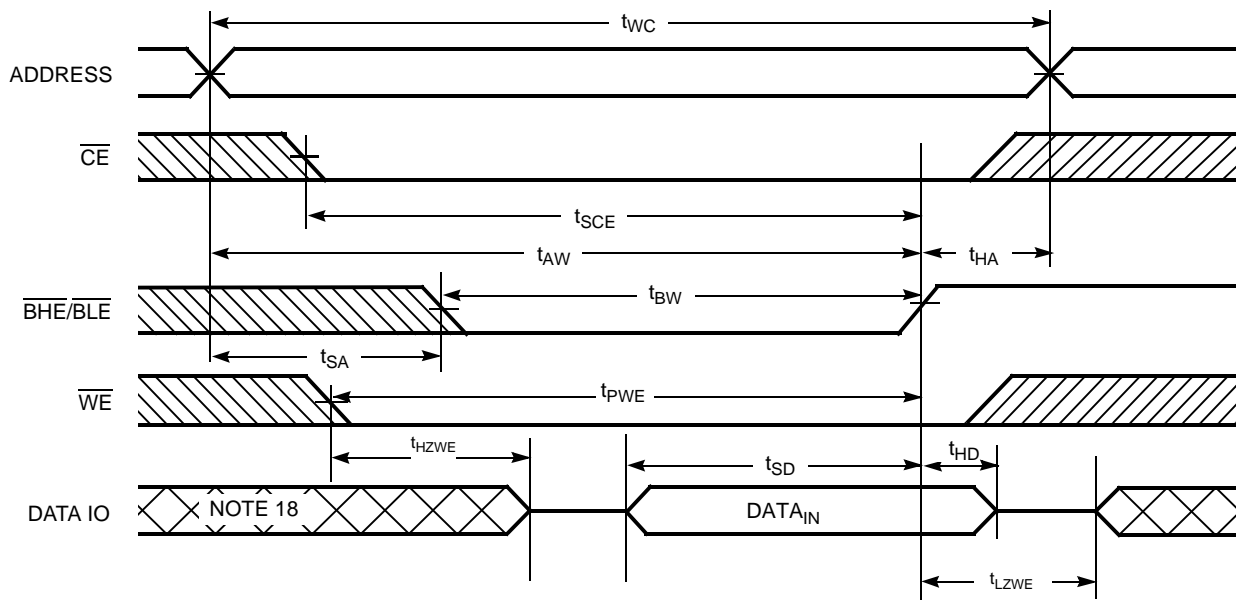


Figure 7. Write Cycle 4: $\overline{BHE/BLE}$ Controlled, \overline{OE} LOW ^[17]



Truth Table

| \overline{CE} | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|---|---------------------|----------------------|
| H | X | X | X | X | High-Z | Deselect/Power down | Standby (I_{SB}) |
| L | X | X | H | H | High-Z | Output Disabled | Active (I_{CC}) |
| L | H | L | L | L | Data Out (IO_0 – IO_{15}) | Read | Active (I_{CC}) |
| L | H | L | H | L | Data Out (IO_0 – IO_7); IO_8 – IO_{15} in High-Z | Read | Active (I_{CC}) |
| L | H | L | L | H | Data Out (IO_8 – IO_{15}); IO_0 – IO_7 in High-Z | Read | Active (I_{CC}) |
| L | H | H | L | L | High-Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | L | High-Z | Output Disabled | Active (I_{CC}) |
| L | H | H | L | H | High-Z | Output Disabled | Active (I_{CC}) |
| L | L | X | L | L | Data In (IO_0 – IO_{15}) | Write | Active (I_{CC}) |
| L | L | X | H | L | Data In (IO_0 – IO_7); IO_8 – IO_{15} in High-Z | Write | Active (I_{CC}) |
| L | L | X | L | H | Data In (IO_8 – IO_{15}); IO_0 – IO_7 in High-Z | Write | Active (I_{CC}) |

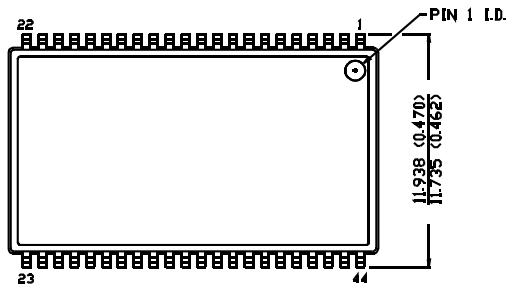
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-------------------|-----------------|---|-----------------|
| 45 | CY62146ESL-45ZSXI | 51-85087 | 44-pin Thin Small Outline Package Type II (Pb-free) | Industrial |

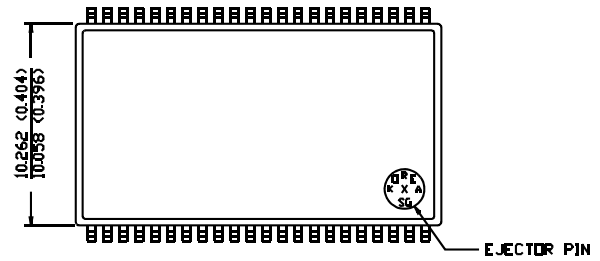
Package Diagrams

Figure 8. 44-Pin TSOP II, 51-85087

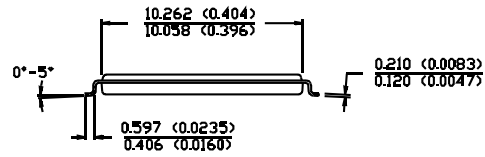
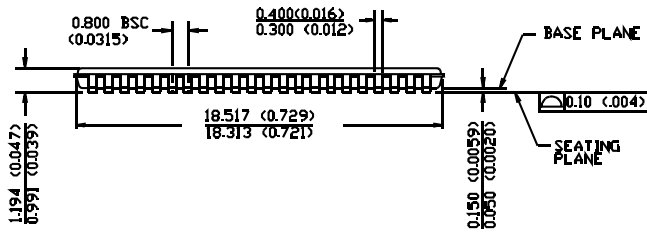
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

Document History Page

| Document Title: CY62146ESL MoBL [®] 4-Mbit (256K x 16) Static RAM Document Number: 001-43142 | | | | |
|--|---------|------------|-----------------|-----------------------|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 1875228 | See ECN | VKN/AESA | New Data Sheet |

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