Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No-Spread Spectrum (XO) Option

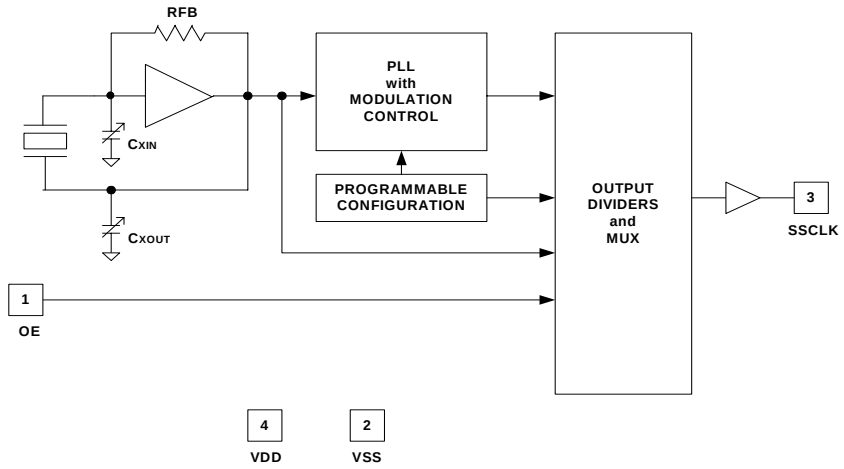
Features

- Crystal Oscillator with Spread Spectrum Clock (SSXO)
- No Spread Spectrum (XO) Option
- Wide operating output clock frequency range of 10–166 MHz
- Programmable spread spectrum with nominal 31.5 kHz modulation frequency
- Center spread: ±0.25% to ±2.0%
- Down spread: –0.5% to –4.0%
- No spread: ± 0.0%
- Integrated phase-locked loop (PLL)
- 85 ps typical cycle-to-cycle Jitter with SSCLK = 133 MHz
- 3.3V operation
- Output Enable function
- Package available in 4-Pin Ceramic LCC SMD
- Pb-free package
- Industrial Temperature from –40°C to 85°C

Benefits

- Provides a wide range of spread percentages for maximum electromagnetic interference (EMI) reduction to meet regulatory agency electromagnetic compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
- This versatile programming feature enables the user to switch between SSXO (with Spread) and XO (without Spread) functions with ease.
- Internal PLL to generate up to 166 MHz output.
- Suitable for most PC, consumer, and networking applications
- Application compatibility in standard and low-power systems
- In-house programming of samples and prototype quantities is available using CY3672 programming kit and CY3724 socket adapters. Production quantities are available through Cypress's value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others.

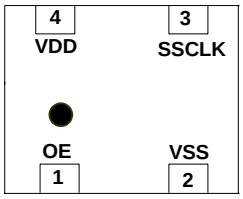
Logic Block Diagram



Pin Configuration

CY25701

4-pin Ceramic SMD



Pin Definition

Pin	Name	Description
1	OE	Output Enable pin: Active HIGH. If OE = 1, SSCLK is enabled
2	VSS	Power supply ground
3	SSCLK	Spread spectrum clock output (with or without spread)
4	VDD	3.3V power supply

Functional Description

The CY25701 is a Spread Spectrum Crystal Oscillator (SSXO) IC used to reduce the EMI found in today's high-speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the embedded input crystal. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

The CY25701 uses a programmable configuration memory array to synthesize output frequency and spread%.

The spread% is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.00%. The range for down spread is from –0.5% to –4.0%. Contact the factory for smaller or larger spread% amounts if required. Refer to *Table 2* for spread selection and no-spread values.

The frequency modulated SSCLK output can be programmed from 10 to 166 MHz.

The CY25701 is available in a 4-pin ceramic SMD package with an operating temperature range of –40 to 85°C.

Programming Description

Factory/Field Programmable CY25701

Factory/Field programming is available for samples and manufacturing by Cypress and its distributors. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or Sales Representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample request and the production orders. Contact your local Cypress FAE or sales representative for details.

Additional information on the CY25701 can be obtained from the Cypress web site at www.cypress.com.

Output Frequency, SSCLK Output (SSCLK, pin 3)

The modulated frequency at the SSCLK output is produced by synthesizing from the embedded crystal oscillator frequency input. The range of synthesized clock is from 10 to 166 MHz.

Spread Percentage (SSCLK, pin 3)

The SSCLK spread can be programmed to various spread percentage values from ±0.25% to ±2.0% for Center Spread and from –0.5% to –4.0% for Down Spread. Refer to *Table 2* for available spread options. Enter ±0.0% (No spread) for XO (Crystal Oscillator) without spread option.

Frequency Modulation (SSCLK, pin 3)

The default frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 10 to 166 MHz. Alternate frequency modulations at 30.1 kHz or 32.9 kHz can be selected via Cyberclocks software. Contact the factory for other alternate modulation frequencies if required.

Table 1. Programming Data Requirement

Pin Function	Output Frequency	Spread Percent Code[1]	Frequency Modulation
Pin Name	SSCLK	SSCLK	SSCLK
Pin#	3	3	3
Units	MHz	%	kHz
Program Value	**ENTER DATA**	**ENTER DATA**	**31.5**

Note
1. ±0.0% or Code "Z" for XO (No-Spread) option.

Table 2. Spread Percent Selection

Center Spread	Code	A	B	C	D	E	F	Z
	Percentage	±0.25%	±0.5%	±0.75%	±1.0%	±1.5%	±2.0%	±0.0%
Down Spread	Code	G	H	J	K	L	M	Z
	Percentage	–0.5%	–1.0%	–1.5%	–2.0%	–3.0%	–4.0%	±0.0%

Absolute Maximum Ratings

Supply Voltage (VDD) ..... –0.5V to +7.0V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5V
Storage Temperature (Non-condensing) .... –55°C to +100°C
Junction Temperature ..... –40°C to +125°C
Data Retention @ Tj = 125°C ..... >10 years
Package Power Dissipation ..... 350 mW

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.00	3.30	3.60	V
T_A	Ambient Temperature (Commercial)	–20	–	70	°C
T_A	Ambient Temperature (Industrial)	–40	–	85	°C
C_{LOAD}	Max. Load Capacitance @ pin 3	–	–	15	pF
F_{SSCLK}	SSCLK output frequency, C_{LOAD} = 15 pF	10	–	166	MHz
F_{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
T_{PU}	Power-up time for VDD to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current (pin 3)	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V (source)	10	12	–	mA
I_{OL}	Output Low Current (pin 3)	V_{OL} = 0.5, V_{DD}= 3.3V (sink)	10	12	–	mA
V_{IH}	Input High Voltage (pin 1)	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	Input Low Voltage (pin 1)	CMOS levels, 30% of V_{DD}	–	–	$0.3V_{DD}$	V
I_{IH}	Input High Current (pin 1)	$V_{in} = V_{DD}$	–	–	10	µA
I_{IL}	Input Low Current (pin 1)	$V_{in} = V_{SS}$	–	–	10	µA
I_{OZ}	Output Leakage Current (pin 3)	Three-state output, OE = 0	–10	–	10	µA
C_{IN}[2]	Input Capacitance (pin 1)	Pin 1, or OE	–	5	7	pF
I_{VDD}	Supply Current	V_{DD} = 3.3V, SSCLK = 10 to 166 MHz, C_{LOAD} = 0, OE = V_{DD}	–	–	50	mA
Δf/f	Initial Accuracy at room temp.	T_A = 25°C, 3.3V	–25	–	25	ppm
	Freq. Stability over temp. range	T_A = –20°C to 70°C, 3.3V	–25	–	25	ppm
	Freq. Stability over voltage range	3.0 to 3.6V	–12	–	12	ppm
	Aging	T_A = 25°C, First year	–5	–	5	ppm

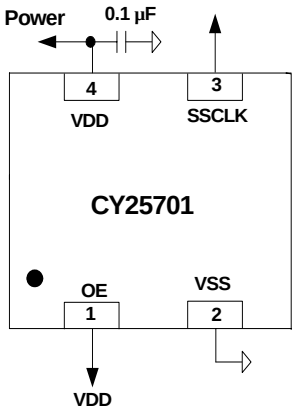
Note
2. Guaranteed by characterization, not 100% tested.

AC Electrical Characteristics[2]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
t_R	Output Rise Time	20%–80% of V_{DD}, C_L = 15 pF	–	–	2.7	ns
t_F	Output Fall Time	20%–80% of V_{DD}, C_L = 15 pF	–	–	2.7	ns
T_{CCJ1}[3]	Cycle-to-Cycle Jitter SSCLK (Pin 3)	SSCLK ≥133 MHz, Measured at $V_{DD}/2$	–	85	200	ps
		25 MHz ≤ SSCLK <133 MHz, Measured at $V_{DD}/2$	–	215	400	ps
		SSCLK < 25 MHz, Measured at $V_{DD}/2$	–	–	1% of 1/SSCK	s
T_{OE1}	Output Disable Time (pin1 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin1 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
T_{LOCK}	PLL Lock Time	Time for SSCLK to reach valid frequency	–	–	10	ms

Application Circuit

Figure 1. Application Circuit Diagram



Note

3. Jitter is configuration dependent. Actual jitter is dependent on output frequencies, spread percentage, temperature, and output load. For more information, refer to the application note, “Jitter in PLL Based Systems: Causes, Effects, and Solutions” available at http://www.cypress.com/clock/appnotes.html, or contact your local Cypress Field Application Engineer.

Switching Waveforms

Figure 2. Duty Cycle Waveform

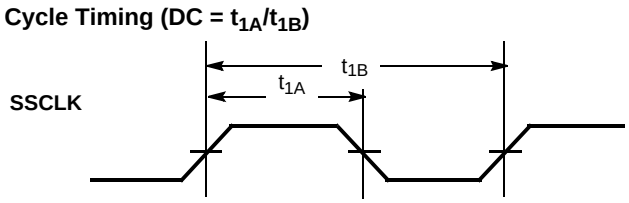
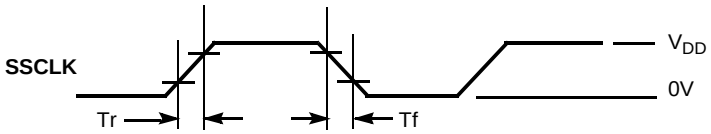
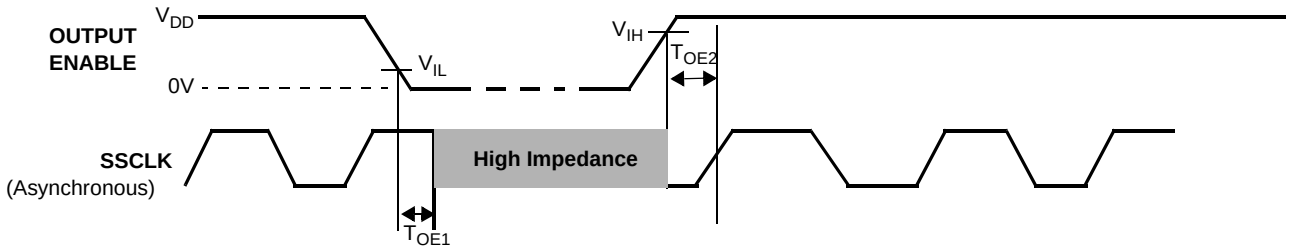


Figure 3. Output Rise/Fall Time Waveform

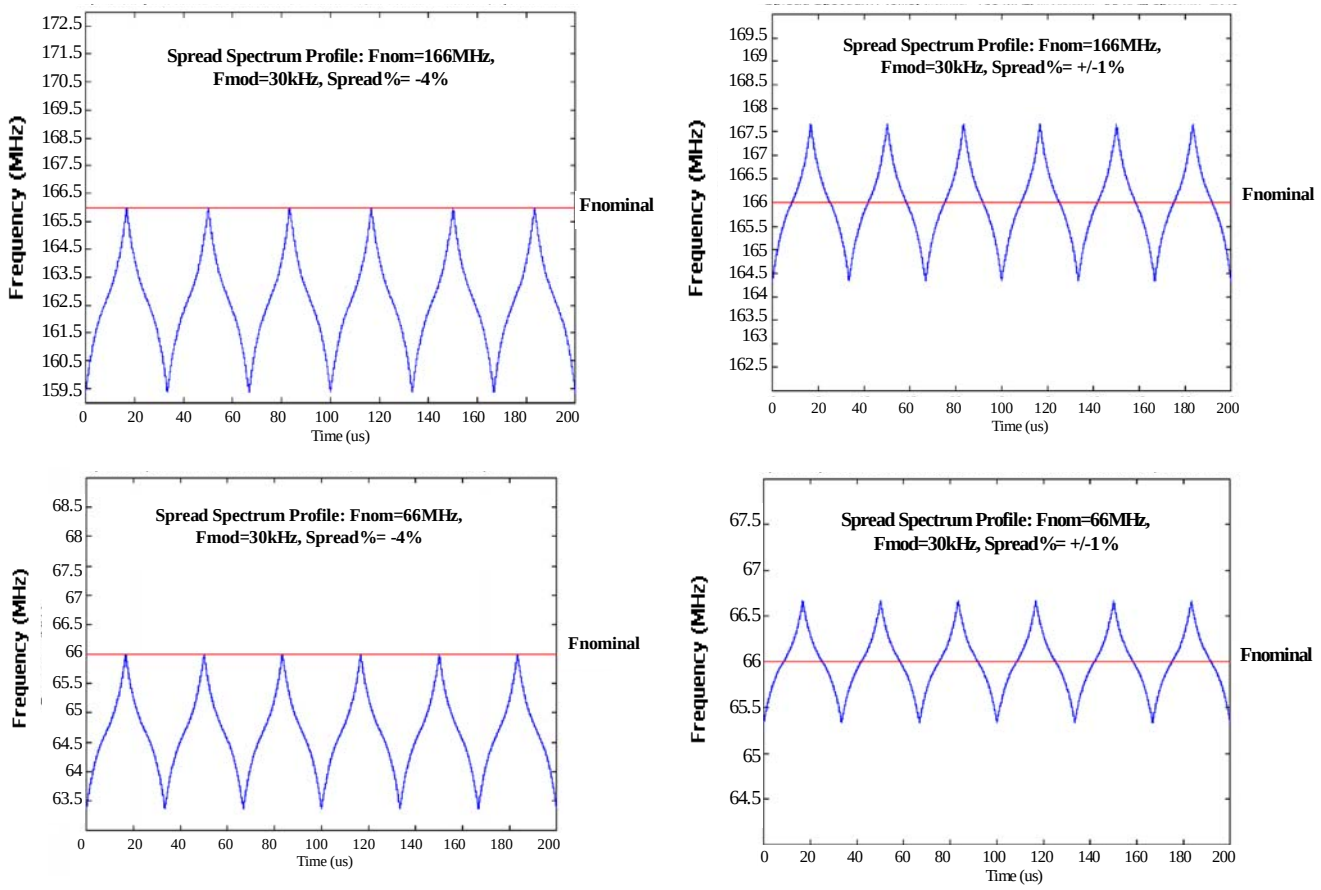


Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 4. Output Enable/Disable Timing Waveforms



Informational Graphs [4]

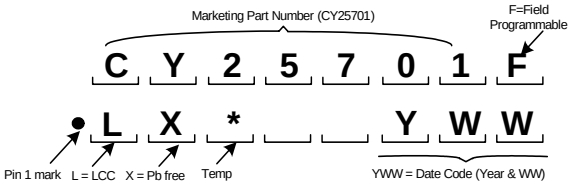


Ordering Information

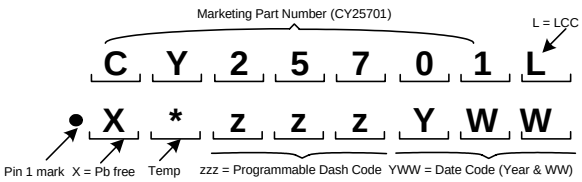
Part Number	Package Description	Product Flow
Lead-free (Pb-free)		
CY25701FLXCT[5]	4-Lead Ceramic LCC SMD -Tape and Reel	Commercial, –20° to 70°C
CY25701FLXIT[5]	4-Lead Ceramic LCC SMD -Tape and Reel	Industrial, –40° to 85°C
CY25701LXCZZZT[6]	4-Lead Ceramic LCC SMD -Tape and Reel	Commercial, –20° to 70°C
CY25701LXIZZZT[6]	4-Lead Ceramic LCC SMD -Tape and Reel	Industrial, –40° to 85°C

Actual Marking[7]

CY25701FLX*



CY25701LX*

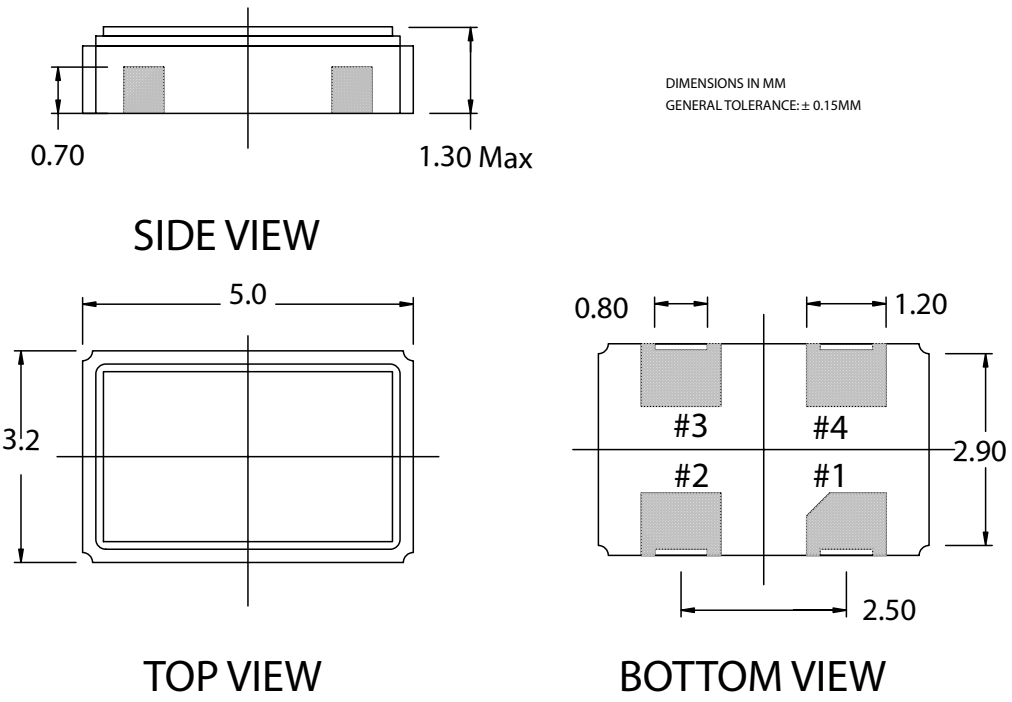


Notes

4. The “Informational Graphs” are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on pages 4 and 5 for device specifications.
5. “FLX” suffix is used for products programmed in field by Cypress Distributors.
6. “ZZZ” denotes the assigned product dash number. This number will be assigned by factory after the output frequency and spread percent programming data is received from the customer.
7. Temp can be C (Com’l) or I (Industrial).

Package Drawings and Dimensions

4-Lead (5.0x3.2mm) Ceramic LCC LZ04A



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Document History Page

Document Title: CY25701 Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No-Spread Spectrum (XO) Option Document Number: 001-07313				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	442944	See ECN	RGL	New data sheet
*A	487736	See ECN	KKVTMP	Added Industrial temp