Freescale Semiconductor
Technical Data

Document Number: MRF7S21150H
Rev. 0, 11/2007

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S21150HR3
MRF7S21150HSR3

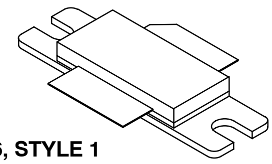
2110-2170 MHz, 44 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

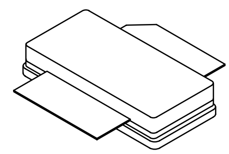
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1350 mA, P_{out} = 44 Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 17.5 dB
  - Drain Efficiency — 31%
  - Device Output Signal PAR — 6.1 dB @ 0.01% Probability on CCDF
  - ACPR @ 5 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz, 150 Watts CW Peak Tuned Output Power
- P_{out} @ 1 dB Compression Point ≥ 150 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465-06, STYLE 1
NI-780
MRF7S21150HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S21150HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 147 W CW Case Temperature 75°C, 45 W CW	$R_{\theta JC}$	 0.33 0.37	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	3A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 348 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1350 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1350 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.5	5.4	6.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.9	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	590	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	320	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, P_{out} = 44 W Avg., f = 2112.5 MHz and f = 2167.5 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

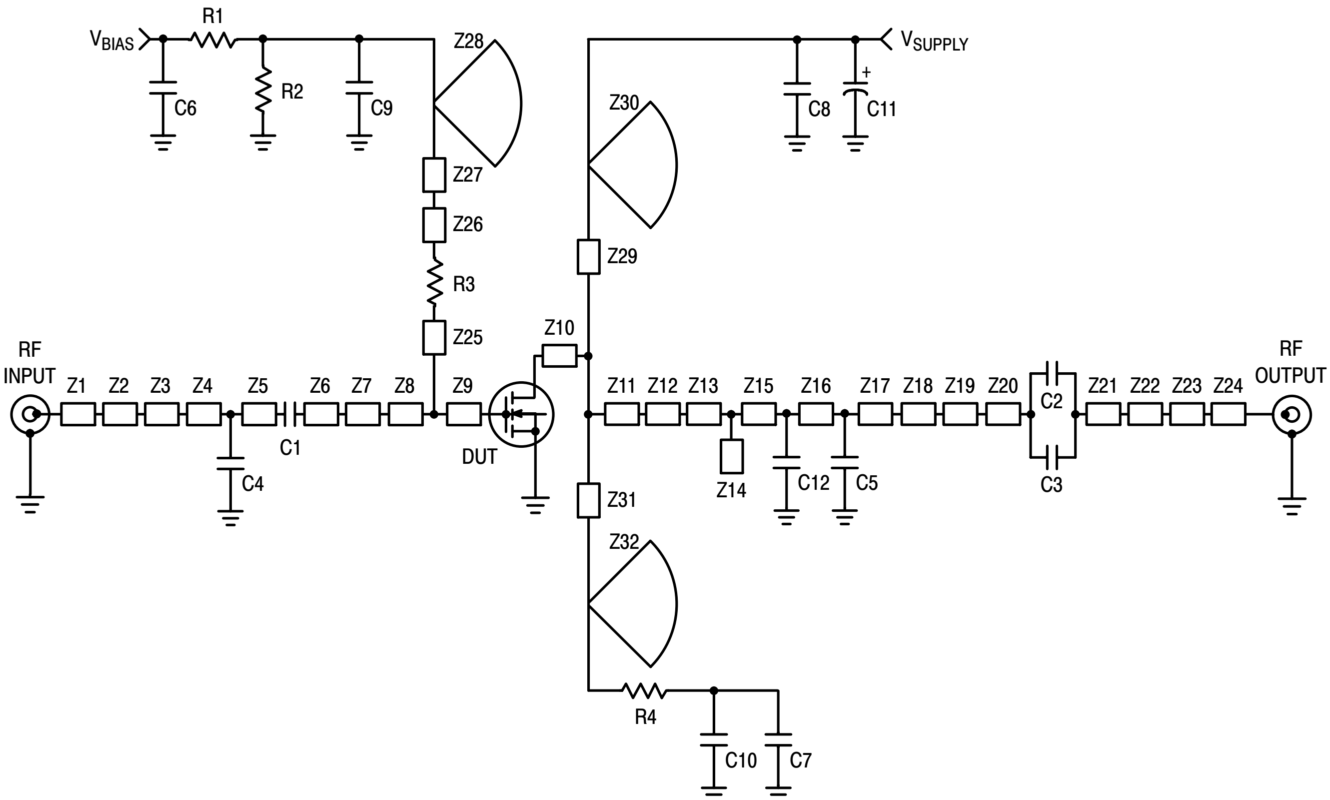
Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	16.5	17.5	19.5	dB
Drain Efficiency	η_D	29	31	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37	-35	dBc
Input Return Loss	IRL	—	-15	-9	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, 2110-2170 MHz Bandwidth					
Video Bandwidth @ 120 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	10	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 44 W Avg.	G_F	—	0.418	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 150 W CW	Φ	—	36.5	—	°
Average Group Delay @ P_{out} = 150 W CW, f = 2140 MHz	Delay	—	2.82	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 150 W CW, f = 2140 MHz, Six Sigma Window	ΔΦ	—	1.45	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.007	—	dBm/°C



Z1	0.980″ x 0.138″ Microstrip	Z12	0.178″ x 0.067″ Microstrip	Z24	0.096″ x 0.138″ Microstrip
Z2	0.461″ x 0.066″ Microstrip	Z13	0.039″ x 0.095″ Microstrip	Z25	0.335″ x 0.066″ Microstrip
Z3	0.534″ x 0.458″ Microstrip	Z14	0.079″ x 0.060″ Microstrip	Z26	0.069″ x 0.080″ Microstrip
Z4*	0.138″ x 0.126″ Microstrip	Z15*	0.168″ x 0.095″ Microstrip	Z27	0.466″ x 0.040″ Microstrip
Z5*	0.536″ x 0.126″ Microstrip	Z16*	0.113″ x 0.095″ Microstrip	Z28	R = 0.526″ α = 60° Microstrip Butterfly
Z6	0.147″ x 0.126″ Microstrip	Z17*	0.128″ x 0.095″ Microstrip	Z29, Z31	0.825″ x 0.066″ Microstrip
Z7	0.060″ x 0.513″ Microstrip	Z18	0.079″ x 0.215″ Microstrip	Z30, Z32	R = 0.526″ α = 60° Microstrip Butterfly
Z8	0.151″ x 0.630″ Microstrip	Z19	0.020″ x 0.095″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z9	0.112″ x 0.630″ Microstrip	Z20, Z21	0.070″ x 0.215″ Microstrip		
Z10	0.337″ x 0.957″ Microstrip	Z22	0.392″ x 0.067″ Microstrip		
Z11	0.176″ x 0.957″ Microstrip	Z23	0.370″ x 0.089″ Microstrip		

* Variable for tuning

Figure 1. MRF7S21150HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S21150HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
C2, C3	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4, C12	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C5	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C6, C7, C8	10 μF Chip Capacitors	C5750X5R1H106M	TDK
C9, C10	100 nF Chip Capacitors	C1206C104K2RAC	Kemet
C11	220 μF, 63 V Electrolytic Capacitor, Axial	222212018221	Vishay BC Components
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
R4	2.2 Ω, 1/4 W Chip Resistor	CRCW12062R20FKEA	Vishay

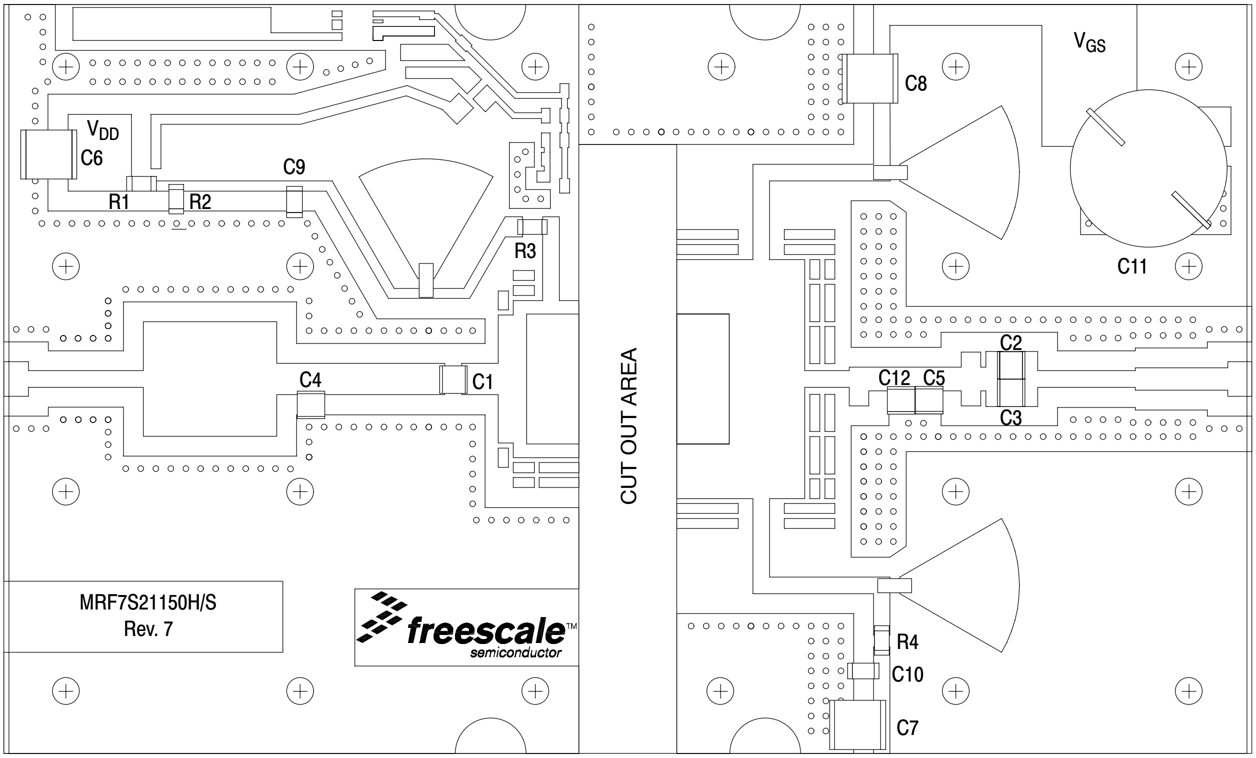


Figure 2. MRF7S21150HR3(HSR3) Test Circuit Component Layout

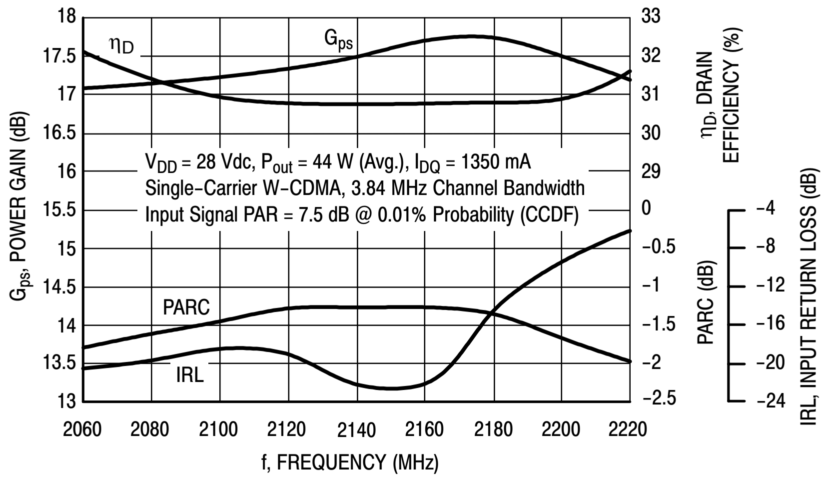


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 44 Watts Avg.

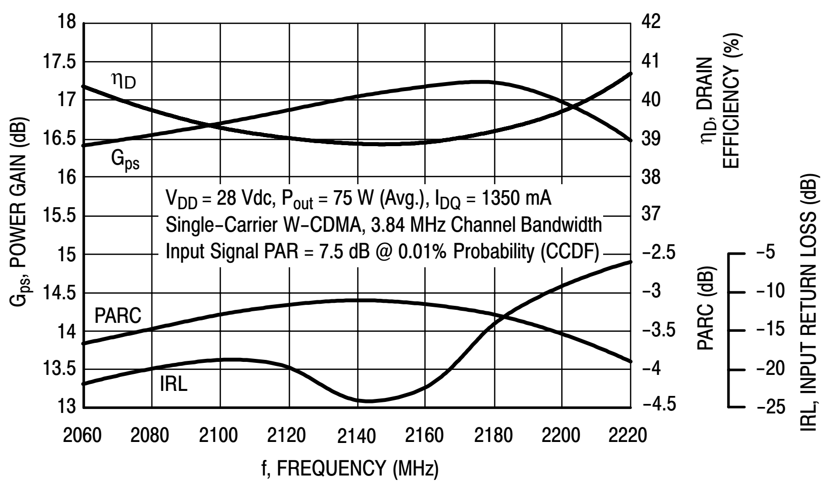


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 75 Watts Avg.

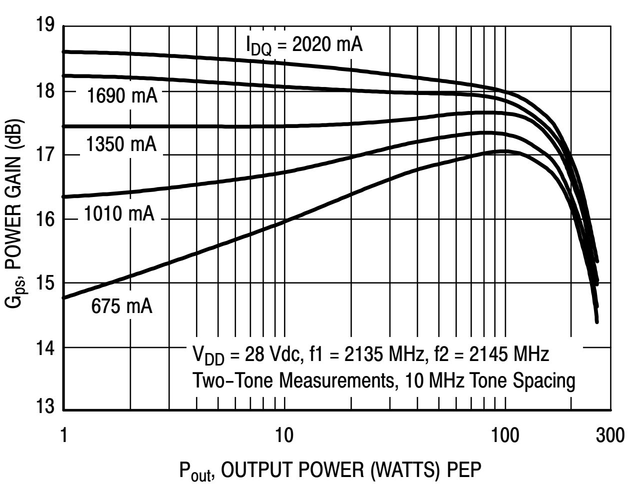


Figure 5. Two-Tone Power Gain versus Output Power

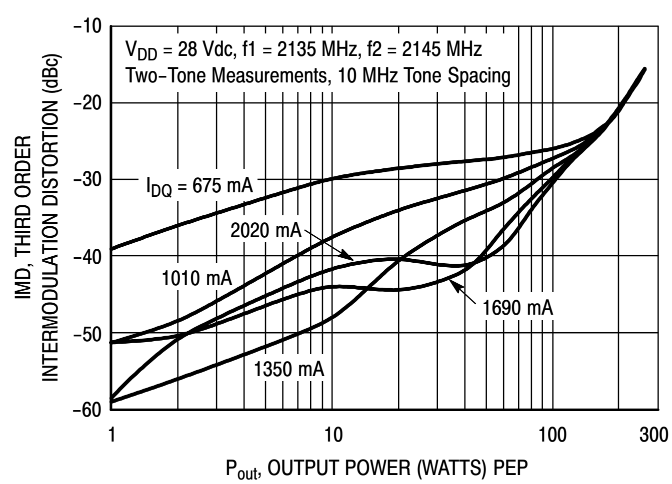


Figure 6. Third Order Intermodulation Distortion versus Output Power

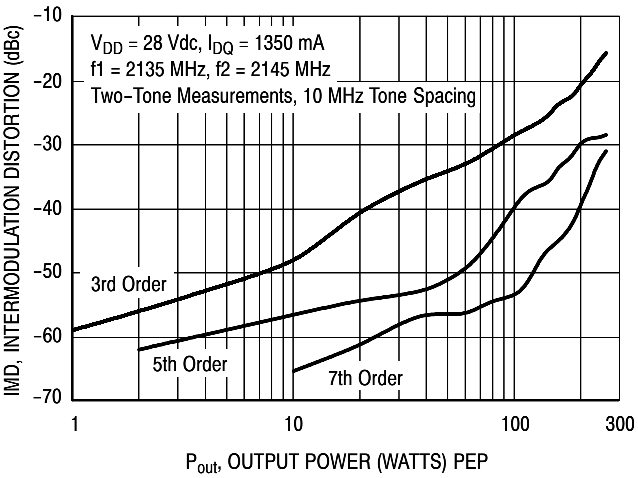


Figure 7. Intermodulation Distortion Products versus Output Power

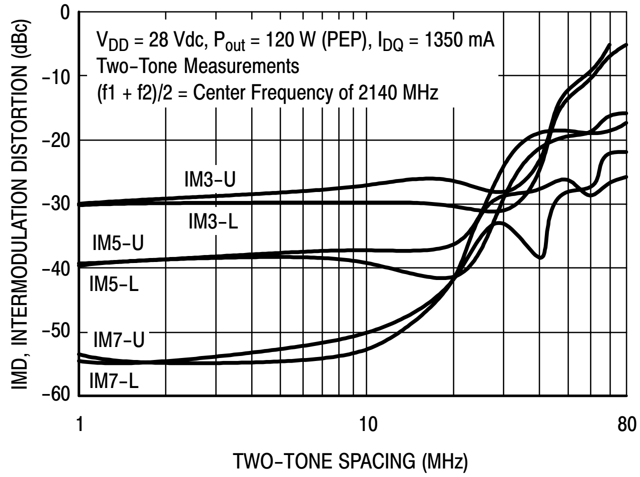


Figure 8. Intermodulation Distortion Products versus Tone Spacing

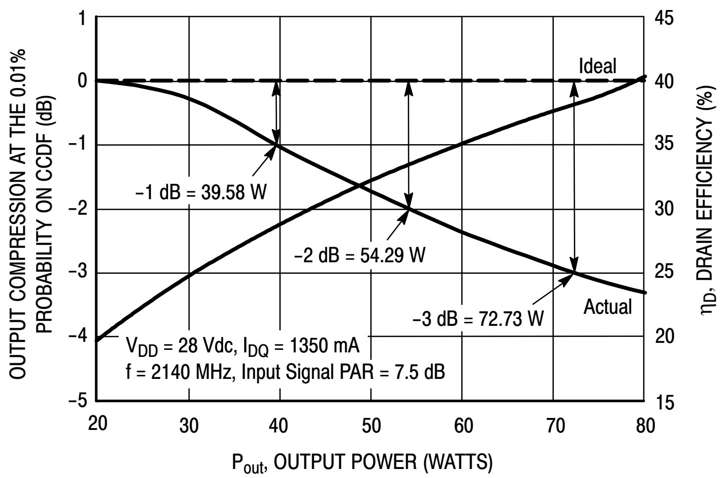


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

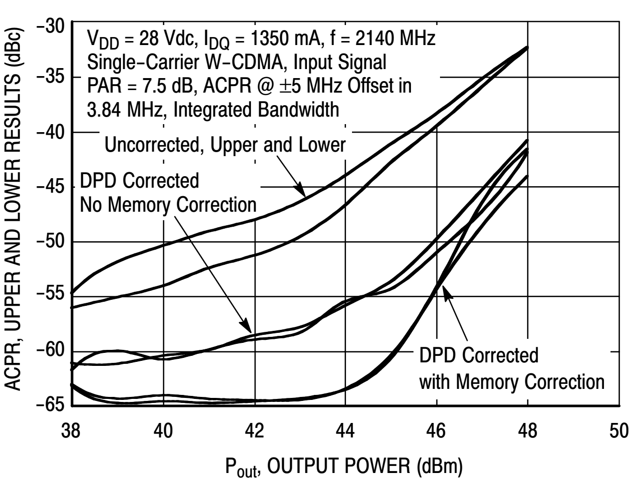


Figure 10. Digital Predistortion Correction versus ACPR and Output Power

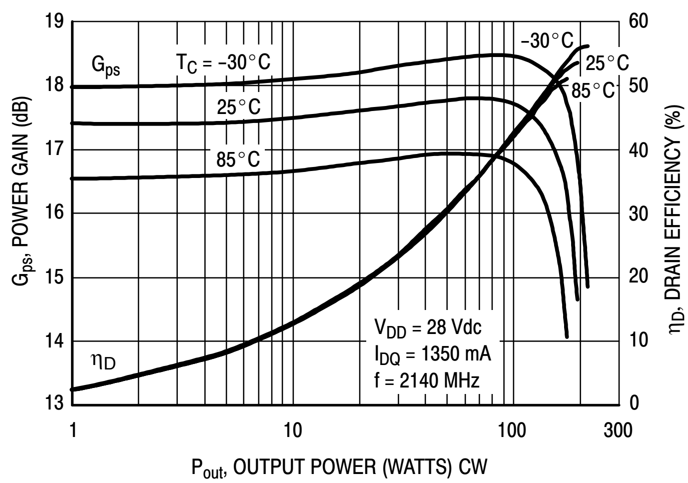


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

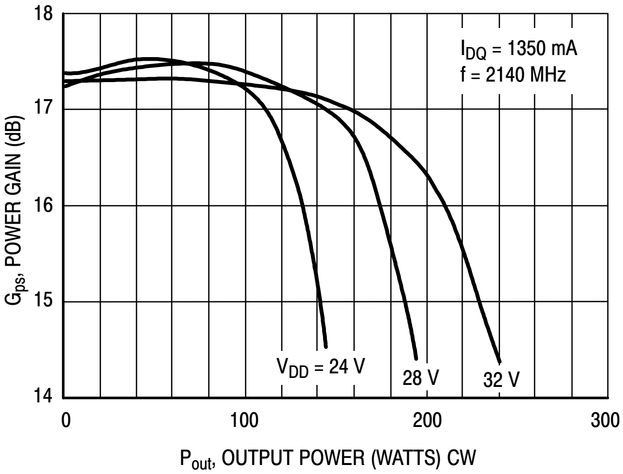
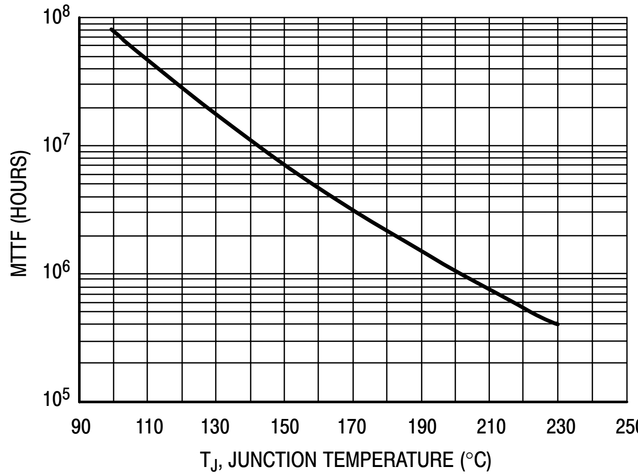


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 44 W Avg., and η_D = 31%.

MTTF calculator available at http:/www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

W-CDMA TEST SIGNAL

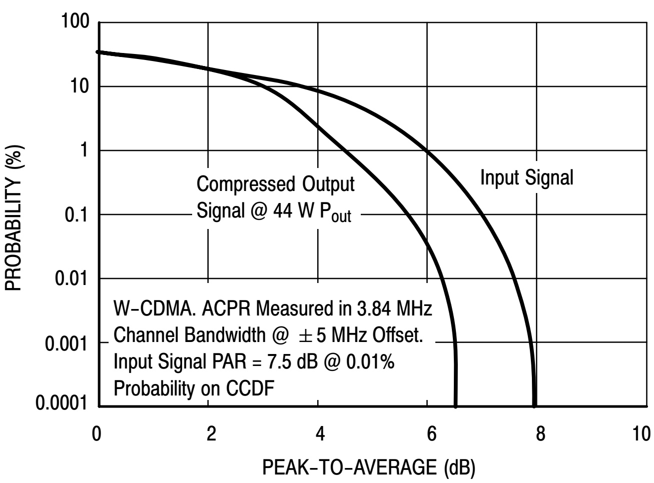


Figure 14. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

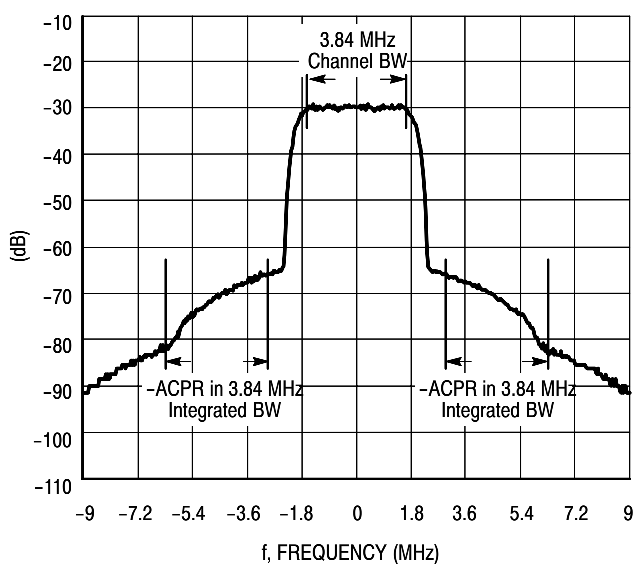
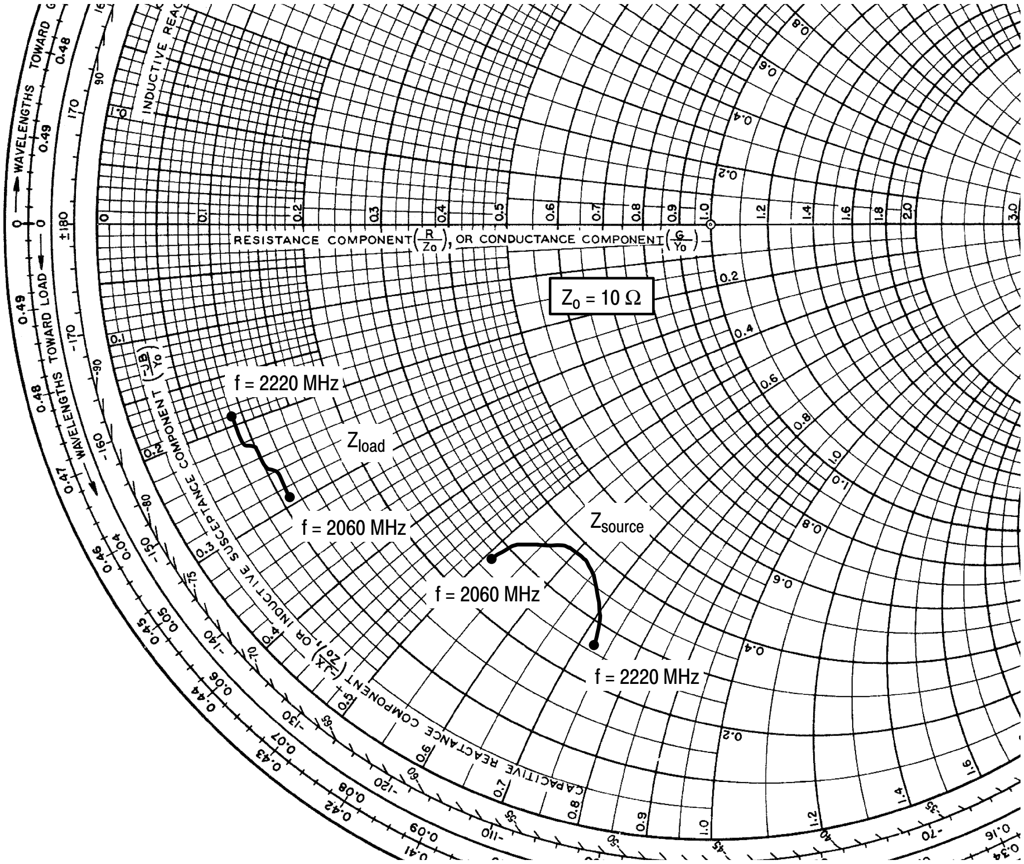


Figure 15. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, P_{out} = 44 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	2.72 - j5.08	1.14 - j2.89
2080	3.10 - j5.17	1.11 - j2.75
2100	3.43 - j5.39	1.08 - j2.62
2120	3.66 - j5.74	1.04 - j2.50
2140	3.72 - j6.17	1.00 - j2.39
2160	3.59 - j6.59	0.96 - j2.28
2180	3.33 - j6.91	0.93 - j2.17
2200	2.98 - j7.10	0.89 - j2.05
2220	2.62 - j7.17	0.86 - j1.93

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

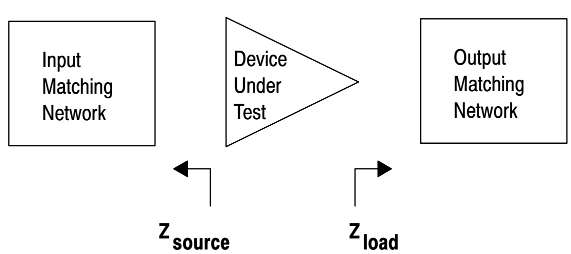
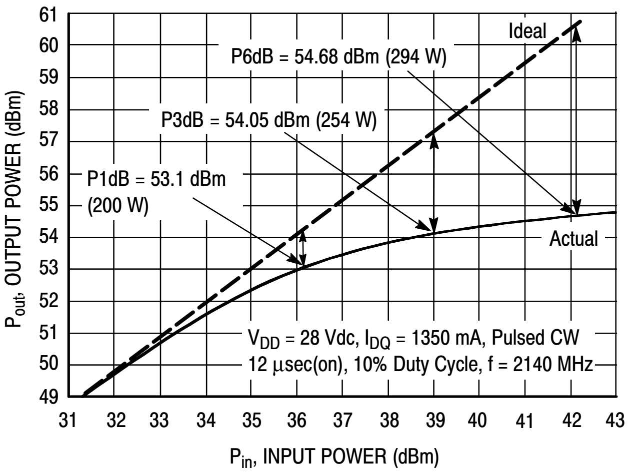


Figure 16. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

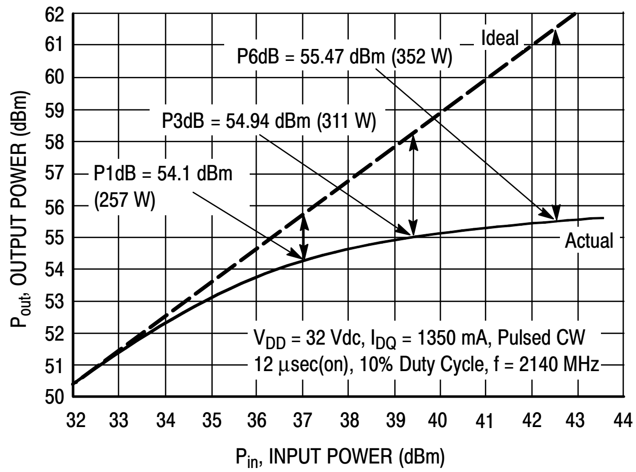


NOTE: Load Pull Test Fixture Tuned for Peak Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	4.66 - j8.05	0.53 - j2.26

Figure 17. Pulsed CW Output Power versus Input Power @ 28 V



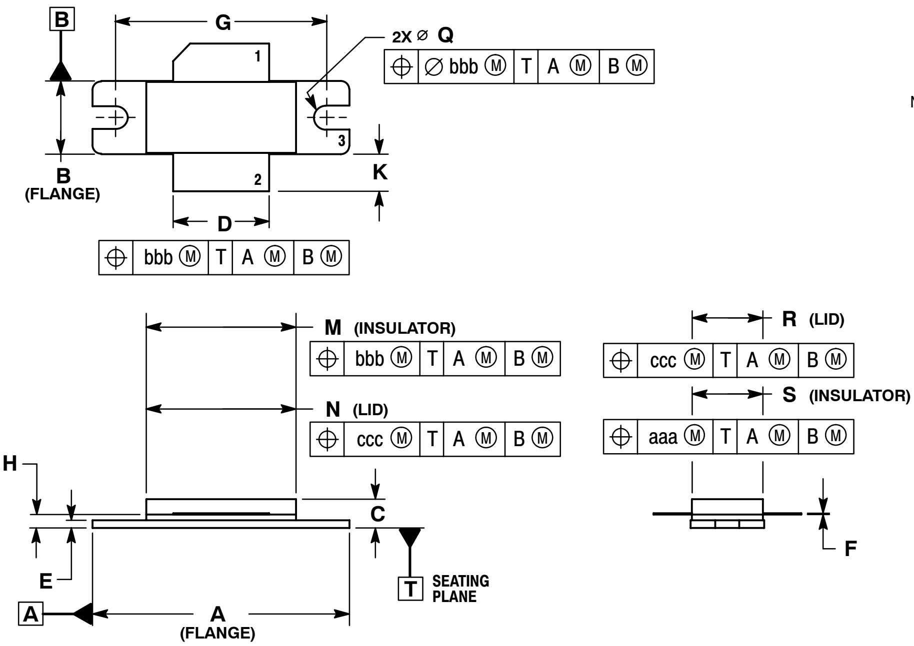
NOTE: Load Pull Test Fixture Tuned for Peak Output Power @ 32 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	4.66 - j8.05	0.64 - j2.17

Figure 18. Pulsed CW Output Power versus Input Power @ 32 V

PACKAGE DIMENSIONS

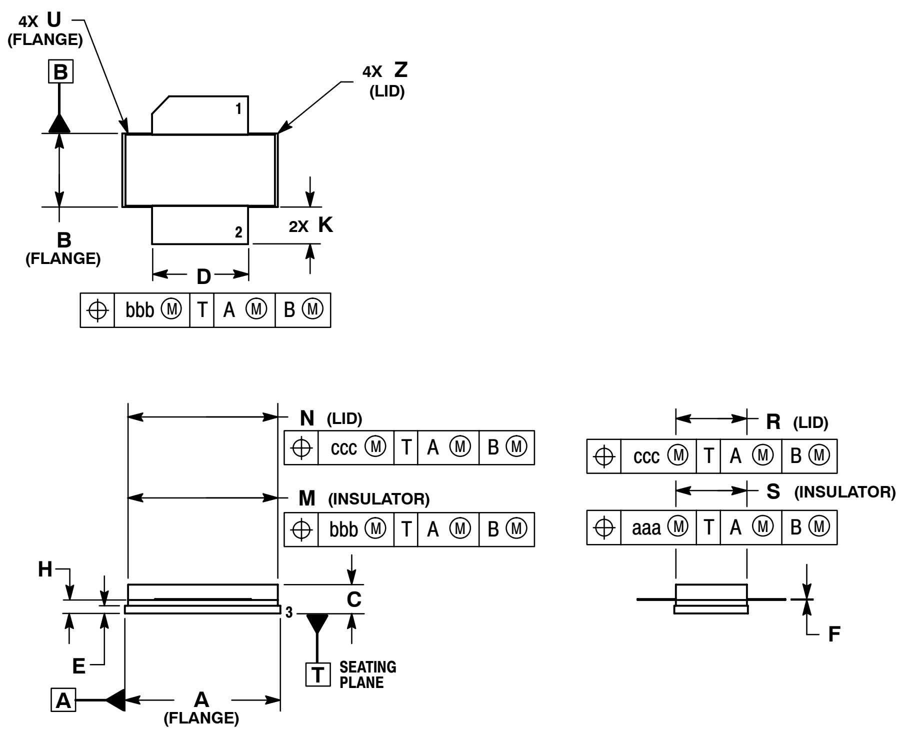


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	⌀.118	⌀.138	⌀3.00	⌀3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465-06
ISSUE G
NI-780
MRF7S21150HR3



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3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF7S21150HSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2007	• Initial Release of Data Sheet

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Document Number: MRF7S21150H
Rev. 0, 11/2007