Managed 10/100Base-TX / FX Media Converter

Features

- A 10/100BASE-TX/ 100BASE-FX converter with a SMI port for management
- Built in a 10/100BASE-TX transceiver
- Built in a PHY for 100BASE-FX
- Built in a 2-port switch
  - Pass all packets without address and CRC check (optional)
  - Supports modified cut-through frame forwarding for low latency
  - Supports pure converter mode data forwarding for extreme low latency
  - Supports flow control for full and half duplex operation
  - Bandwidth control
  - Forward 1600 bytes packet for management
  - Optional forward fragments
- Built in 128Kb RAM for data buffer
- Supports 3.3v I/O tolerance SMI (MDC, MDIO) and MII registers for management
  - Configure local and remote IP113F through local SMI
  - Monitor local and remote IP113F through local SMI
  - Configure/ monitor TP port support (auto-negotiation or force 10M/100M, full/half)
  - Configure/ monitor flow control, bandwidth
  - Supports loop back test (In-band or out-band, auto or program)
  - The maintenance frame is compatible to TS-1000 standard (the Telecommunication Technology Committee, TTC)
- Supports Statistic Counters
- Supports auto MDI-MDIX function
- Supports link fault pass through function
- Supports far end fault function
- LED display for link/activity, full/half, 10/100
- Built in a watchdog timer to monitor internal switch error
- Supports EEPROM Configuration
- 0.25u CMOS technology
- Single 2.5V power supply
- 48-pin LQFP package

General Description

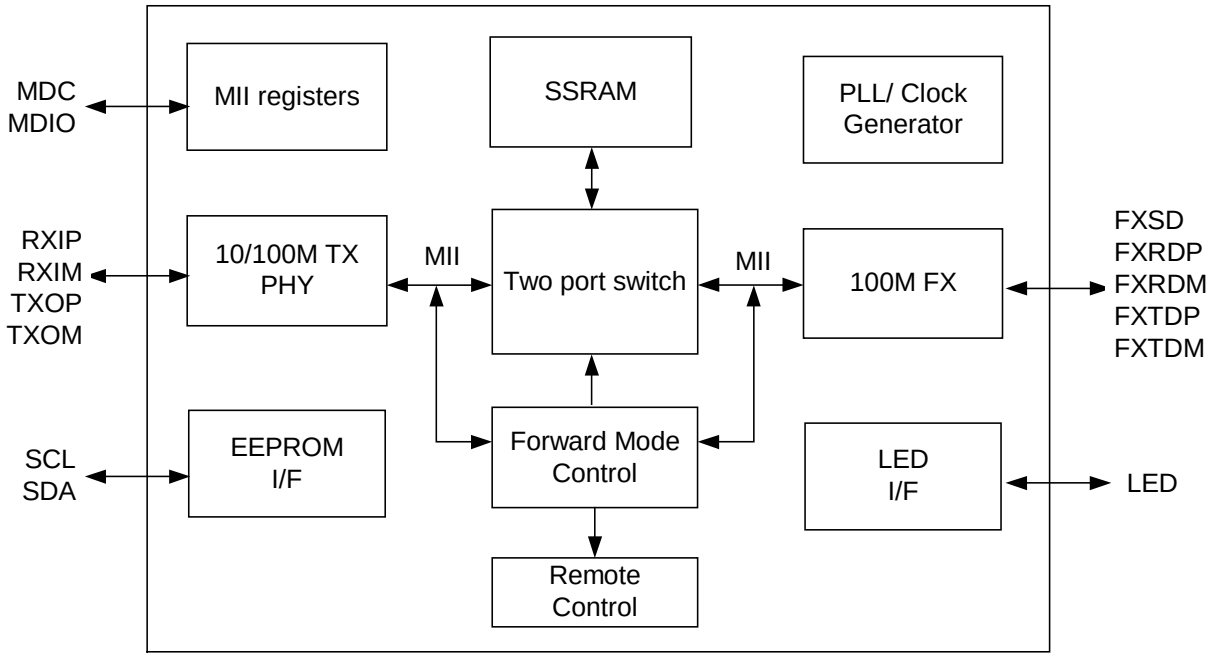
IP113F can be a 10/100BASE-TX to 100BASE-FX converter or a 100BASE-FX to 100BASE-FX repeater with an SMI port for management. It consists of a 2-port switch controller, a fast Ethernet transceiver and a PHY for 100BASE-FX. The transceivers in IP113F are designed in DSP approach with advance 0.25um technology; this results in high noise immunity and robust performance.

IP113F not only supports store and forward mode, it also supports modified cut through mode and pure converter mode for low latency data forwarding. IP113F can transmit packet(s) up to 1600 bytes to meet requirement of extra long packets.

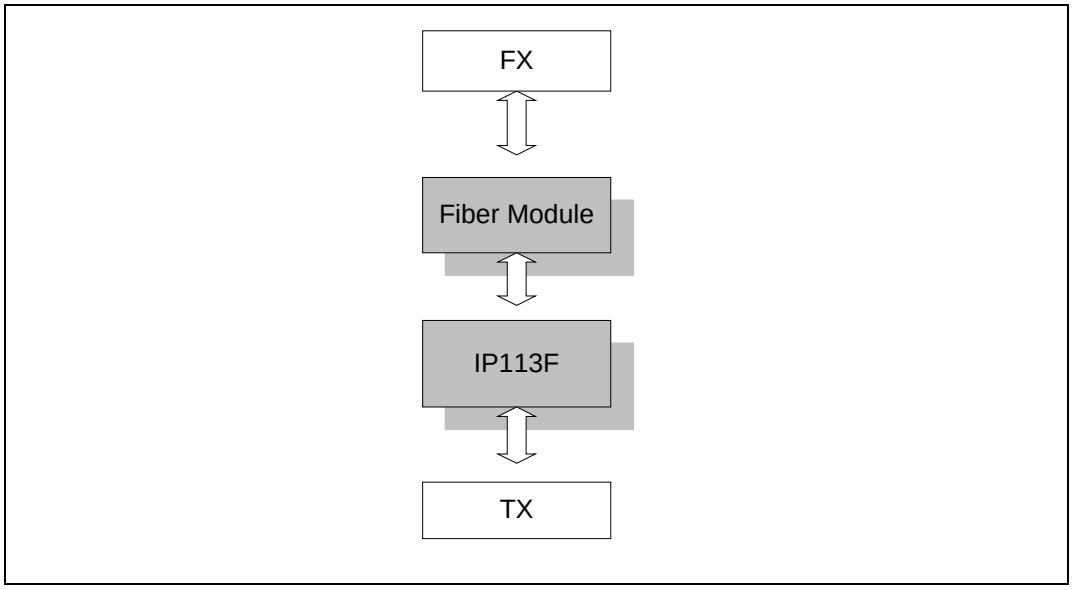
IP113F supports remote management function. IP113F supports remote access functions and it also supports remote monitor and loop back test function defined in TS-1000 spec. Local IP113F can access the MII register of remote IP113F by programming local IP113F's MII registers via SMI connection. IP113F implements the management function using the maintenance frame defined in TS-1000 spec.

IP113F supports IEEE802.3x, collision base backpressure, and various LED functions, etc. These functions can be configured to fit the different requirements by feeding operation parameters via EEPROM interface or pull up/down resistors on specified pins.

Block Diagram

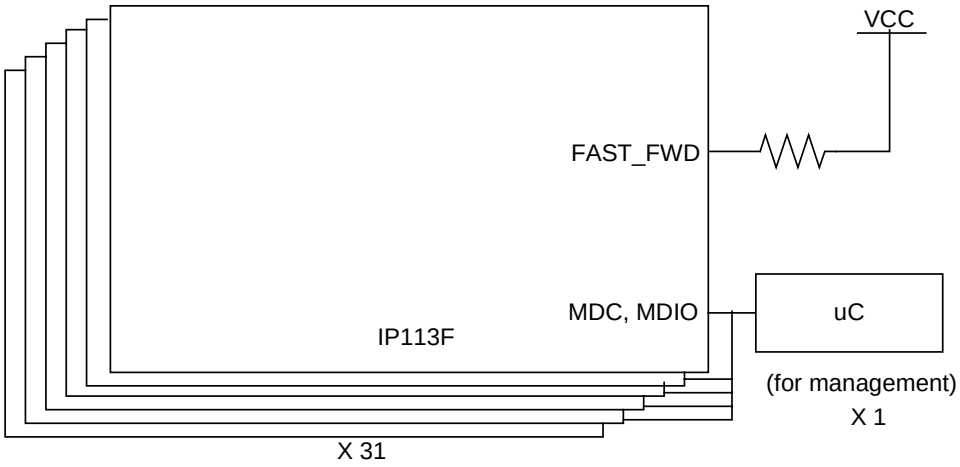


Application Diagram

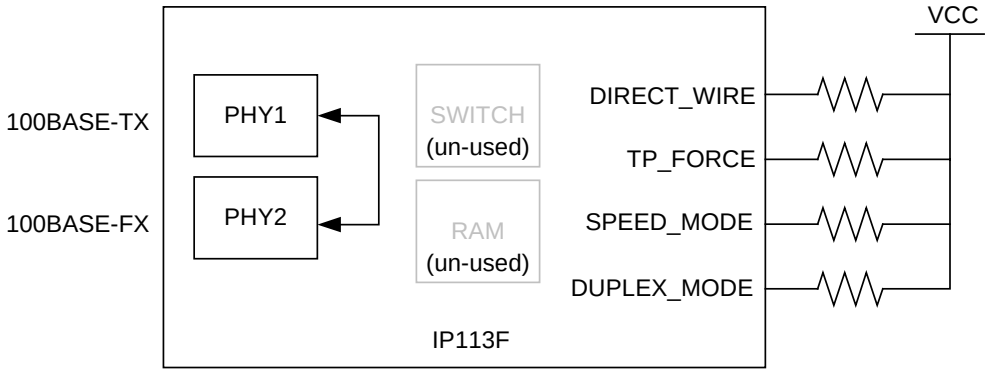


Applications

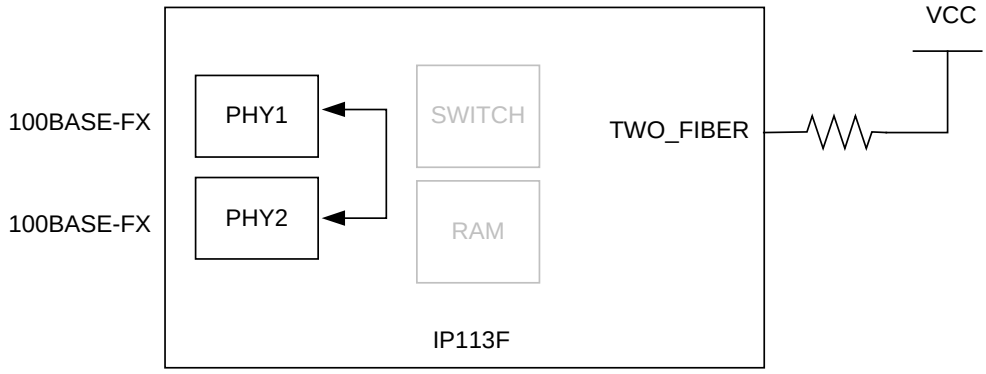
Managed converter (up to 31 pieces of IP113F in a chassis)



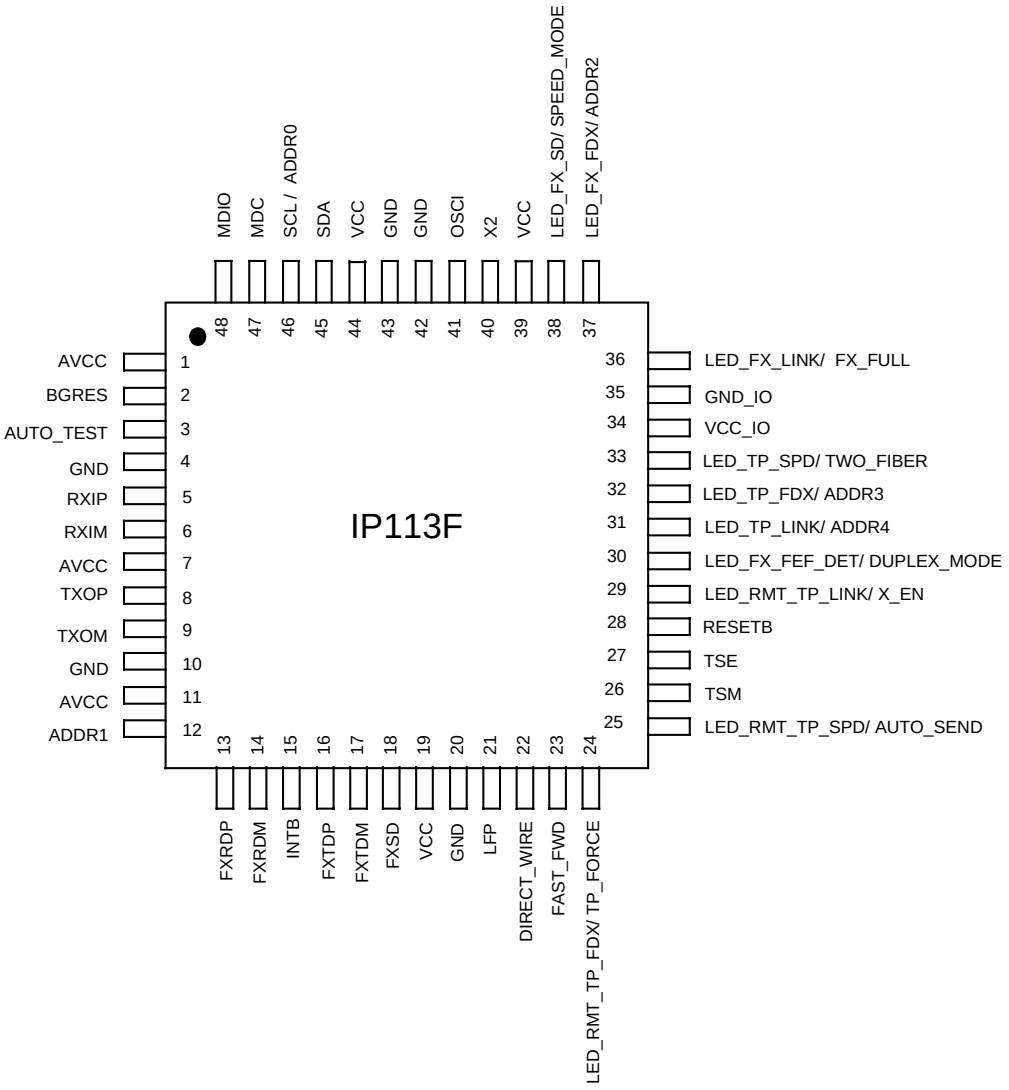
Un-managed converter



Fiber Repeater



PIN Diagram



1. PIN Description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with pull-hi resistor
IPH	Input pin with pull-low resistor

Pin no.	Label	Type	Description
Transceiver			
5, 6	RXIP, RXIM	I	**TP receive**
8, 9	TXOP, TXOM	O	**TP transmit**
2	BGRES	O	**Band gap resistor** It is connected to GND through a 6.19k (1%) resistor in application circuit.
18	FXSD	I	**100Base-FX signal detect** Fiber signal detect. It is an input signal from fiber MAU. Fiber signal detect is active if the voltage on FXSD is higher than the threshold voltage, which is 1.35v ±5% when VCC is equal to 2.5v.
13, 14	FXRDP, FXRDM	I	**Fiber receiver data pair**
16, 17	FXTDP, FXTDM	O	**Fiber transmit data pair**

1. PIN Description (continued)

Pin no.	Label	Type	Description
LED pins			
31	LED_TP_LINK	O	**TP port link LED** On: link ok, Off: link fail, Flash: link ok & activity (Flash: on for 20ms and off for 80ms)
33	LED_TP_SPD	O	**TP port speed LED** On: 100M, Off: 10M
32	LED_TP_FDX	O	**TP port full duplex LED** On: full, Off: half, Flash: half & collision happens (Flash: on for 20ms and off for 80ms)
36	LED_FX_LINK	O	**Fiber port link LED** On: link ok, Off: link fail, Flash: link ok & activity (Flash: on for 20ms and off for 80ms)
37	LED_FX_FDX	O	**Fiber port full duplex LED** On: full, Off: half, Flash: half & collision happens (Flash: on for 20ms and off for 80ms)
38	LED_FX_SD	O	**Fiber port signal detect** On: fiber signal detected, Off: fiber unplugged
30	LED_FX_FEF_DET	O	**Far end fault pattern received** For End Fault Patterns Receive LED On: 80ms, LED Off: 20ms For End Fault Pattern not Receive LED always Off
29	LED_RMT_TP_LINK	O	**LED for link status of TP port of remote IP113F** When AUTO_TEST is logic low, On: link ok, Off: link fail When AUTO_TEST is pulled high, it is always flash in a period of 100ms (On: 80ms, Off: 20ms)
25	LED_RMP_TP_SPD	O	**LED for speed of TP port of remote IP113F** When AUTO_TEST is logic low, On: 100M, Off: 10M When AUTO_TEST is pulled high, On: loop back test complete, Off: during loop back test
24	LED_RMT_TP_FDX	O	**LED for full duplex of TP port of remote IP113F** When AUTO_TEST is logic low, On: full, Off: half When AUTO_TEST is pulled high, On: loop back test ok, Off: loop back test fail

Note: The output of LED pin is logic low when the LED is on.

1. PIN Description (continued)

Pin no.	Label	Type	Description
LED pins used as initial setting mode during reset			
29	X_EN	IPH	**IEEE 802.3X enable on TP port and fiber port** 1: enable (default), 0: disable
24	TP_FORCE	IPL	**Local TP port auto negotiation enable** 1: TP port supports auto-negotiation with limited capability defined in SPEED_MODE and DUPLEX_MODE. 0: TP port supports auto-negotiation with 10M/100M, full/ half capability (default) The default value may be updated by either programming EEPROM register 3.5 or MII register 20.13.
38	SPEED_MODE	IPH	**Local TP port speed** 1: TP port has the 100Mb speed ability 0: TP port has the 10Mb speed ability only It is valid only if TP_FORCE is enabled.
30	DUPLEX_MODE	IPH	**Local TP port duplex** 1: TP port has the Full duplex ability 0: TP port has the Half duplex ability only It is valid only if TP_FORCE is enabled.
25	AUTO_SEND	IPL	**Auto send the status to the remote IP113F** 1: enable 0: disable (default)
36	FX_FULL	IPH	**Set the duplex of fiber port** 1: full duplex (default) 0: half duplex
3	AUTO_TEST	IPL	**Auto loop back test** 1: enable When IP113F detects a low-to-high transition on this pin, it will perform loop back test for once. 0: disable (default)

1. PIN Description (continued)

Pin no.	Label	Type	Description
LED pins used as initial setting mode during reset			
33	TWO_FIBER	IPL	**Two fiber ports** 1: IP113F supports two-fiber ports mode. Both port 1 and port 2 are fiber ports. RXIP and RXIM are used as FXRDP and FXRDM for the second fiber port. TXOP and TXOM are used as FXTDP and FXTDM for the second fiber port. A special requirement for the fiber MAU of port1 in this application is that the output of FXRDP and FXRDM should have no incoming signals when fiber is unplugged. For some fiber MAUs, there are amplified noisy signals on FXRDP and FXRDM when fiber is unplugged. These amplified noisy signals, which include coupled idle patterns from FXTDP and FXTDM will cause the LEDs of port1 malfunction Generally, a 3.3-V small form factor type fiber MAUs (e.g. Agilent HFBR-5903) can meet this special requirement, but 5-V duplex-SC and -ST type fiber MAUs cannot. Port2 is not limited by this special requirement. 0: IP113F supports one fiber port and one TP port. Port 1 is a TP port and port 2 is a fiber port.

1. PIN Description (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">MC operation mode</td></tr>
<tr><td>21</td><td>LFP</td><td>IPL</td><td>Link fault pass through (LFP)
1: enable
Link status of one port is forwarded to the other port.
0: disable (default)</td></tr>
<tr><td>22
23</td><td>DIRECT_WIRE
FAST_FWD</td><td>IPL</td><td>
<table>
<tr><th>DIRECT_WIRE</th><th>FAST_FWD</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Store and forward switch mode (default)</td></tr>
<tr><td>0</td><td>1</td><td>Modified cut-through switch mode</td></tr>
<tr><td>1</td><td>0</td><td>Converter mode</td></tr>
<tr><td>1</td><td>1</td><td>Converter mode with auto-change-forward function</td></tr>
</table>
Store and forward switch mode:
IP113F begins to forward a frame at the end of receiving a frame completely.

Modified cut-through switch mode:
IP113F begins to forward a frame after the first 64 bytes data received. TP port should be forced at 100M at this mode.

Converter mode:
Incoming frames are not buffered in IP113F to achieve the min latency. TP port should be forced at 100M at this mode.

Converter mode with auto-change-forward function:
IP113F will change forward mode itself if it detects the speed is different in TP port and FX port.

In converter mode, IP113F forwards IEEE802.3x pause frame directly. In the other modes, IP113F doesn’t forward IEEE802.3x pause frame directly, it sends out pause frame when its internal buffer is full.</td></tr>
</table>

1. PIN Description (continued)

Pin no.	Label	Type	Description
SMI interface			
47, 48	MDC, MDIO	I, IO	**SMI interface** The external MAC device uses the interface to program IP113F. MDIO is an open drain.
31, 32, 37, 12, 46	ADDR[4:0]	IPL	**PHY address** The external MAC device uses the address to identify each IP113F in a chassis. IP113F also uses ADDR[2:0] as EEPROM address A[2:0] to read EEPROM.

Pin no.	Label	Type	Description
EEPROM interface			
45, 46	SDA, SCL	IPH, O	**EEPROM interface**

Pin no.	Label	Type	Description
Misc.			
28	RESETB	I	**Reset** It is low active.
41, 40	OSCI, X2	I, O	**Crystal pins** OSCI and X2 are connected to a 25Mhz crystal. If a 25MHz oscillator is used, OSCI is connected to the oscillator's output and X2 should be left open.
26, 27	TSM, TSE	IPL	**Scan pins** These two pins should be left open or connected to ground for normal operation.
15	INTB	O	**Interrupt** 0: an interrupt happens. Its output is low. 1: no interrupt. Its output is high impedance and it needs an external pull up resistor.

2. Functional Description

Data forwarding

IP113F supports three types of data forwarding mode, store & forward mode, modified cut-through mode and pure converter mode. It can forward a frame despite of its address and CRC error. IP113F begins to forward the received data when it receives the frame completely. The latency depends on the packet length.

Modified cut-through mode

IP113F begins to forward the received data when it receives the first 64 bytes of the frame. The latency is about 512 bits time width. The maximum packet length is up to1600 bytes in this mode. Please refer to pin description of FAST_FWD for configuration information.

Pure converter mode

IP113F operates with the minimum latency in this mode. The transmission flow does not wait until entire frame is ready, but instead it forwards the received data immediately after the data being received. Both transceivers are interconnected via internal MIIs and the internal switch engine and data buffer are not used. TP port should be forced at 100M in this application. The packet length is not limited at this mode. Please refer to pin description of DIRECT_WIRE for configuration information.

Fragment forwarding

IP113F forwards CRC error packets but it will filter fragments when it works in modified cut-through mode. IP113F forwards fragments if user turns on bit 3 of MII register 20.

TP port force mode

The TP port of IP113F can work at auto mode or force mode. The following table shows all of the combination of its TP port.

TP_FORCE	SPEED_MODE	DUPLEX_MODE	IP113F's capability
0	1	1	100/10M, Full/Half with auto-negotiation
0	1	0	100/10M, Half with auto-negotiation
0	0	1	10M, Full/Half with auto-negotiation
0	0	0	10M, Half with auto-negotiation
1	1	1	100M, Full with auto-negotiation
1	1	0	100M, Half with auto-negotiation
1	0	1	10M, Full with auto-negotiation
1	0	0	10M, Half with auto-negotiation

Remote management

IP113F supports remote monitor and configuration function. IP113F implement the function by exchanging maintenance frames on fiber ports between two IP113Fs. The maintenance frames are not forwarded to TP ports. The frame format follows the TS-1000 standard.

Maintenance frame format at MII

TXD0	F0	F4	C0	C4	C8	C12	S0	S4	S8	S12	M0	M4	M8	M12	M16	M20	M24	M28	M32	M36	M40	M44	E0	E4
TXD1	F1	F5	C1	C5	C9	C13	S1	S5	S9	S13	M1	M5	M9	M13	M17	M21	M25	M29	M33	M37	M41	M45	E1	E5
TXD2	F2	F6	C2	C6	C10	C14	S2	S6	S10	S14	M2	M6	M10	M14	M18	M22	M26	M30	M34	M38	M42	M46	E2	E6
TXD3	F3	F7	C3	C7	C11	C15	S3	S7	S11	S15													E3	E7

Bit definition of maintenance frame

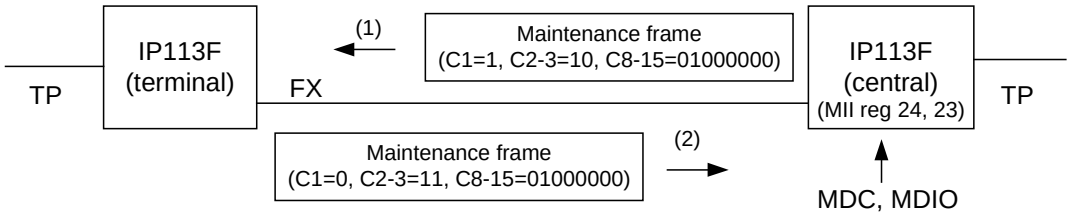
Bit	Item	Description	Note
F7 – F0	Preamble	01010101	Fixed
C0	Discriminator for the maintenance signal	0	Fixed
C1	Direction	0: terminal MC → central MC 1: central MC → terminal MC (MC: media converter)	
C3 – C2	Command	00: Reserved 10: Indication 01: Request 11: Acknowledge	
C7 – C4	Version	0000	Fixed
C15 – C8	Control signal	00 00 00 01 : Loop test starts 00 00 00 00 : Loop test ends 00 00 00 10 : Status notice addr[4:0] RW 11 : IP113F R/W reg.	
S0	Condition of power	0: normal, 1: power off	
S1	Situation of receiving optical power	0: normal, 1: abnormal	
S2	Terminal/ network side link	0: link up, 1: link down If S11="1", S2="X"	
S3	MC (media converter) fails	0: normal, 1: abnormal	
S4	Informing way for optical receiving power off	0: maintenance frame 1: Far end fault indication	
S5	Status indication for loop test	0: normal mode, 1: under loop test	

Bit definition of maintenance frame (continued)

Bit	Item	Description	Note
S6	Information for notice of terminal link status (Available for option B or not)	0: terminal IP113F does not support option B. 1: terminal IP113F supports option B, which can inform speed, duplex, and auto-negotiation in terminal IP113F. If S11 = “1”, S6=”X’	
S8 – S7	Terminal link speed	00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: others It is valid, if S6 = ”1”. If S2 or S11 = “1”, S7, S8 = {X, X}	
S9	Duplex for the terminal side	1: full duplex, 0: half duplex It is valid, if S6 = ”1”. If S6 =“0”, S9=“0”. If {S7, S8} = {1,1}, S9=”X” If S2 or S11 = “1”, S9=”X”	
S10	Auto-negotiation capability for the terminal side	1: available, 0: un-available It is valid, if S6 = ”1”. If S6 =“0”, S10=“0”. If {S7, S8} = {1,1}, S10=”X” If S11 = “1”, S10=”X”	
S11	Number of interface in Terminal/ network side	0: one UTP 1: more than one UTP	
S15 – S12	Reserved		
M23 – M0	Vender code	Vender code for TTC standard It is C30900h.	
M47 – M24	Model number	Specified by vender It is 000000h.	
E7 – E0	FCS	CRC – 8 FCS calculation area: C0 - M47	

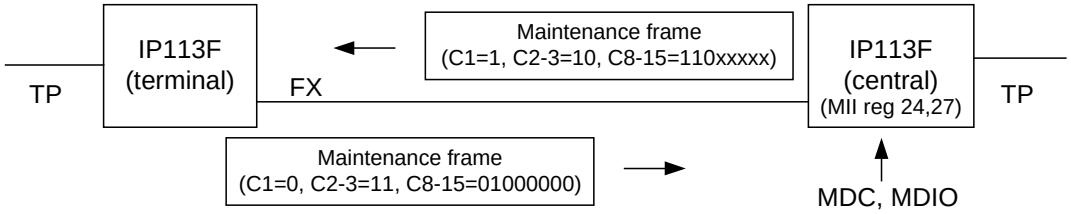
Remote monitor

Refer to the diagram below, users can instruct central IP113F, on the right, to issue a status request frame to get status defined in TS-1000 by programming MII register 24. The terminal IP113F, on the left, receives the status request frame and sends out its current status as a response frame onto the fiber port when it is available. The central IP113F receives the status frame and stores the status of terminal IP113F to its MII register 23. An acknowledge maintenance frame is store to MII register 26~30. The status of terminal IP113F is shown on the LEDs of central IP113F.



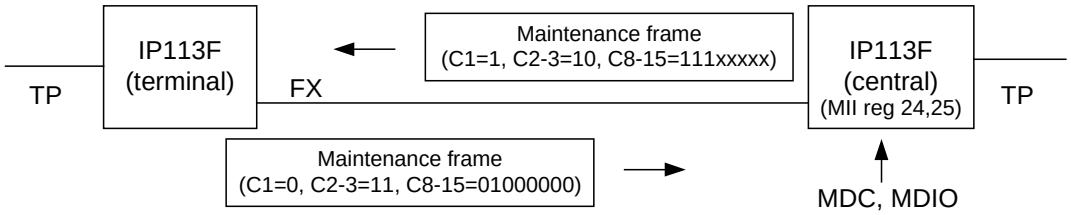
Remote control read

Users can instruct central IP113F to issue a remote control read frame to read the MII register of terminal IP113F by programming MII register 24. The bits [11:7] of the register 24 are filled with the address of register and bits [6:4] of the register 24 are filled with “011”. The terminal IP113F receives the frame and sends out the content of the MII register to central IP113F when it is available. The central IP113F receives the frame and stores the data to MII register 27. An acknowledge maintenance frame is stored to MII register 26~30. The status of terminal IP113F is shown on LED of central IP113F.



Remote control write

Users can instruct central IP113F to issue a configure frame to write the MII register of terminal IP113F by programming MII register 24 and 25. The bits [11:7] of the register 24 are filled with the address of register and bits [6:4] of the register 24 are filled with “111”. MII register 25 defines the data. The terminal IP113F receives the configure frame, configures itself according to the content of the frame and sends out its current status as a response frame onto the fiber port when it is available. The status of terminal IP113F is shown on LED of central IP113F.



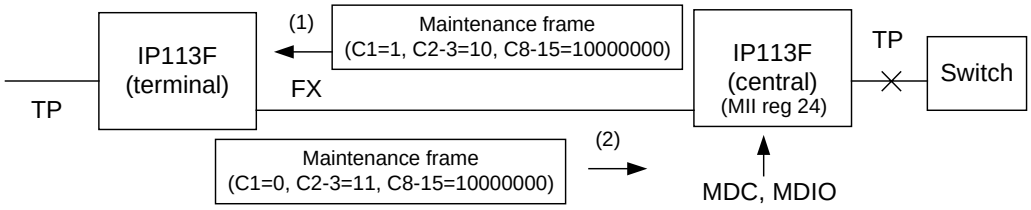
Loop back test

IP113F supports two kind of loop back test function, in-band loop back test and out-band loop back test.

Out-band loop back test

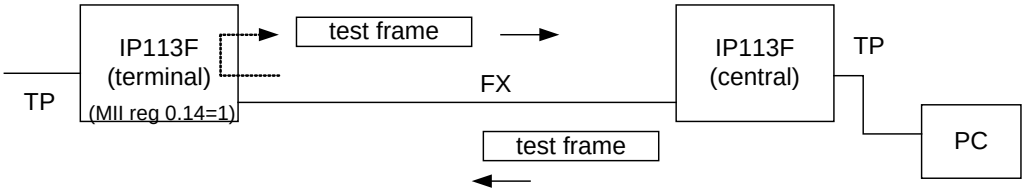
Users can instruct central IP113F to issue a maintenance frame onto the fiber port by programming MII register 24 to request a loop back test. Central IP113F does not generate test frames and users need an external packet source from PC.

1. Disconnect switch port and instruct the terminal IP113F to perform loop back and disable terminal T2 timer by programming central IP113F through SMI

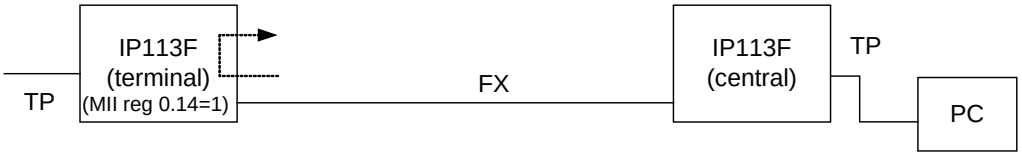


2. Terminal IP113F runs at loop back mode

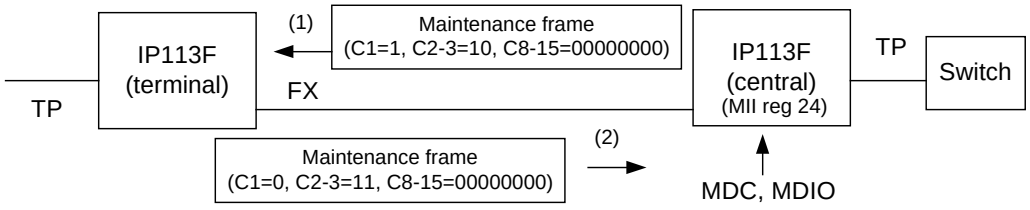
3. PC forces test frames to central IP113F and terminal IP113F loops back the frames.



4. PC reports the loop back test result after sending all test frames.



5. Reconnect switch and instruct the central IP113F to end loop back test and enable T2 timer.

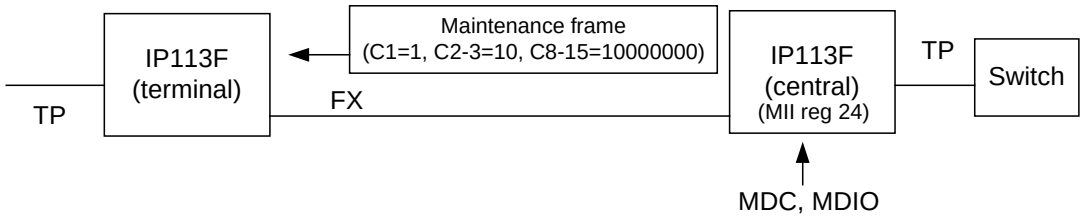


Loop back test (continued)

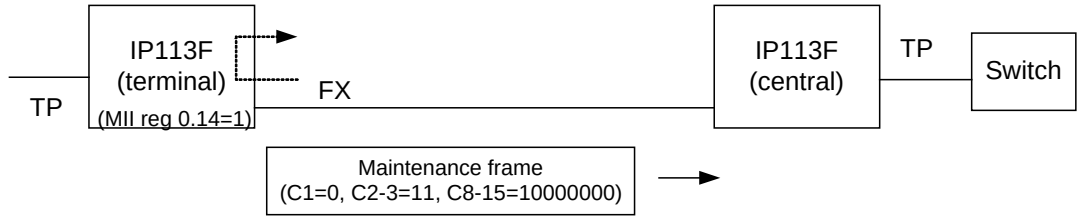
In-band loop back test

Besides performing the loop back test with an external packet source, IP113F supports an easy alternative. IP113F sends out private maintenance frame to do loop back test. All users have to do is to program MII registers through SMI.

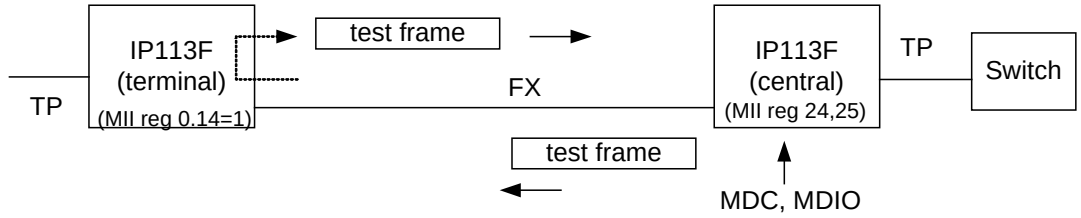
1. Disabe receive function of central TP port and instruct the terminal IP113F to perform loop back and disable T2 timer by programming central IP113F through SMI



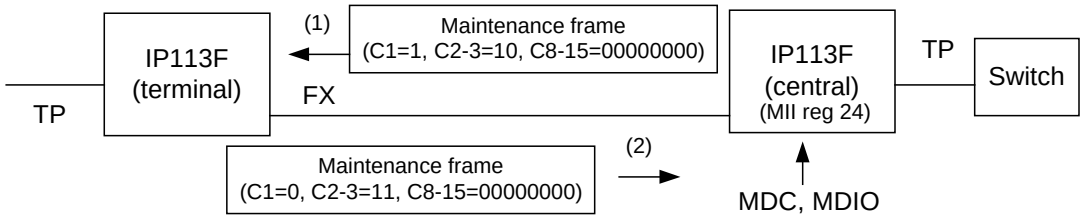
2. Terminal IP113F runs at loop back mode and acknowledges with maintenance frame



3. Central IP113F forces test frames to terminal IP113F and terminal IP113F loops back the test frames. Central IP113F checks the received test frame.



4. Central IP113F ends loop back test enables receive function of TP port and enable LP T2 timer



Loop back test (continued)

Programming procedure for In-band loop back test

Step	Description	C1	C3~C2	C15~C8	Note
1	Set local IP113F TP receive disabled				Set Reg. 20.14 off
2a	Set remote T2 timer disabled by maintenance frame	1	01	11 11 11 11	Reg24 and Reg 25
2	Set remote IP113F to be loop back mode enabled by maintenance frame	1	01	00 00 00 01	TS-1000: loop back set
3	Remote IP113F sends back loop back acknowledge	--	--	--	--
4	Send loop back test maintenance frame	1	01	11 01 10 11	Reg24 and Reg 25
5	Remote IP113F send back acknowledge	--	--	--	--
6	Local IP113F stores the loop back maintenance to Reg. 26~30 and checks CRC bit is in Reg. 26.12	--			
7	Repeat step 4~6 continuously	--			
8	Set remote IP113F to be loop back mode disable by maintenance frame	1	01	00 00 00 00	TC-1000: loop back end
9	Remote IP113F sends back loop back acknowledge	--	--	--	--
10	Set local IP113F TP receive enable				Set Reg. 20.14 on

Auto in-band loop back test

Step	Description
1	Set pin AUTO_TEST to “1” (The following step is executed automatically by IP113F)
1.1	Central IP113F sends loop back start request to remote IP113F and goes to CST2 state.
1.2	Remote IP113F sends loop back start acknowledge to Central IP113F and enters loop back test mode.
1.3	Central IP113F goes to CST1 state and begins sending 15 frames in 64 bytes.
1.4	Remote IP113F loops back the received frames at the TP port’s PMD sub-layer.
1.5	Central IP113F checks the loop back frames and reports the result.
2	The LED pin LED_RMT_TP_LINK is Flash (on 80ms / off 20ms) during the auto loop back test period (AUTO_TEST is “1”).
3	The LED pin LED_RMT_TP_SPD indicates the loop back test complete (on) (when AUTO_TEST is “1”). The LED pin LED_RMT_TP_FDX indicates the loop back test ok (on) (when AUTO_TEST is “1”)
4	If another auto loop back test is needed, set AUTO_TEST to “0” and then “1”. That is, AUTO_TEST is triggered whenever there is a low-to-high transition on this pin.

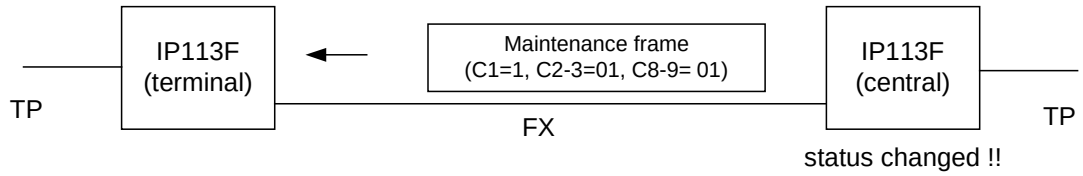
Remote monitor without SMI programming

Auto sends (Status change notice)

IP113F sends out status frame without receiving status request frame if pin AUTO_SEND is pulled high. It sends out the first status frame onto the fiber port when the link status of fiber port has established. It sends out status frames when the status on TP port has changed. IP113F supports two types of frame. For a TS-1000 maintenance frame, C[9:8] is 2'b10 and S[15:0] is defined as that in TS-1000 standard. For an ICplus maintenance frame, C[9:8] is 2'b11 and S[15:0] is the content of MII register 22. It carries ICplus private defined information. User can select the frame type by programming MII register 20.10. Central IP113F uses the mechanism to get the status of the remote IP113F even if there is no SMI programming.

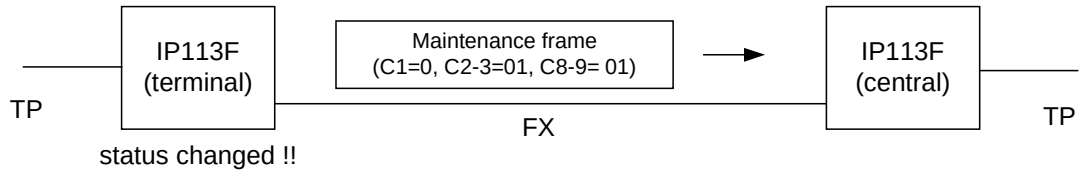
Option A

Central IP113F sends indication frames to terminal IP113F if its status is changed.

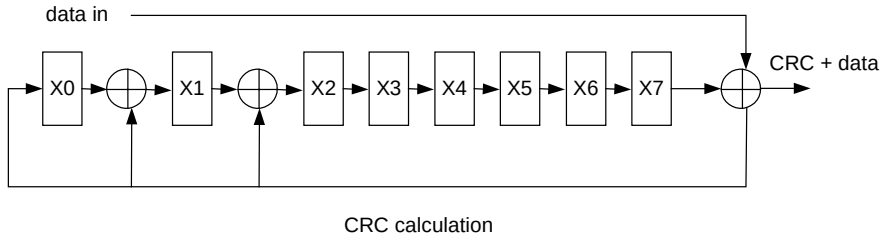


Option B

Terminal IP113F sends indication frames to central IP113F if its status is changed.

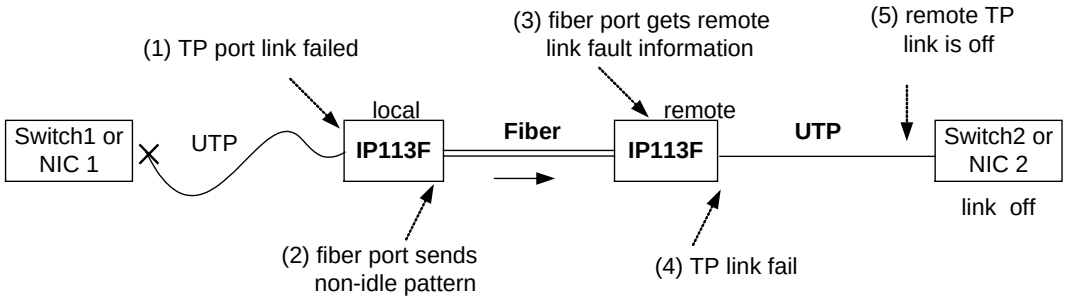


CRC polynomial for maintenance frame: X8 + X2 + X + 1



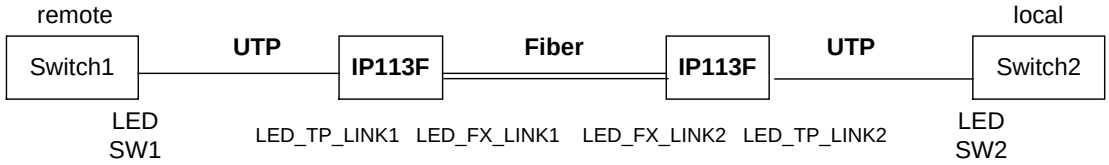
Link fault pass through

When link fault pass through function is enabled, link status on TX port will inform the FX port of the same device and vice versa. From the link fault pass through procedure illustrates in the figure below, if link fail happens on IP113F's TX port (1), the local FX port sends non-idle pattern to notice the remote FX port (2). The remote FX port then forces its TX port to link failed after receiving the non-idle pattern (4). In other words, this mechanism will alert the link fault status of local TX port to the remote converter's TX port, and the link status of the remote TX port will become off. Link status LED will also be off for both IP113F and its link partner.



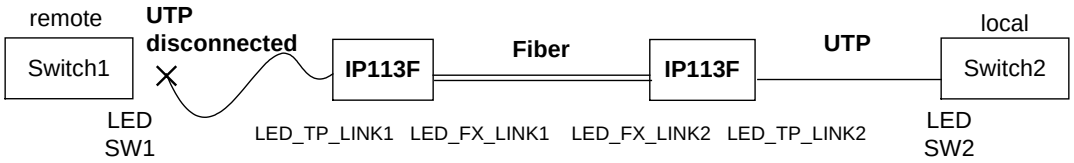
The procedure of link fault pass through

Normal case



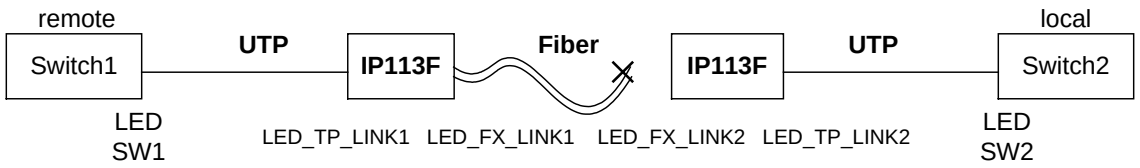
Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
ON	ON	ON	ON	ON	ON

Remote TP port disconnected



Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

FX port disconnected



Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

LED diagnostic functions for fault indication

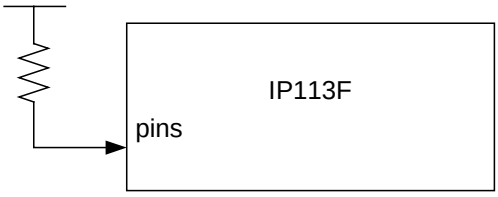
LED_TP_LINK	LED_FX_LINK	LED_FX_SD	LED_FX_FEF_DET	Status
On	On	On	Off	Link ok
Flash	Flash	On	Off	Link ok & activity
Off	Off	On	Off	Remote TP link off
Off	Off	Off	Off	Fiber RX off, Fiber TX/ RX off
Off	Off	On	Flash	Fiber TX off

Note
Flash: flash, period 100 ms
Link fault pass through is enabled.

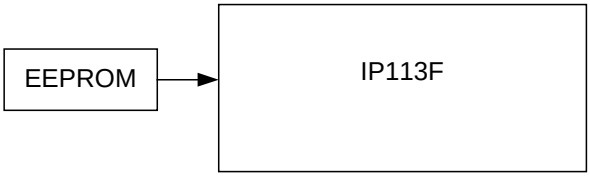
EEPROM – store the initial value

IP113F supports two ways to load initial value of MII registers. The procedure is illustrated as below.

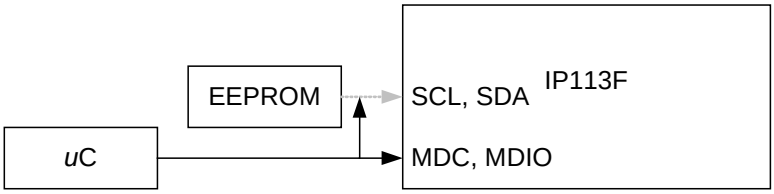
1. IP113F reads the default setting of MII register from pins



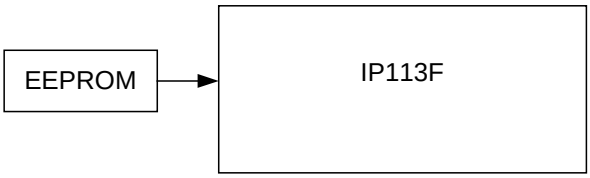
2. IP113F updates the default setting of MII by reading EEPROM. If there exists an EEPROM.



3. After reading EEPROM, IP113F is virtually isolated from the EEPROM. Micro-controller can program both MII register and EEPROM.

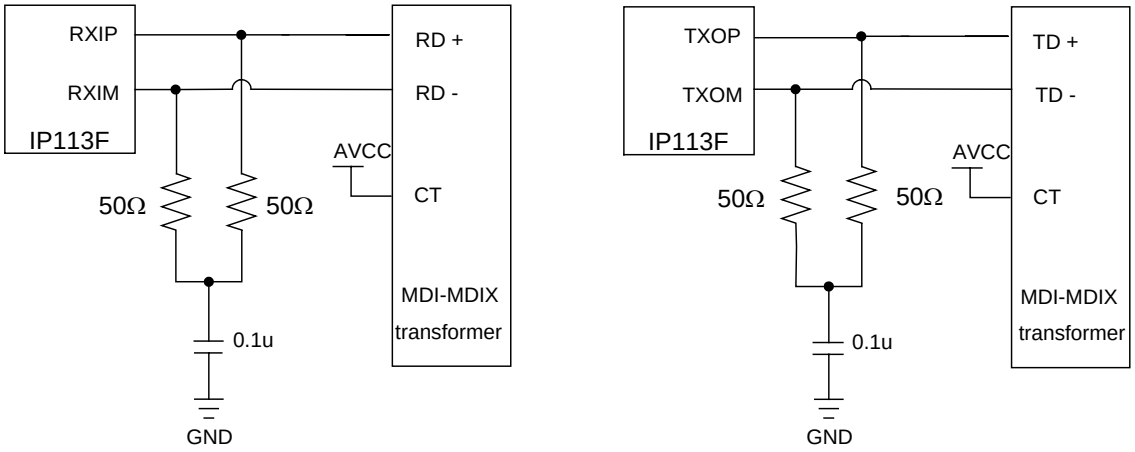


4. IP113F reloads the content of EEPROM to recover the value in MII registers programmed by Micro-controller after power on reset.



Auto MDI_MDIX

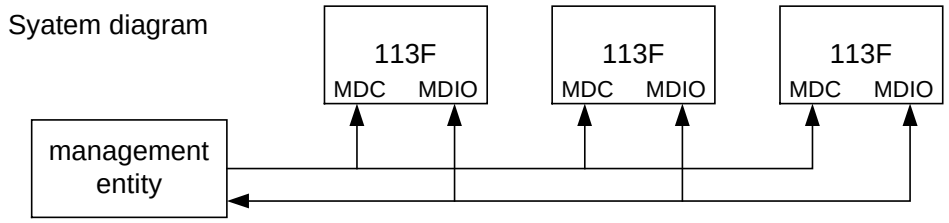
IP113F supports auto MDI-MDIX. It is always enabled. The following is its application circuit for auto MDI-MDIX.



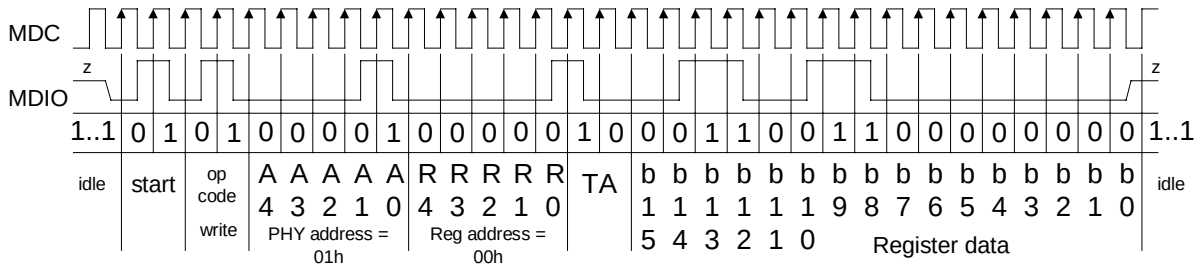
IP113F's application circuit (auto MDI-MDIX on)

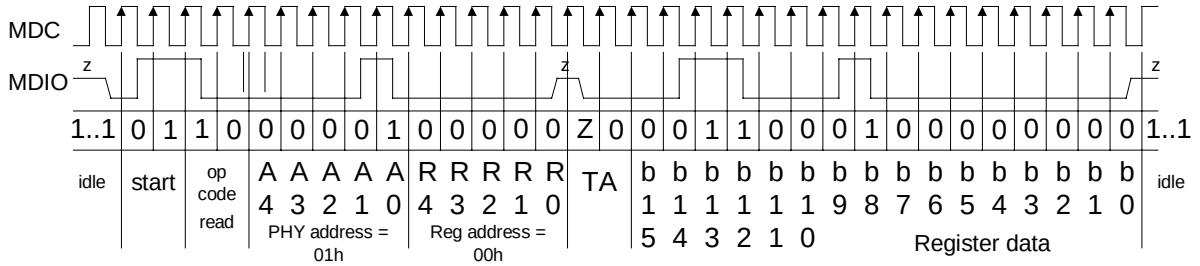
Serial management interface

User can access IP113F's MII registers through serial management interface MDC and MDIO. A specific pattern on MDIO is used to access a MII register. Its format is shown in the following table. When the SMI is idle, MDIO is in high impedance. To initialize the MDIO interface, the management entity sends a sequence of 32 contiguous "1" and "start" on MDIO.



Frame format	<Idle><start><op code><IP113F's address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 $b_1$$b_0$><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 $b_1$$b_0$><Idle>





MII registers

Address	Control	Register Name
0	Control Register	NWAY
1	Status Register	NWAY
2	PHY identifier Register 1	NWAY
3	PHY identifier Register 2	NWAY
4	AN Advertisement Register	NWAY
5	AN Link Partner Base Page Ability Register	NWAY
6	AN Expansion Register	NWAY
7	(Reserved)	
8	(Reserved)	
9	(Reserved)	
10	(Reserved)	
11	(Reserved)	
12	(Reserved)	
13	(Reserved)	
14	(Reserved)	
15	(Reserved)	
16	Special Control Register	NWAY
17	Interrupt Register	NWAY
18	Extended Status Register	NWAY
19	Statistic Counter Register	SWITCH
20	Switch Configuration Register 1	SWITCH
21	Switch Configuration Register 2	SWITCH
22	Local Switch Extended Register	SWITCH
23	Link Partner Switch Extended Status Register	SWITCH
24	Remote Control Transmit Register 1	RMC
25	Remote Control Transmit Register 2	RMC
26	Remote Control Receive Register 1	RMC
27	Remote Control Receive Register 2	RMC
28	Remote Control Receive Register 3	RMC
29	Remote Control Receive Register 4	RMC
30	Remote Control Receive Register 5	RMC
31	Switch Configuration Register 3	SWITCH

The basic MII registers

Type	Description
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
Pin(1)	The default value is “1” and it depends on the setting of its corresponding pin.

Type	Description
RC	Read and Clear
LL	Latching Low
LH	Latching High
Pin(0)	The default value is “0” and it depends on the setting of its corresponding pin.

MII	NAME	R/W	DESCRIPTION	DEFAULT
MII control register (address 00h)				
0.15	Reset	R/W SC	1 = PHY reset 0 = normal operation This bit is self-clearing, IP113F will return a value of 1 before reset process is completed, and will not accept any write transaction of MII Management within reset process. Make any change to Auto-Negotiation or speed mode will cause IP113F reset again.	0
0.14	Loopback	R/W	1 = Loopback mode 0 = normal operation When this bit is set, IP113F will be isolated from the network media, and the assertion of TXEN at the MII will not transmit data on the network. All MII transmit data path will return to MII receive data path in response to the assertion of TXEN. MII COL signal will remain de-asserted at all times, unless bit 0.7 (Collision Test) is set. Use has to wait about 100ms for loop back path ready.	0
0.13	Speed Selection	RW	1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	Pin(1)
0.12	Auto-Negotiation Enable	RW	1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable MII register 16.11 auto-MDI/MDIX should be disabled if auto-negotiation is disabled.	1
0.11	Power Down	R/W	1 = power down 0 = normal operation Setting this bit to 1 will cause IP113F into power down mode, but still respond to management transactions.	0
0.10	Isolate	R/W	1 = electrically isolate PHY from MII 0 = normal operation When this bit is setting to 1, IP113F will be isolated from RMII, and not respond to the TXD[3:0] and TXEN and keep CRS, RXDV and RXD[3:0] in high impedance, but will respond to management transactions. If PHY address of IP113F is setting to 0 at power-on reset, this bit will be set to 1, otherwise will be set to 0.	0

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
MII control register (address 00h)				
0.9	Restart Auto-Negotiation	RW	1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete Setting this bit to logic high will cause IP113F to restart an Auto-Negotiation cycle, but depend on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and change to Read Only. When an Auto-Negotiation cycle is being processed, write 0 into this bit has no effect. This bit is self-clearing after Auto-Negotiation process is completed.	0
0.8	Duplex mode	R/W	1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	Pin(1)
0.7	Collision test enable	R/W	1 = enable the collision test 0 = disable the collision test If setting this bit to logic 1, when MII TXEN signal is asserted, IP113F will assert the MII COL signal within 512BT (Bit Time, depend on 10Mbps or 100Mbps). When MII TXEN is de-asserted, then TP110 will assert MII COL signal within 4BT. Clearing this bit to logic 0 for normal operation	0
0[6:0]	Reserved	R/W	Write as 0, ignore on read	-

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
MII status register (address 01h)				
1.15	100Base-T4 capable	RO	1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP113F does not support 100Base-T4. This bit is fixed to be 0.	0
1.14	100Base-X full duplex Capable	RO	1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable The default of this bit will change depend on the external setting of IP113F. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0.	1
1.13	100Base-X half duplex Capable	RO	1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable The default of this bit will change depend on the external setting of IP113F. If external pin setting without 100Base-X half duplex support, then this bit will change default to logic 0	1
1.12	10Base-T full duplex Capable	RO	1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable The default of this bit will change depend on the external setting of IP113F. If external pin setting without 100Base-T full duplex support, then this bit will change default to logic 0	1
1.11	10Base-T half duplex Capable	RO	1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable The default of this bit will change depend on the external setting of IP113F. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0	1
1[10:7]	Reserved	RO	Ignore on read	-
1.6	MF preamble Suppression	RO	1 = preamble may be suppressed 0 = preamble always required	1
1.5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4, 5, 6 and 7 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4, 5, 6 and 7 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
MII status register (address 01h)				
1.4	Remote fault	RO LH	1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP113F has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP113F reset.	0
1.3	Auto-Negotiation Ability	RO	1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP113F has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of IP113F operation mode.	1
1.2	Link Status	RO LL	1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP113F has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
1.1	Jabber Detect	RO LH	1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP113F has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP113F reset. This bit is set until jabber condition is cleared and reading the contents of the register.	0
1.0	Extended capability	RO	1 = Extended register capabilities 0 = No extended register capabilities IP113F has extended register capabilities.	1

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
PHY Identifier (address 02h)				
2[15:0]	PHY identifier	RO	IP113F OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of IP113F OUI ID, and the lsb is 18th bit of IP113F OUI ID. IP113F OUI is 0090C3.	0243h

MII	NAME	R/W	DESCRIPTION	DEFAULT
PHY Identifier (address 03h)				
3[15:10]	PHY identifier	RO	IP113F OUI ID, the msb is 19th bit of IP113F OUI ID, and lsb is 24th bit of IP113F OUI ID.	3h
3[9:4]	Manufacture's Model Number	RO	TP110 model number	6h
3[3:0]	Revision Number	RO	IP113F revision number	0

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
Auto-Negotiation Advertisement register (address 04h)				
4.15	Next Page	RO	1 = Next Page ability is supported 0 = Next Page ability is not supported IP113F does not support next page, this bit is fixed to be 0.	0
4.14	Reserved	RW	Reserved by IEEE, write as 0, ignore on read	0
4.13	Remote Fault	R/W	1 = Advertises that this device has detected a remote fault 0 = No remote fault detected	0
4[12:11]	Reserved	RO	Reserved for future IEEE use, write as 0, ignore on read	0
4.10	Pause	RW	1 = Advertises that this device has implemented pause function 0 = No pause function supported	Pin(0)
4.9	100BASE-T4	RW	1 = 100BASE-T4 is supported 0 = 100BASE-T4 is not supported	0
4.8	100BASE-TX full duplex	R/W	1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	Pin(1)
4.7	100BASE-TX	R/W	1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	Pin(1)
4.6	10BASE-T full duplex	R/W	1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	Pin(1)
4.5	10BASE-T	R/W	1 = 10BASE-T is supported 0 = 10BASE-T is not supported	Pin(1)
4[4:0]	Selector Field	RO	Use to identify the type of message being sent by Auto-Negotiation.	00001

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
Link partner ability register (address 05h) Base Page				
5.15	Next Page	RO	1 = Next Page ability is supported by link partner 0 = Next Page ability is not supported by link partner	0
5.14	Acknowledge	RO	1 = Link partner has received the ability data word 0 = Not acknowledge	0
5.13	Remote Fault	RO	1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
5[12:10]	Reserved	RO	Reserved by IEEE for future use, write as 0, read as 0.	0
5.9	100BASE-T4	RO	1 = Link partner support 100BASE-T4 0 = Link partner is not support 100BASE-T4	0
5.8	100BASE-TX full duplex	RO	1 = Link partner support 100BASE-TX full duplex 0 = Link partner is not support 100BASE-TX full duplex	0
5.7	100BASE-TX	RO	1 = Link partner support 100BASE-TX 0 = Link partner is not support 100BASE-TX	0
5.6	10BASE-T full duplex	RO	1 = Link partner support 10BASE-T full duplex 0 = Link partner is not support 10BASE-T full duplex	0
5.5	10BASE-T	RO	1 = Link partner support 10BASE-T 0 = Link partner is not support 10BASE-T	0
5[4:0]	Selector Field	RO	Protocol selector of the link partner	00000

The basic MII registers (continued)

MII	NAME	R/W	DESCRIPTION	DEFAULT
Auto-Negotiation Expansion register (address 06h)				
6[15:5]	Reserved	RO	Reserved by IEEE, writes as 0, ignore on read.	0
6.4	Parallel Detection Fault	RO LH	1 = A fault has been detected via Parallel Detection function 0 = A fault has not detected via Parallel Detection function	0
6.3	Link Partner Next Page Able	RO	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	0
6.2	Next Page Able	RO	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	0
6.1	Page Received	RO LH	1 = A New Page has been received 0 = A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	0

Extended MII registers and EEPROM registers

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
EEPROM enable register 0 (EEPROM register 00D)					
--	0[7:0]		RO	**EEPROM enable register 0** This register should be filled with 55. IP113F will examine the specified pattern to confirm if there is a valid EEPROM.	55

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
EEPROM enable register 1 (EEPROM register 01D)					
--	1[7:0]		RO	**EEPROM enable register 1** This register should be filled with AA. IP113F will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found.	AA

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Special control register (16D)					
16.0	--	mr_analog_off	R/W	ANALOG on/off (It is valid only if register 16.15=0.) 1: analog off, 0: analog on (default)	0
16.1	--	mr_lpds_mode	R/W	Low power mode disable (It is valid only if 16.15=0.) 1: disable, 0:enable (default)	0
16.2	--	mr_repeater_mode	R/W	REPEAT mode enable 1: enable, 0:disable (default)	0
16.3	--	mr_bypass_scramble	R/W	Bypass PCS scrambler (It is valid only if 16.15=1.) 1: bypass scrambler, 0: not bypass (default)	0
16.4	--	mr_bypass_100x _coder	R/W	Bypass PCS 4B/5B coder (It is valid only if 16.15=1.) 1: bypass 4B/5B, 0: not bypass (default)	0
16.5	--	mr_bypass_dsp _rst	R/W	Bypass DSP re-start function in PCS 1: bypass DSP re-start, 0: not bypass (default)	0
16.6	--	mr_tx_nlp_disable	R/W	10Mb transmit NLP enable 1: enable (default), 0:disable	0
16.7	--	mr_analog_pwsv _disable	R/W	Analog power save mode disable 1: disable, 0: enable (default)	0
16.8	--	mr_fef_disable	R/W	Far-End-Fault function disable 1: disable, 0: enable (default)	0
16.9	--	mr_jabber_enable	R/W	Jabber function enable 1: enable, 0:disable (default)	0
16.10	--	mr_heart_beat _enable	R/W	Heart Beat function enable 1: enable, 0:disable (default)	0
16.11	--	mr_auto_cross _disable	R/W	Auto Crossover function disable 1: disable, 0: enable (default) It should be disabled if MII register 0.12 auto-negotiation is disabled.	0
16.12	--	mr_speed_up_dsp	R/W	Speed Up DSP (It is valid only if 16.15=1.) 1: enable, 0:disable (default)	0
16.13	--	mr_speed_up	R/W	Speed Up Digital Simulation (It is valid only if 16.15=1.) 1: enable, 0:disable (default)	0
16.14	--	Reserved	R/W		0
16.15	--	mr_debug_mode	R/W	DEBUG mode enable 1: enable, 0:disable (default)	0

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Interrupt register (17D)					
17.0	--	intr_link	RO RC	Link status change It is logic “1” when link status changes on TP port and it will active interrupt pin. It is self-clear after reading the register. 1: Interrupt occur 0: nothing happen	0
17.1	--	intr_duplex	RO RC	Duplex mode change 1: Interrupt occur 0: nothing happen	0
17.2	--	intr_speed	RO RC	Speed mode change 1: Interrupt occur 0: nothing happen	0
17.3	--	intr_mf_rx_indicate	RO RC	Maintenance frame receive indication 1: Interrupt occur 0: nothing happen	0
17.4	--	intr_cnt_overflow	RO RC	Statistic counter overflow 1: Interrupt occur 0: nothing happen	0
17.5	--	intr_status	RO RC	Interrupt status 1: Interrupt occur 0: nothing happen It is logic “OR” of 17.0~17.4.	0
17.6	--	Intr_pwabn	RO RC	Interrupt status 1: remote link partner power abnormal 0: nothing happen	0
17.7	--	Intr_pwabn_en	RW	Remote LP power abnormal interrupt enable 1: not mask interrupt 0: mask interrupt	0
17.8	--	intr_link_mask	RW	Mask TP port link change Interrupt 1: mask, 0: not mask (default)	1
17.9	--	intr_duplex_mask	RW	Mask TP port duplex mode change Interrupt 1: mask interrupt (default), 0: not mask	1
17.10	--	intr_speed_mask	RW	Mask TP port speed mode change Interrupt 1: mask interrupt (default), 0: not mask	1
17.11	--	intr_mf_rx_indc _mask	RW	Mask maintenance frame receive indication Interrupt 1: mask interrupt (default), 0: not mask	1
17.12	--	intr_cnt_ov_mask	RW	Mask Statistic counter overflow Interrupt 1: mask interrupt (default), 0: not mask	1
17.13	--	intr_all_mask	RW	Mask all Interrupt 1: mask interrupt (default), 0: not mask	1
17[15:14]	--	Reserved	RW		0

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
PHY extended status register (18D)					
18[3:0]	--	an_arbit_state[3:0]	RO	NWAY state machine	0
18[6:4]	--	Reserved[2:0]	RO		0
18.7	--	jabber	RO	Jabber status 1: jabber, 0: no jabber (default)	0
18.8	--	polarity	RO	Polarity status 1: polarity error, 0: polarity ok (default)	0
18.9	--	mdix_en	RO	MDI/MDIX status 0: MDI, 1:MDIX	0
18.10	--	link_real	RO	TP port link Status 1: link ok, 0; link fail (default)	0
18.11	--	resolved	RO	Resolve complete 1: Nway or force mode complete, 0: not complete (default)	0
18.12	--	Reserved	RO		0
18.13	--	mr_duplex_mode	RO	TP port duplex mode (It is valid only if 18.11=1.) 1: full (default), 0: half	1
18.14	--	mr_speed_selection	RO	TP port operation speed (It is valid only if 18.11=1.) 1: 100M (default), 0: 10M	1
18.15	--	Reserved	RO		0

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Statistic counter registers (MII register 19D)					
19[11:0]	--	mg_statistic_cnt[11:0]	RO	Statistic Counter [11:0]	0
				Cnt_index: Content of statistic counter[11:0]	
				3'b000: TP port (port1) received packet count	
				3'b001: TP port (port1) received CRC error count	
				3'b010: TP port (port1) drop packet count	
				3'b011: TP port (port1) collision event count	
				3'b100: FX port (port2) received packet count	
				3'b101: FX port (port2) received CRC error count	
				3'b110: FX port (port2) drop packet count	
				3'b111: FX port (port2) collision event count	
19[14:12]	--	cnt_index[2:0]	RW	The current counter index	0
19.15	--	cnt_loop_en	RW	The counter index loop enable 1: Each time reading of this register (MII register 19) will increase cnt_index[2:0] by one. The content will be loop back to “0” after reading if it is “7”. 0: cnt_index[2:0] is fixed to the setting value.	1

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 1 (MII register 20D, EEPROM register 02~03D)					
20.0	2.0	mg_crossover_en	R/W	Select TP to be MDIX or MDI. It is valid only if MII register16.11 is disabled. 0: MDI 1: MDIX	0
20.1	2.1	direct_wire	R/W	Please see pin description of DIRECT_WIRE for more detail information.	Pin (0)
20.2	2.2	fast_fwd	R/W	Please see pin description of FAST_FWD for more detail information.	Pin (0)
20.3	2.3	mg_pass_fragment _en	R/W	Pass fragment packet (>7B and <64B) 1: pass fragment 0: not pass fragment	0
20.4	2.4	mg_col16_drop_en	R/W	Collision 16 times drop enable 1: drop 0: not drop	0
20.5	2.5	mg_col_backoff _en	R/W	Collision back-off enable 1: back after collision 0: not back off after collision	1
20.6	2.6	reserved	R/W	It must be 0.	0
20.7	2.7	p01_mg_backpress _en	R/W	TP port backpressure control enable for half duplex 1: backpressure enable 0: backpressure disable	1
20.8	3.0	mg_rem_ctrl_en	R/W	Remote control enable (TX/RX. ability for maintenance frame) 1: ability enable 0: ability disable	1
20.9	3.1	mg_auto_tx_mf_en	R/W	Auto send status frame to remote partner enable (AUTO_SEND) 1: auto send indication maintenance frame 0: disable auto send	Pin (0)
20.10	3.2	mg_auto_tx_ttc _content	R/W	The content of auto send status frame 1: TTC (TS-1000) The frame format is defined in TS-1000. 0: ICPLUS The frame format is similar to the one defined in TS-1000 except the bit definition of S[15:0]. S[15:0] is the content of MII register 22[15:0]. Local IP113F uses the frame to indicate its status to the remote IP113F. The remote IP113F receives the frame and stores the information to the MII register 23.	1
20.11	3.3	mg_sd_off_way	R/W	Informing way for optical receiving SD off 1: far end fault pattern 0: maintenance frame	1

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 1 (MII register 20D, EEPROM register 02~03D)					
20.12	3.4	mg_em_bist_en	R/W	SSRAM BIST enable (R/W by EEPROM only) 1: BIST enable 0: bypass BIST	1
20.13	3.5	tp_force	R/W	This pin overwrites the setting on pin 26 TP_FORCE.	Pin (0)
20.14	3.6	mg_receive_en	R/W	TP receive enable 1: TP port can receive packet 0: TP port drop all received packet	1
20.15	3.7	p02_link_on	RO	Fiber port link status (descramble_locked) 1: Fiber port is link 0: Fiber port is not link	0

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 2 (MII register 21D, EEPROM register 04~05D)					
21[7:0]	4[7:0]	p01_mg_port _page_no	R/W	TP port allocated memory pages The default is 120 pages with 64 bytes per page.	120d
21[15:8]	5[7:0]	p02_mg_port _page_no	R/W	FX port allocated memory pages The default is 120 pages with 64 bytes per page.	120d

Note: p01_mg_port_page_no adds p02_mg_port_page_no must be equal to 240.

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Local MC extended register (MII register 22D, EEPROM register 06~07D)					
22.0	6.0	mg_loopback_en	R/W	Loop-back test enable (same as MII register 0.14) 1: loop back mode 0: normal mode	0
22.1	6.1	mg_status_rpt _en	RO	TP port status available 1: TP status is valid 0: TP status is not ready	0
22.2	6.2	p01_mg_auto _neg_en	R/W	TP port auto-negotiation enable (same as MII register 0.12) 1: TP auto-negotiation enable 0: TP auto-negotiation disable	1
22.3	6.3	p01_mg_speed _mode	R/W	TP port speed selection (same as MII register 0.13) 1: 100M, 0:10M	Pin (1)
22.4	6.4	p01_mg_duplex _mode	R/W	TP port duplex mode selection (same as MII register 0.8) 1: full duplex, 0:half duplex	Pin (1)
22.5	6.5	p01_mg_flow _ctrl_en	R/W	TP port flow control selection (same as MII register 4.10) 1: on, 0:off	Pin (1)
22.6	6.6	p01_mg_link _status	RO	TP port link status off 1: link off, 0: link ok	0
22.7	6.7	p02_mg_flow _ctrl_en	R/W	Fiber port flow control/backpressure enable 1: enable, 0: disable	Pin (1)
22.8	7.0	p02_mg_duplex _mode	R/W	Fiber port duplex mode (FX_FULL) 1: full duplex, 0:half duplex	1
22.9	7.1	p02_mg_link _status	RO LL RC	Fiber port signal detect (power) 1: Fiber SD has been low since last read 0: Fiber SD is O.K.	1
22.10	7.2	p02_mg_fef _detect	RO LH RC	Fiber port Far-End-Fault detect 1: FEF has been detected since last read 0: no FEF pattern detected	0
22[12:11]	7[4:3]	p01_mg_throttle _confg	R/W	TP port input Rate Control 2'b00: full speed 2'b01: 1/4 speed 2'b10: 2/4 speed 2'b11: 3/4 speed	00
22[14:13]	7[6:5]	p01_mg_throttle_co nfg	R/W	TP port output Rate Control 2'b00: full speed 2'b01: 1/4 speed 2'b10: 2/4 speed 2'b11: 3/4 speed	00
22.15	7.7	mg_link_pass_en	R/W	Link Fault Pass through enable (LFP) 1: enable, 0: disable	Pin (0)

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Link partner MC extended status register (MII register 23D)					
23.0	--	lp_loopback_en	RO	Loop-back enable of remote LP 1: LP is in loop back mode 0: LP is in normal mode	0
23.1	--	lp_status_rpt_en	RO	Option B support 1: support 0: not support	0
23.2	--	lp_tp_autoneg_en	RO	TP port auto-negotiation enable 1: enable, 0:disable	0
23.3	--	lp_tp_speed_mode	RO	TP port speed selection 1: 100M, 0:10M	0
23.4	--	lp_tp_duplex_mode	RO	TP port duplex mode selection 1: full duplex, 0: half duplex	0
23.5	--	lp_tp_flow_ctrl_en	RO	TP port flow control selection ∗ Note 1: flow control enable 0: flow control disable	0
23.6	--	lp_tp_link_off	RO	TP port link off 1: link off, 0:link on	1
23.7	--	lp_fb_flow_ctrl_en	RO	Fiber port flow control/backpressure enable ∗ 1: flow control enable 0: flow control disable	0
23.8	--	lp_fb_duplex_mode	RO	Fiber port duplex mode ∗ 1: full duplex, 0: half duplex	0
23.9	--	lp_fb_link_status	RO	Fiber port signal detect (power) off ∗ 1: off, 0: on	0
23.10	--	reserved	RO		0
23.11	--	lp_power_abnormal	RO	MC power abnormal 1: power abnormal 0: power O.K.	0
23.12	--	lp_mc_failed	RO	MC failed 1: MC is out of function 0: MC is normal	0
23.13	--	lp_sd_off_way	RO	Link Partner informing way of SD off 1: far end fault pattern 0: maintenance frame	0
23.14	--	lp_multi_tp_port	RO	MC support multi-port UTP 1: more than one TP port 0: one TP port	0
23.15	--	mg_link_pass_en	RO	Link Fault Pass through enable ∗ 1: LFP is enable 0: LFP is disable	0

∗ Note: Only available when MII 20.10 = 0.

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Transmit register 1 (MII register 24D)					
24.0	--	mg_rem_tx_code	R/W	Remote control frame send trigger	0
24.1	--	mg_rem_tx_code	R/W	Transmitted maintenance direction discriminator C1 Frame direction 0: upstream 1: downstream	0
24[3:2]	--	mg_rem_tx_code	R/W	Transmitted maintenance frame command discriminator C3~C2 01: request 11: acknowledge 10: Indication 00: reserved	00
24[11:4]	--	mg_rem_tx_code	R/W	Transmitted maintenance frame control signals C15~C8 bit11 (C15) bit4 (C8) 0 0 0 0 0 0 01: Loop test start 0 0 0 0 0 0 00: Loop test finished 0 0 0 0 0 0 10: Status indication A4 A3 A2 A1 A0 RW 11: IP113F R/W registers RW: 0: read, 1: write A[4:0]: register address	8'b0
24[15:12]	--	Reserved			

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Transmit register 2 (MII register 25D)					
25[15:0]	--	mg_rem_wt_data	R/W	Remote control write data If a remote write command is issued, that is, MII register 24[11:4] is programmed as xxxxx111. The content in this register will be embedded into S[15:0] and is sent to the remote site. The partner IP113F receives the frame (register write) and update the addressed MII register with the value defined in this register	16'b0

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Receive register 1 (MII register 26D)					
26.0	--	mg_rem_rx_code	RO RC	Receive a acknowledge or not defined maintenance frame C0 1: IP113F receives a maintenance frame. 0: no maintenance frame received. User can poll this bit to make sure a there is a maintenance frame is received. It is a read and auto-clear bit.	0
26.1	--	mg_rem_rx_code	RO	Received maintenance direction discriminator C1	0
26[3:2]	--	mg_rem_rx_code	RO	Received maintenance frame command discriminator C3~C2	00
26[11:4]	--	mg_rem_rx_code	RO	Received maintenance frame control signals C15~C8	8'b0
26[12]	--	mg_rem_rx_code	RO RC	Received maintenance frame CRC error 1: received maintenance frame CRC error. 0: received maintenance frame CRC ok. It is a read and auto-clear bit.	
26[15:13]	--	Reserved			

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Receive register 2 (MII register 27D)					
27[15:0]	--	mg_rem_rd_data	RO	Remote control read data S0~S15.	16'b0

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Receive register 3 (MII register 28D)					
28[15:0]	--	mg_rem_rd_data	RO	Vender message M0~M15	16'b0

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Receive register 4 (MII register 29D)					
29[15:0]	--	mg_rem_rd_data	RO	Vender message M16~M29	16'b0

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Remote control Receive register 5 (MII register 30D)					
30[15:0]	--	mg_rem_rd_data	RO	Vender message M30~M55	16'b0

Extended MII registers and EEPROM registers (continued)

MII	ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 3 (MII register 31D)					
31.0	--	software_reset	R/W SC	Chip software reset It is a self-clear bit. All registers are not affected after the software reset is asserted. 1: reset, 0: not reset	0
31.1	--	mg_power_indicate _disable	R/W	IP113F power abnormal indication disable 1: disable power abnormal notice 0: enable power abnormal notice	0
31[3:2]	--	link_list_fail	RO	Link list failure indication bit[2] : TP port link list abnormal bit[3] : Fiber port link list abnormal 1: fail 0: ok	00
31[5:4]	--	BIST_status	RO	BIST Status of embedded SSRAM bit[4] : memory is under testing 1: under testing, 0: testing over bit[5] : memory test result is good when testing over 1: good, 0: fail	01
31[6]	--	mg_auto_loopback _test	R/W	Auto loopback test enable 1: enable, 0:disable	0
31[7]	--	mg_t2_timer _disable	R/W	Loopback test T2 timer disable (TS-1000) 1: The MC will not send loopback end indication MF when T2 timer expired 0: The MC will send loopback end MF when T2 timer expired	0
31[8]	--	mg_auto_loopback _complete	RO	Auto loopback test complete 1: completed, 0: still testing	0
31[9]	--	mg_auto_loopback _ok	RO	Auto loopback test OK 1: good, 0: fail	0
31[15:10]	--	Reserved			

3. Signal Requirements

3.1. Absolute Maximum Rating

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to Vcc+0.3V
Input Voltage	–0.3V to Vcc+0.3V
Output Voltage	–0.3V to Vcc+0.3V
Storage Temperature	-55°C to 125°C
Ambient Operating Temperature (Ta)	0°C to 70°C

3.2. DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.375	2.5	2.645	V	
Operation Junction Temperature	Tj		TBD		°C	
Power Consumption			0.475		W	VCC=2.5v

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-100		+100	PPM	

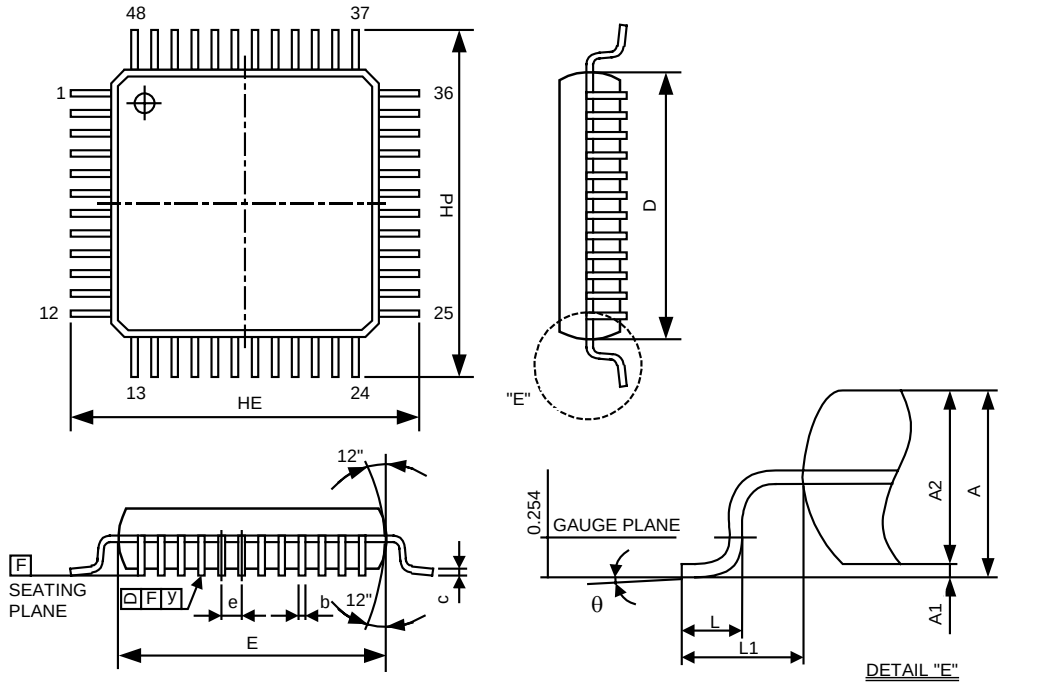
I/O Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA
Output High Voltage	VOH	VCC_IO-0.4			V	IOL=4mA

4. Order Information

Part No.	Package	Notice
IP113F	48-PIN LQFP	-

5. Package Detail



Symbol \ unit	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400 ± 0.05	0.0551 ± 0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000 ± 0.100	0.2756 ± 0.0039
E	7.000 ± 0.100	0.2756 ± 0.0039
e	0.500TYP	0.0196TYP
Hd	9.000 ± 0.250	0.3543 ± 0.0098
He	9.000 ± 0.250	0.3543 ± 0.0098
L	0.600 ± 0.150	0.0236 ± 0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
θ	0"~7"	0"~7"

Notes:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

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