



## GENERAL DESCRIPTION

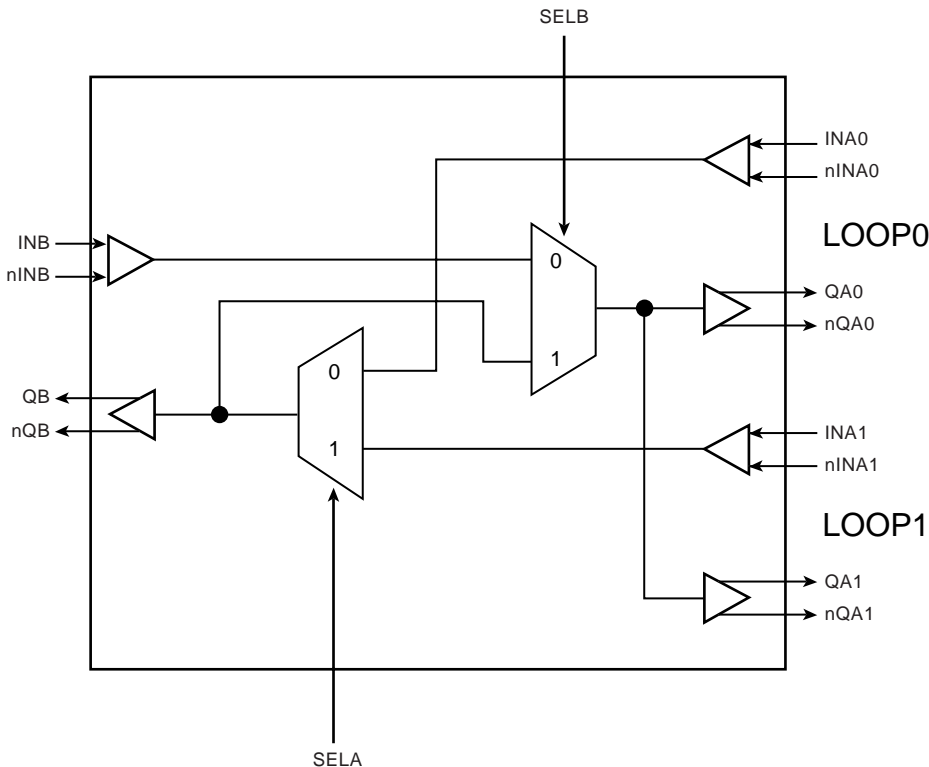
The ICS85454-01 is a 2:1/1:2 Multiplexer and a member of the HiPerClockS™ family of high performance clock solutions from ICS. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to both of two outputs. This device may be useful for multiplexing multi-rate Ethernet PHYs which have 100Mbit and 1000Mbit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. Another mode allows loop back testing and allows the output of a PHY transmit pair to be routed to the PHY input pair. For examples, please refer to the Application Information section of the data sheet.

The ICS85454-01 is optimized for applications requiring very high performance and has a maximum operating frequency in 2.5GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

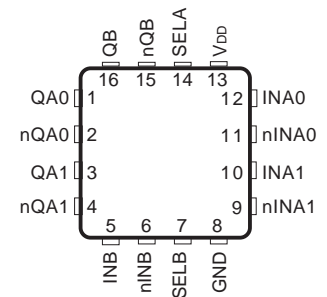
## FEATURES

- Dual 2:1/1:2 MUX
- Three LVDS outputs
- Three differential inputs
- Differential inputs can accept the following differential levels: LVPECL, LVDS, CML
- Loopback test mode available
- Maximum output frequency: 2.5GHz
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.05ps (typical)
- Propagation delay: 550ps (maximum)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS85454-01**  
**16-Lead VFQFN**  
 3mm x 3mm x 0.95 package body  
**K Package**  
 Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
3, 4	QA1, nQA1	Output		Differential output pair. LVDS interface levels.
5	INB	Input	Pulldown	Non-inverting differential clock input.
6	nINB	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
7	SELB	Input	Pulldown	Select pin for QAx outputs. When HIGH, selects same inputs used for QB output. When LOW, selects INB input. LVCMOS/LVTTL interface levels.
8	GND	Power		Power supply ground.
9	nINA1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
10	INA1	Input	Pulldown	Non-inverting differential clock input.
11	nINA0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
12	INA0	Input	Pulldown	Non-inverting differential clock input.
13	$V_{DD}$	Power		Positive supply pin.
14	SELA	Input	Pulldown	Select pin for QB outputs. When HIGH, selects INA1 input. When LOW, selects INA0 input. LVCMOS/LVTTL interface levels.
15, 16	nQB, QB	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			37.5		$k\Omega$
$R_{PULLUP}$	Input Pullup Resistor			37.5		$k\Omega$

**TABLE 3. INPUT CONTROL FUNCTION TABLE**

Control Inputs		Mode
SELA	SELB	
0	0	LOOP0 selected
1	0	LOOP1 selected
0	1	Loopback mode: LOOP0
1	1	Loopback mode: LOOP1



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient)	51.5°C/W (0 lfpm)

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				90	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		0		0.7	V
$I_{IH}$	Input High Current	SELA, SELB $V_{DD} = V_{IN} = 2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	SELA, SELB $V_{DD} = 2.625V, V_{IN} = 0V$	-150			$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{IH}$	Input High Current			150			150			150	$\mu A$
$I_{IL}$	Input Low Current	-150			-150			-150			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage	0.15		1.2	0.15		1.2	0.15		1.2	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2	1.2		$V_{DD}$	1.2		$V_{DD}$	1.2		$V_{DD}$	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for INAx, nINAx and INB, nINB is  $V_{DD} + 0.3V$ .



**TABLE 4D. LVDS DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OD}$	Differential Output Voltage	250	350	450	250	350	450	250	350	450	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			30			30			30	mV
$V_{OS}$	Offset Voltage	0.93	1.18	1.43	0.97	1.22	1.47	1.02	1.27	1.52	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			10			10			10	mV

NOTE 1: Refer to Parameter Measurement Information, "2.5V Output Load Test Circuit" diagram.

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 2.375V$  TO  $2.625V$**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				2.5	GHz
$t_{PD}$	Propagation Delay; NOTE 1	INAx to QB or INB to QAx	250		550	ps
		INAx to QAx	300		650	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3			250		ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	$f = 622.08MHz$ , 12kHz - 20MHz		0.05		ps
$MUX_{ISOLATION}$	MUX Isolation	@ 500MHz output		55		dB
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	50		250	ps

All parameters are measured  $\leq 1.7GHz$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

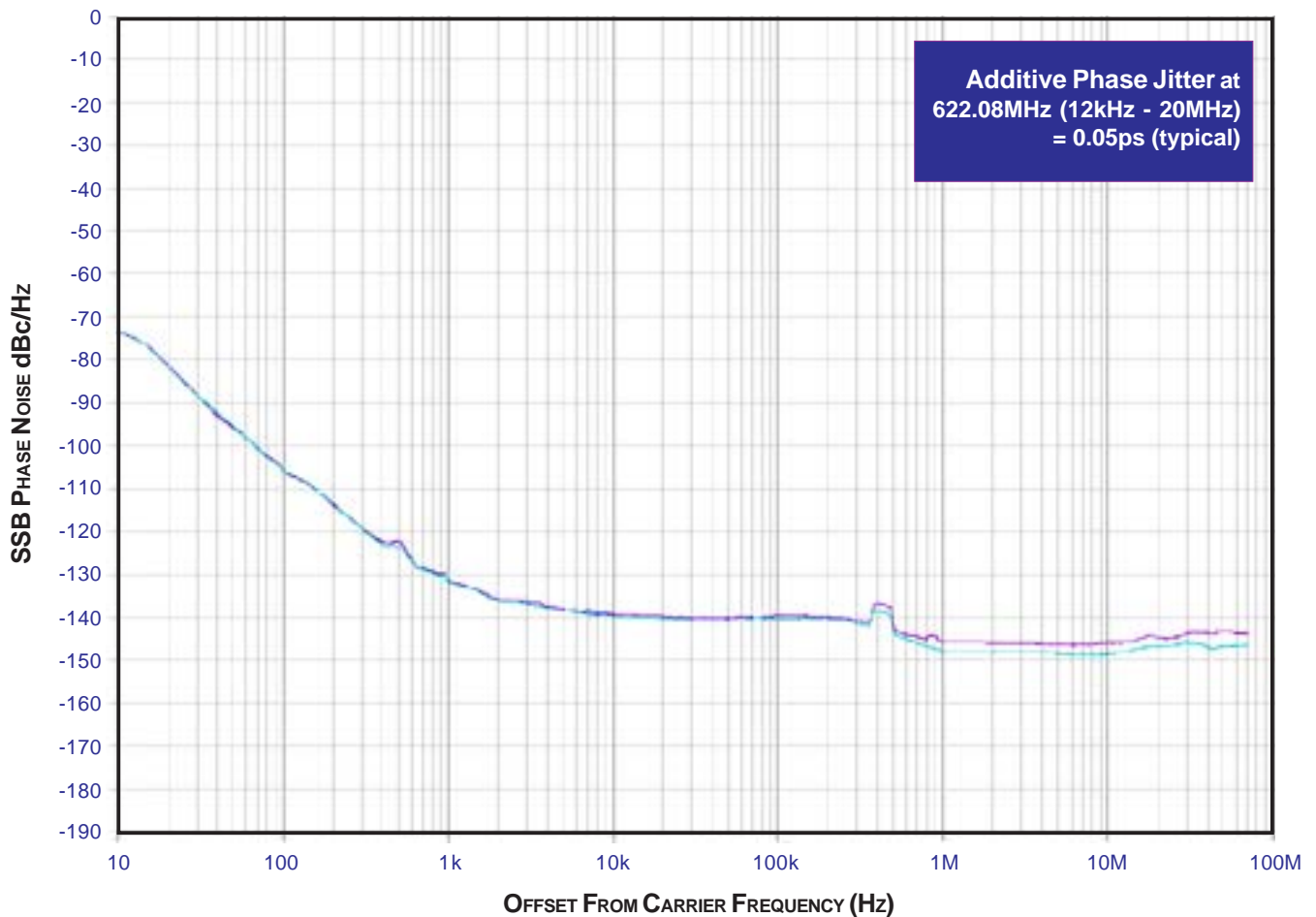
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



### ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

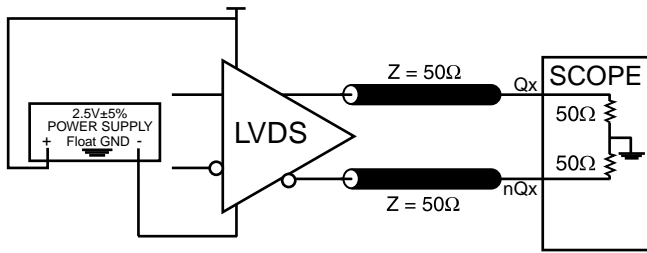


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated

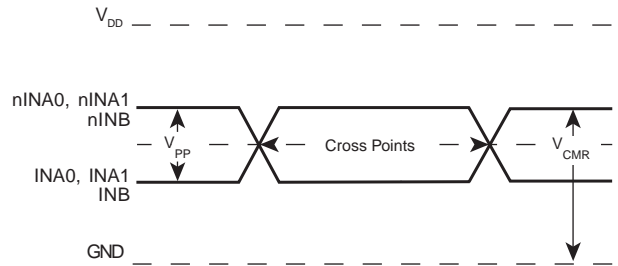
above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



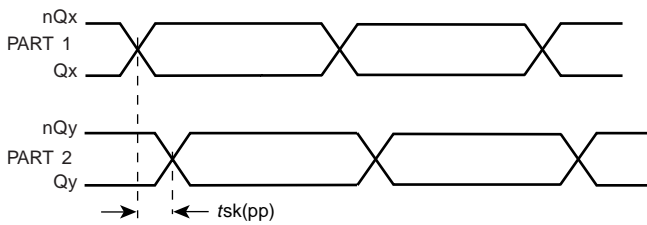
**PARAMETER MEASUREMENT INFORMATION**



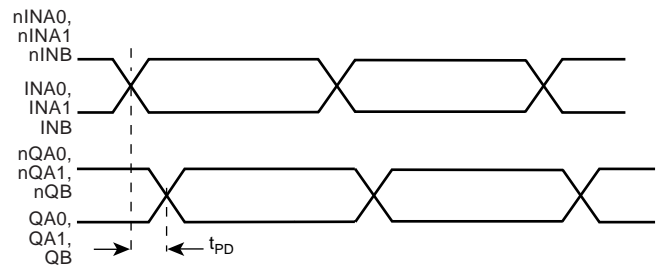
**OUTPUT LOAD AC TEST CIRCUIT**



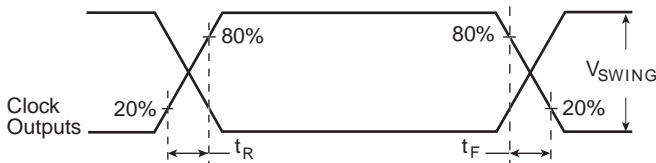
**DIFFERENTIAL INPUT LEVEL**



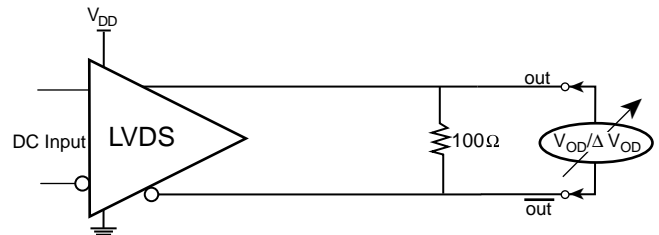
**PART-TO-PART SKEW**



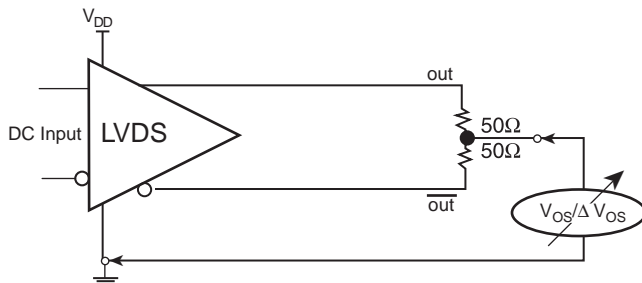
**PROPAGATION DELAY**



**OUTPUT RISE/FALL TIME**



**DIFFERENTIAL OUTPUT VOLTAGE**



**OFFSET VOLTAGE SETUP**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit

should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing.

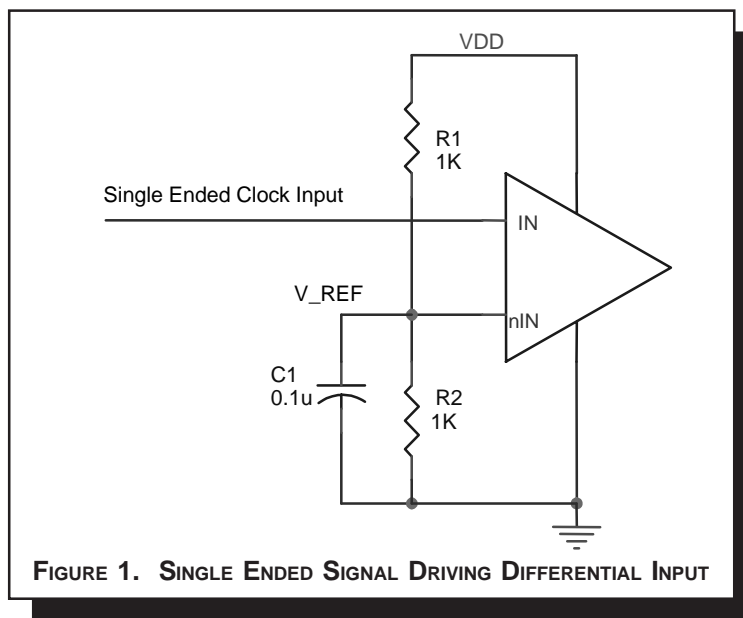


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### IN/nIN INPUT:

For applications not requiring the use of the differential input, both IN and nIN can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from IN to ground.

##### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVDS

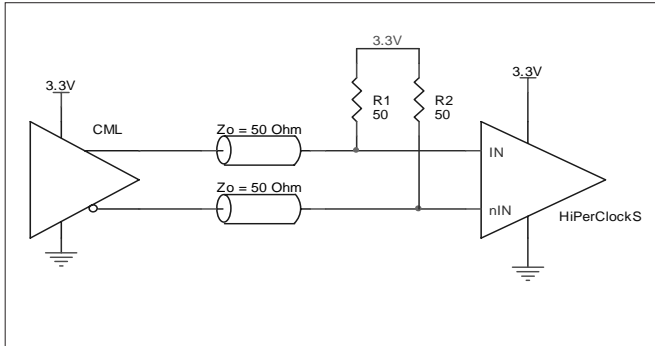
All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, we recommend that there is no trace attached.



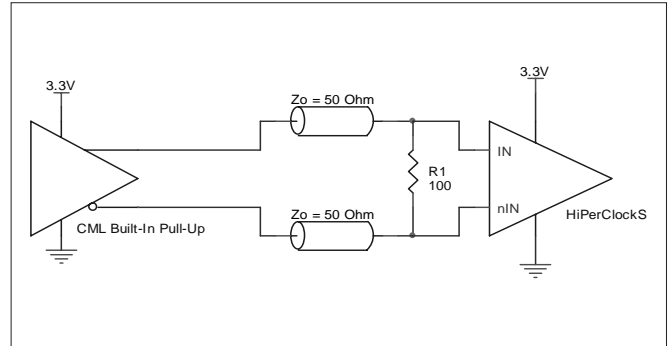
### DIFFERENTIAL CLOCK INPUT INTERFACE

The IN/nIN accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2D* show interface examples for the HiPerClockS IN/nIN input driven by the most common driver types. The input interfaces suggested here

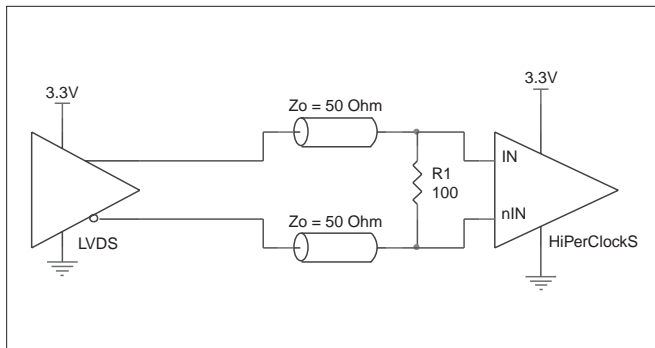
are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



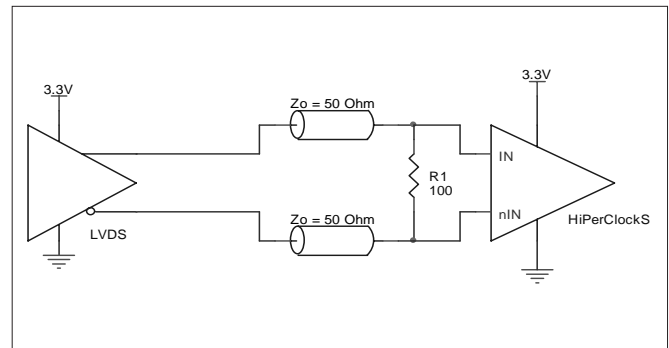
**FIGURE 2A. HiPerClockS IN/nIN INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**



**FIGURE 2B. HiPerClockS IN/nIN INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**



**FIGURE 2C. HiPerClockS IN/nIN INPUT DRIVEN BY A 3.3V LVPECL DRIVER**

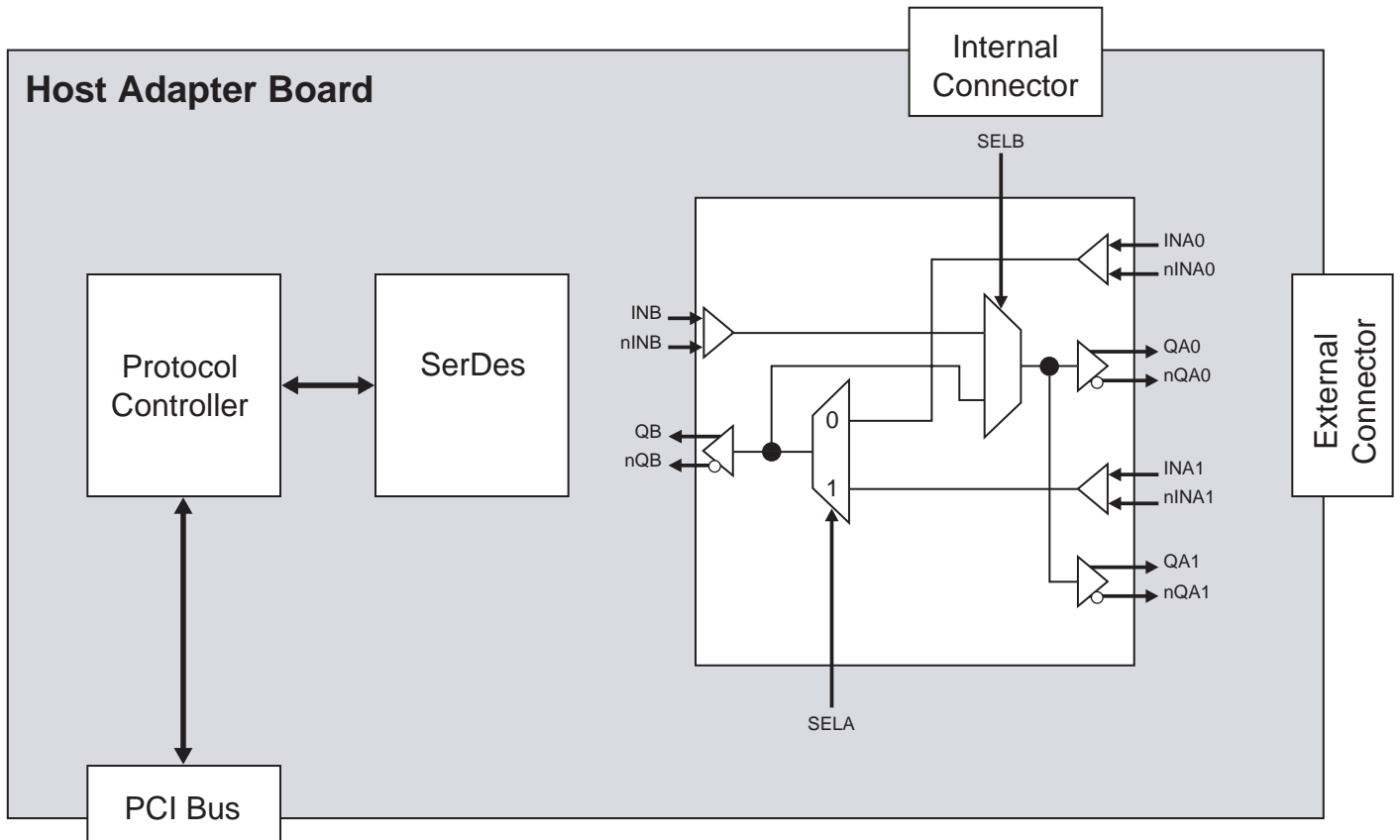


**FIGURE 2D. HiPerClockS IN/nIN INPUT DRIVEN BY A 3.3V LVDS DRIVER**



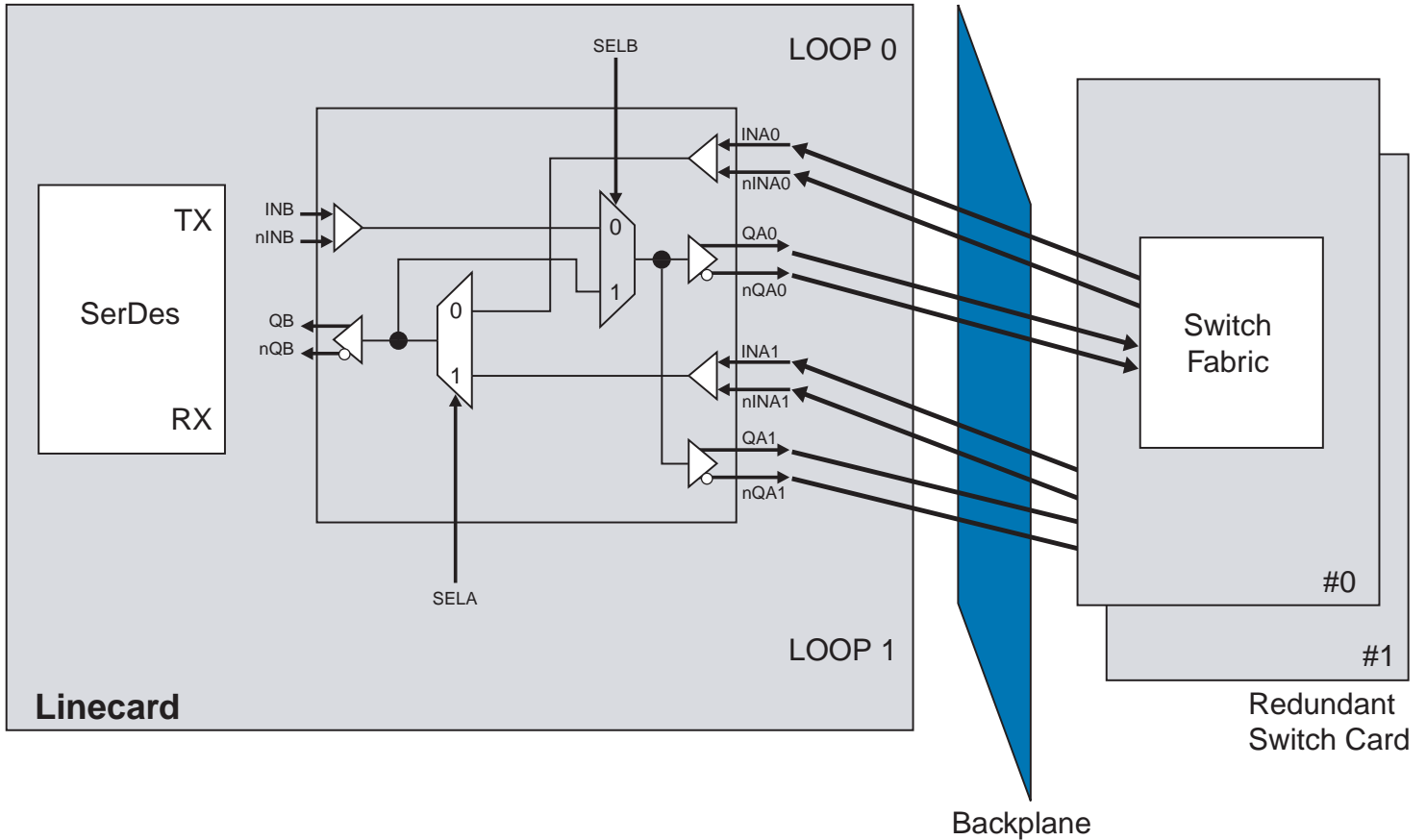


#### TYPICAL APPLICATION DIAGRAM FOR HOST BUS ADAPTER BOARDS FOR ROUTING BETWEEN INTERNAL AND EXTERNAL CONNECTORS



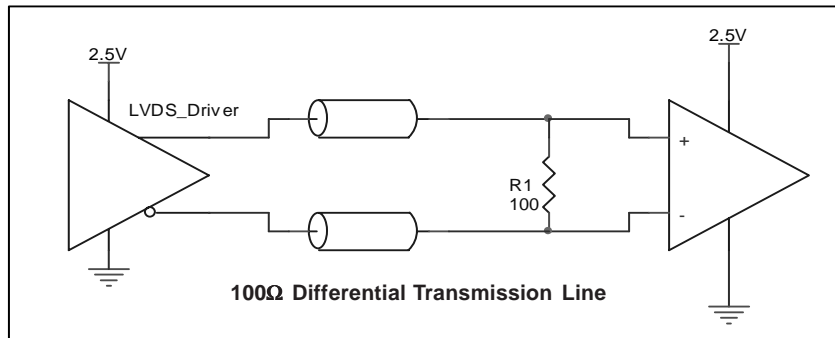


**TYPICAL APPLICATION DIAGRAM FOR HOT-SWAPPABLE LINKS TO REDUNDANT SWITCH FABRIC CARDS**



**2.5V LVDS DRIVER TERMINATION**

Figure 3 shows a typical termination for LVDS driver in transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.



**FIGURE 3. TYPICAL LVDS DRIVER TERMINATION**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85454-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85454-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 2.5V + 5\% = 2.625V$ , which gives worst case results.

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 90mA = 236.3mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow of and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.236W * 51.5^\circ C/W = 97.2^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 16-PIN VFQFN, FORCED CONVECTION**

$\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 16 LEAD VFQFN

$\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	0 51.5°C/W

### TRANSISTOR COUNT

The transistor count for ICS85454-01 is: 171



PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

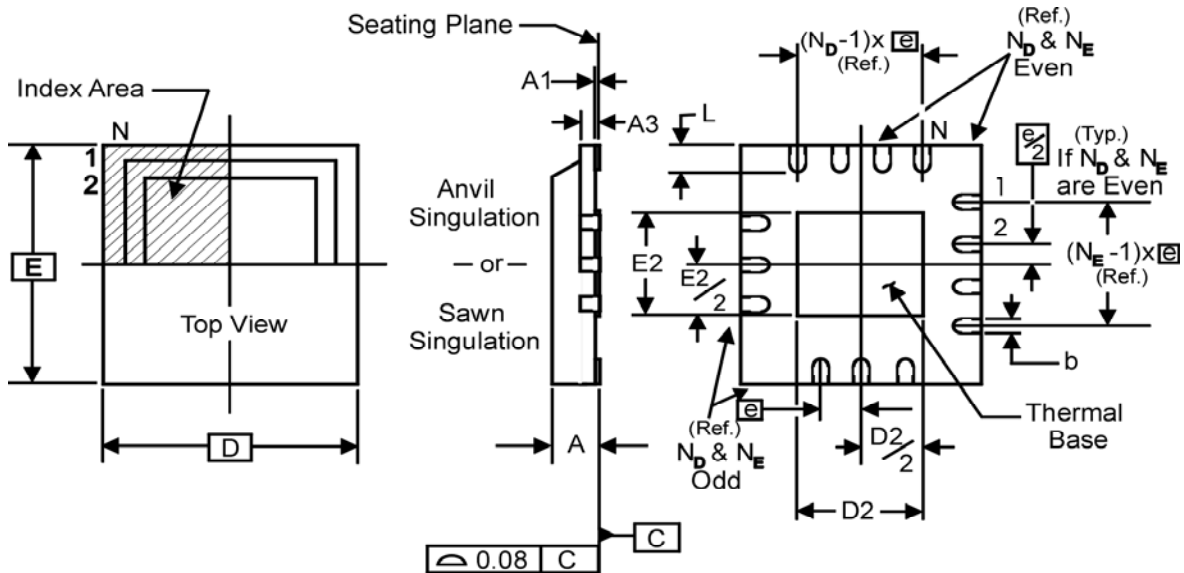


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
$N_D$	4	
$N_E$	4	
D	3.0	
D2	1.0	1.8
E	3.0	
E2	1.0	1.8
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220



Integrated  
Circuit  
Systems, Inc.

# ICS85454-01

DUAL 2:1/1:2  
DIFFERENTIAL-TO-LVDS MULTIPLEXER

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85454AK-01	5A01	16 Lead VFQFN	Tube	-40°C to 85°C
ICS85454AK-01T	5A01	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS85454AK-01LF	A01L	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
ICS85454AK-01LFT	A01L	16 Lead "Lead-Free" VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Systems, Inc.

**ICS85454-01**

DUAL 2:1/1:2

DIFFERENTIAL-TO-LVDS MULTIPLEXER

**REVISION HISTORY SHEET**

Rev	Table	Page	Description of Change	Date
B	T4D	4	LVDS DC Characteristics - changed $V_{OD}$ parameters. Changed $\Delta V_{OD}/V_{OS}$ parameters from typical to maximum.	3/14/06
	T9	14	Ordering Information - corrected Shipping Packaging from Tray to Tube.	
B	T8	13	Package Dimension Table - corrected D2/E2 from 0.25min/1.25max. to 1.0min./1.8max.	6/16/06