QUAD, 1-TO-1, DIFFERENTIAL-TO-2.5V, 3.3V, 5V LVPECL RECEIVER

ICS853017

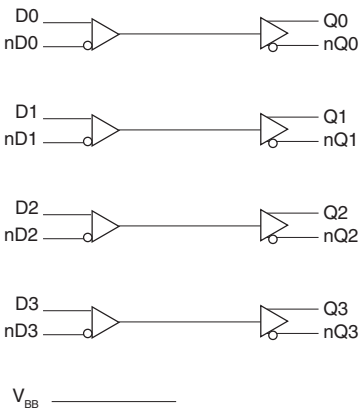
General Description

The ICS853017 is a quad 1-to-1, 2.5V/3.3V/5V differential LVPECL/ECL receiver and a member of the Hiperclocks™ family of High Performance Clock Solutions from IDT. The ICS853017 operates with a positive or negative power supply at 2.5V, 3.3V or 5V, and can accept both single-ended and differential inputs. For single-ended operation, an internally generated voltage, which is available on output pin V_{BB}, can be used as a switching bias voltage on the unused input of the differential pair. V_{BB} can also be used to rebias AC coupled inputs.

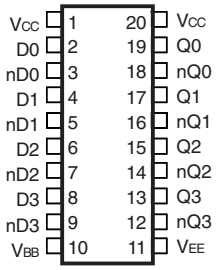
Features

- Four differential LVPECL / ECL 1:1 receivers
- Four differential LVPECL clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2GHz (typical)
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx input
- Output skew: TBD
- Part-to-part skew: TBD
- Propagation delay: 320ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 5.25V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -5.25V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS853017
20-Lead, 300-MIL SOIC
7.5mm x 12.8mm x 2.3mm body package
M Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 20	V_{CC}	Power		Core supply pins.
2	D0	Input	Pulldown	Non-inverting differential clock input.
3	nD0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
4	D1	Input	Pulldown	Non-inverting differential clock input.
5	nD1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
6	D2	Input	Pulldown	Non-inverting differential clock input.
7	nD2	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
8	D3	Input	Pulldown	Non-inverting differential clock input.
9	nD3	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
10	V_{BB}	Power		Bias Voltage.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
D0:D3	nD0:nD3	Q0:Q3	nQ0:nQ3,		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

Absolute Maximum Ratings

Supply Voltage, V_{CC}	5.5V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-5.5V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sing/Source, I_{BB}	± 0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	46.2°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 5.25V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	3.3	5.25	V
I_{EE}	Power Supply Current			46		mA

Table 4B. LVPECL DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			2.275			2.295			2.33		V
V_{OL}	Output Low Voltage; NOTE 1			1.545			1.52			1.535		V
V_{IH}	Input High Voltage, Single-Ended		2.075			2.075			2.075			V
V_{IL}	Input Low Voltage, Single-Ended		1.43			1.43			1.43			V
V_{BB}	Output Voltage Reference; NOTE 2		1.86			1.86			1.86			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1, nD2, nD3			200			200			200	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1, nD2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			1.475			1.495			1.53		V
V_{OL}	Output Low Voltage; NOTE 1			0.745			0.72			0.735		V
V_{IH}	Input High Voltage, Single-Ended		1.275			1.275			1.275			V
V_{IL}	Input Low Voltage, Single-Ended		0.63			0.63			0.63			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1, nD2, nD3			200			200			200	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1, nD2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			3.975			3.995			4.03		V
V_{OL}	Output Low Voltage; NOTE 1			3.245			3.22			3.235		V
V_{IH}	Input High Voltage, Single-Ended		3.775			3.775			3.775			V
V_{IL}	Input Low Voltage, Single-Ended		3.13			3.13			3.13			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		5	1.2		5	1.2		5	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1, nD2, nD3			200			200			200	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1, nD2, nD3	-200			-200			-200			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4C. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			-1.025			-1.005			-0.97		V
V_{OL}	Output Low Voltage; NOTE 1			-1.755			-1.78			-1.765		V
V_{IH}	Input High Voltage, Single-Ended		-1.225			-1.225			-1.225			V
V_{IL}	Input Low Voltage, Single-Ended		-1.87			-1.87			-1.87			V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44			-1.44			-1.44			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	D0:D3, nD0:nD3			200			200			200	µA
I_{IL}	Input Low Current	D0:D3	-10			-10			-10			µA
		nD0:nD3	-200			-200			-200			µA

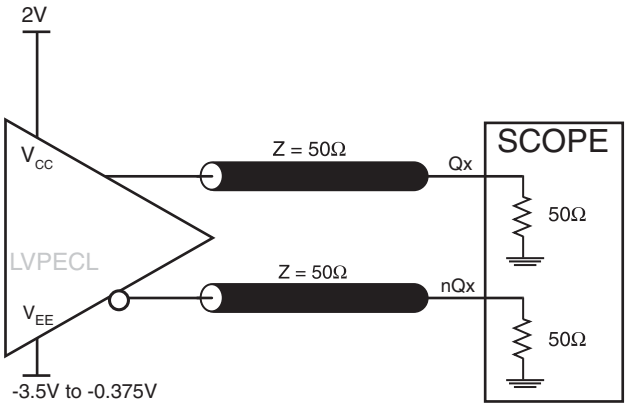
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V OR V_{CC} = 2.375V TO 5.25V; V_{EE} = 0V

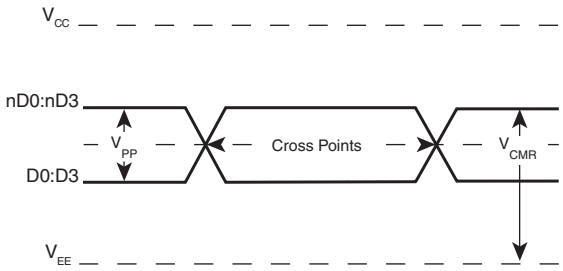
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>2			>2			>2		GHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			320			320			320		ps
tp_{HL}	Propagation Delay, High-to-Low; NOTE 1			320			320			320		ps
*t*sk(o)	Output Skew; NOTE 2, 4			TBD			TBD			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD			TBD			TBD		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		175			175			175		ps

All parameters tested ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

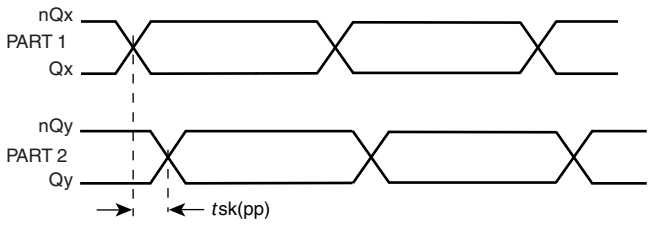
PARAMETER MEASUREMENT INFORMATION



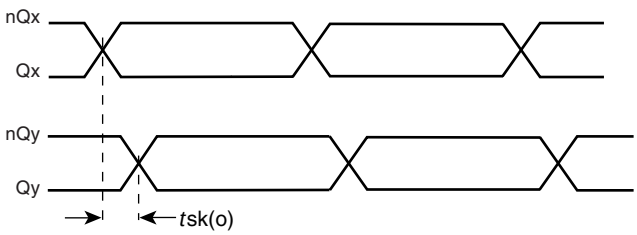
OUTPUT LOAD AC TEST CIRCUIT



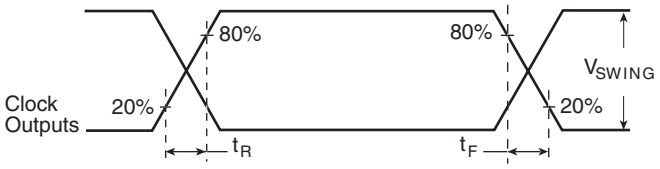
DIFFERENTIAL INPUT LEVEL



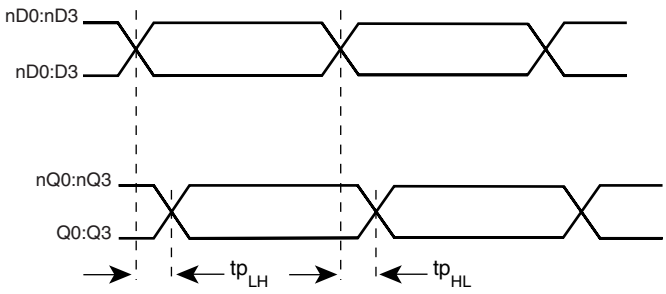
PART-TO-PART SKEW



OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

Dx Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the Dx input to ground.

OUTPUTS:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≃ V_{cc}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

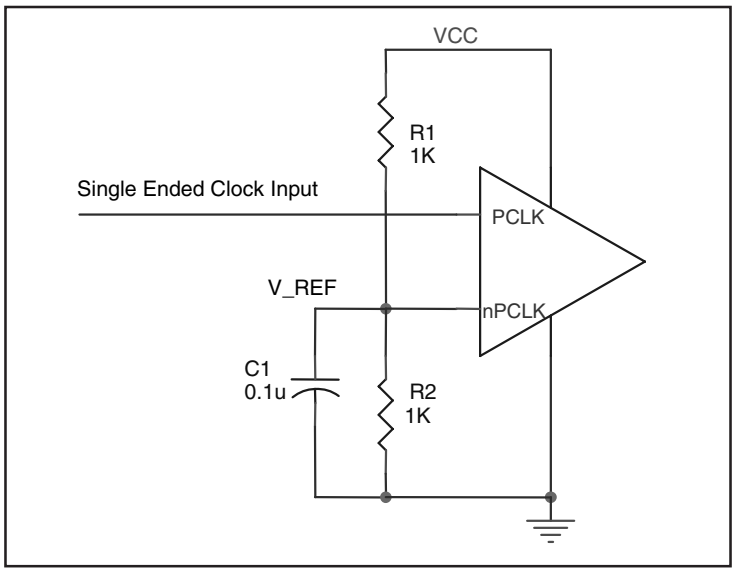


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LVPECL Clock Input Interface

The PCLKx /nPCLKx accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLKx/nPCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

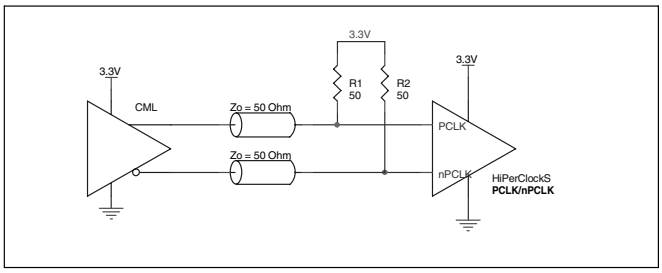


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver

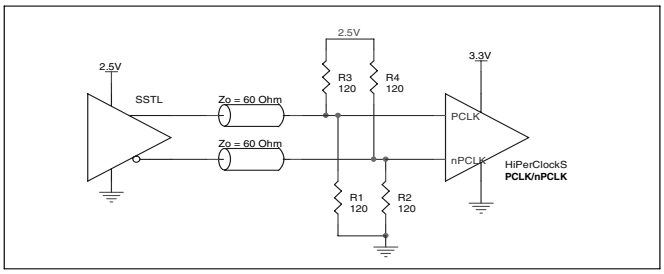


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

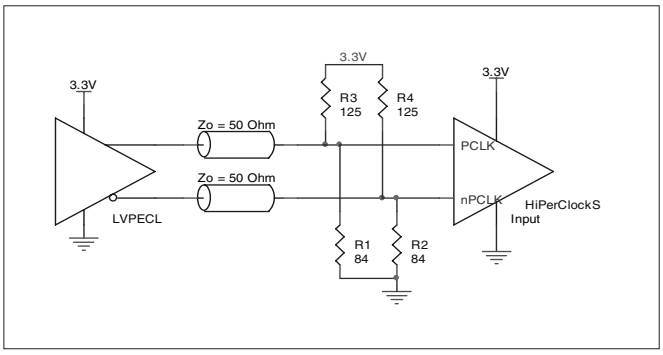


Figure 2C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

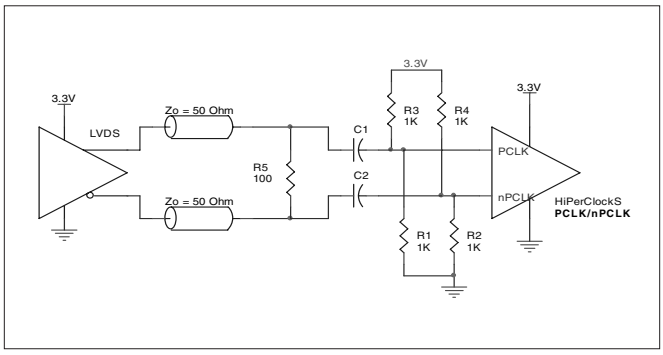


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

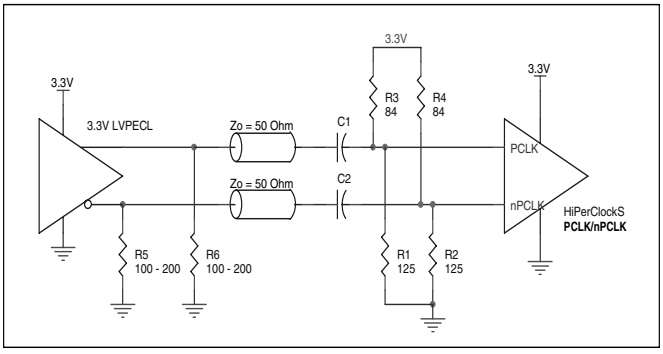


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

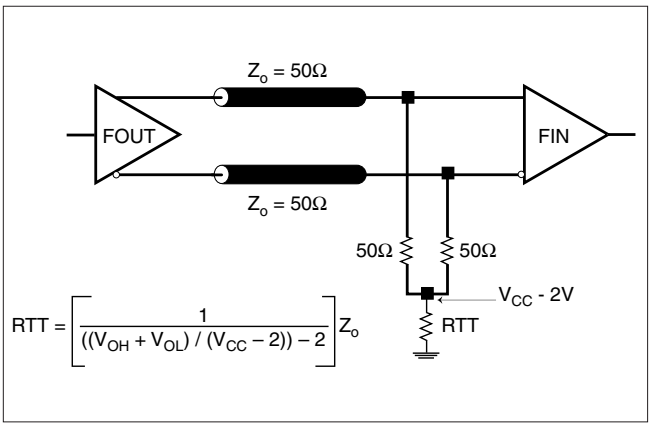


FIGURE 3A. LVPECL OUTPUT TERMINATION

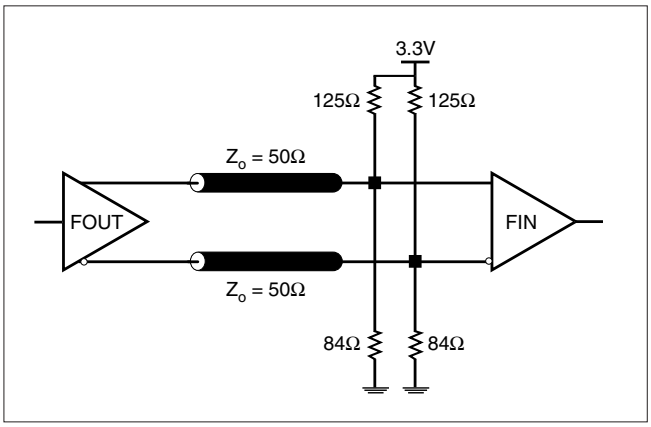


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 5V LVPECL OUTPUT

This section shows examples of 5V LVPECL output termination. *Figure 4A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to V_{CC} - 2V = 3V at the receiver. *Figure 4B* shows Thevenin equivalence of Figure 4A. In actual application where the 3V DC power supply is not available, this approached is normally used.

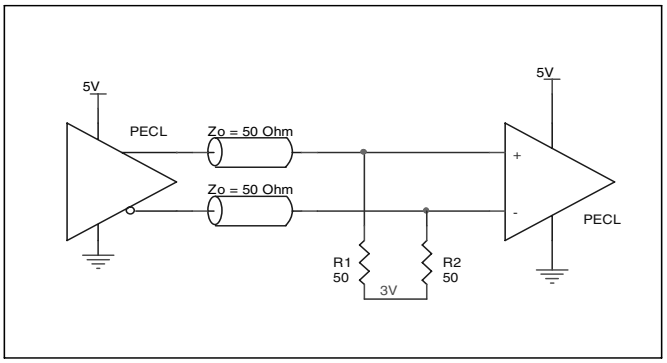


FIGURE 4A. STANDARD 5V LVPECL OUTPUT TERMINATION

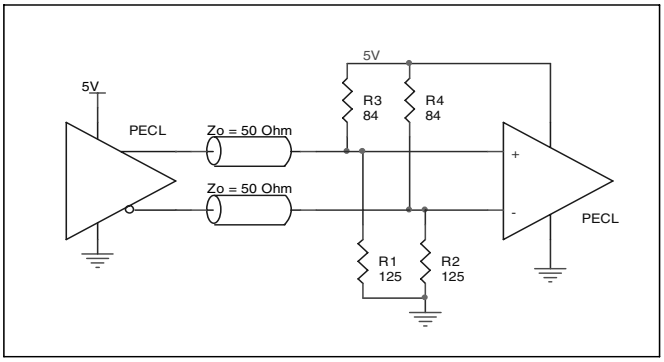


FIGURE 4B. 5V LVPECL OUTPUT TERMINATION EXAMPLE

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

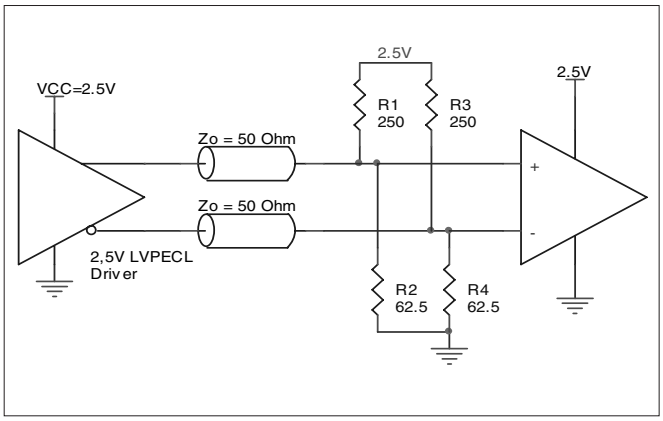


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

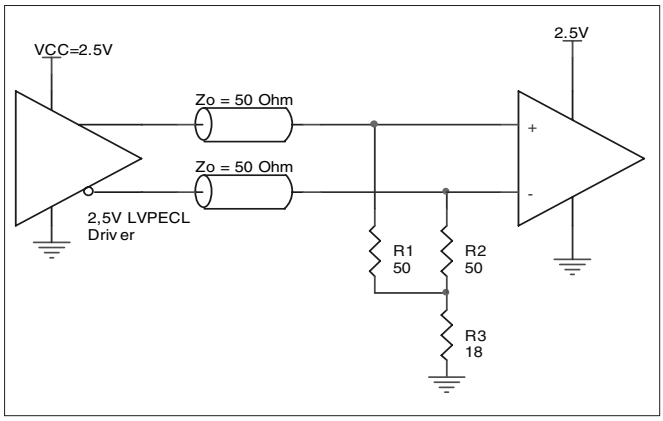


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

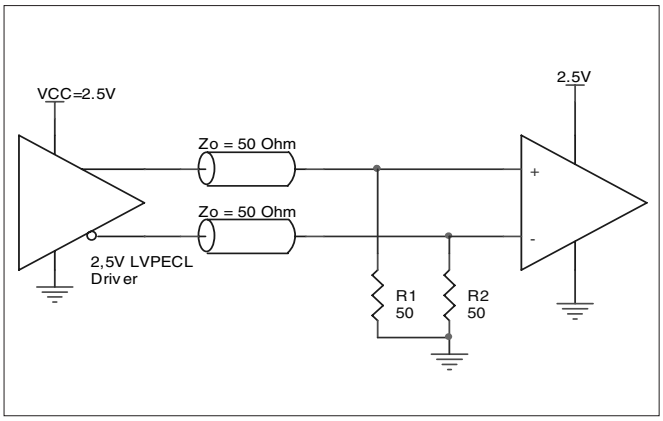


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853017.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853017 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 5.5V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 5.5V * 46mA = **253mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.94mW = **123.76mW**

  Total Power$_{\_MAX}$ (5.5V, with all outputs switching) = 123.76mW + 253mW = **376.76mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.377W * 46.2°C/W = 102.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN SOIC, FORCED CONVECTION

	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 6.

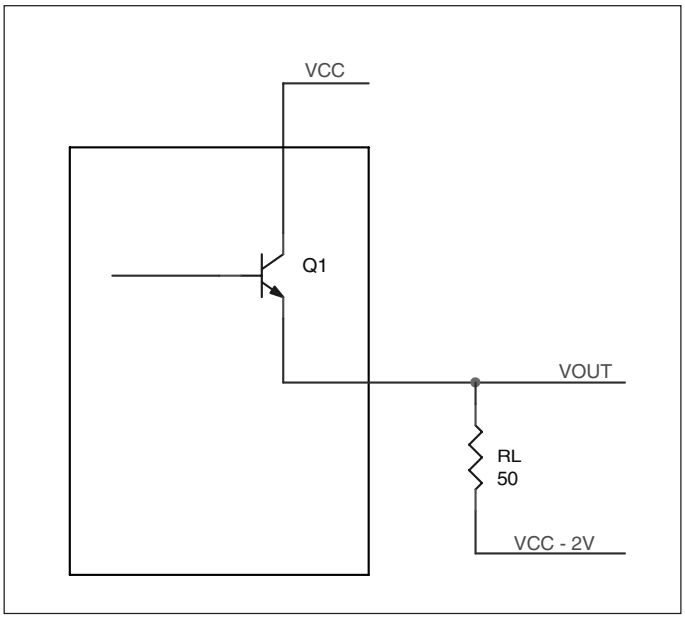


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} – 1.67V$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853017 is: 187

Pin compatible with MC100EP58

PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

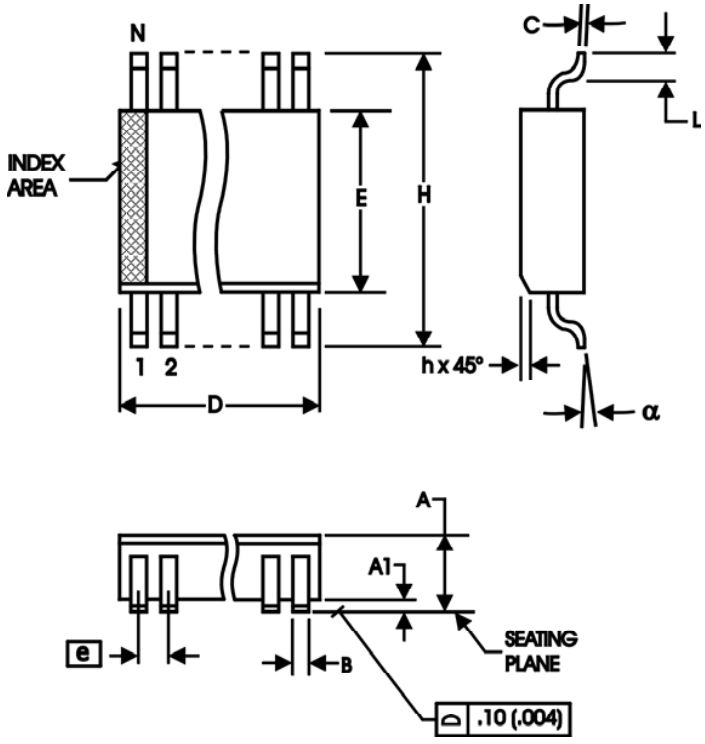


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853017AM	ICS853017AM	20 lead SOIC	tube	-40°C to 85°C
ICS853017AMT	ICS853017AM	20 lead SOIC	1000 tape & reel	-40°C to 85°C
ICS853017AMLF	TBD	20 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS853017AMLFT	TBD	20 lead "Lead-Free" SOIC	1000 tape & reel	-40°C to 85°C

Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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