FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20206-5E

Semicustom

CMOS

Standard cell

CS81 Series

■ DESCRIPTION

The CS81 series 0.18 μm CMOS standard cell is a line of highly integrated CMOS ASICs featuring high speed and low power consumption.

This series incorporates up to 40 million gates which have a gate delay time of 11 ps, resulting in both integration and speed about three times higher than conventional products.

In addition, CS81 can operate at a power-supply voltage of down to 1.1 V, substantially reducing power consumption.

■ FEATURES

- Technology : 0.18 μm silicon-gate CMOS, 3- to 6-layer wiring capable of integrating a mixture of high-speed processes and cells on a single chip (under development)
- Supply voltage : +1.8 V ± 0.15 V (normal) to +1.1 V ± 0.1 V
- Junction temperature range : –40 to +125 °C
- Gate delay time : t_{pd} = 11 ps (1.8 V, inverter, F/O = 1)
- Gate power consumption : P_d = 5 nW/MHz/BC (1.1 V, 2-NAND, F/O = 1)
- Support for high speed (62.2 Mbps to 780 Mbps, 2.5 Gbps to 3.125 Gbps) interface macros for transmission
- Output buffer cells with noise reduction circuits
- Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells
- Buffer cells dedicated to crystal oscillators
- Special interfaces (P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others. including those under development)
- IP macros (CPU (FR, ARM7, ARM9), DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others. including those under development)
- Capable of incorporating compiled cells (RAM/ROM/multiplier, and others.)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using a timing driven layout tool
- Support for static timing sign-off
  Dramatically reducing the time for generating test vectors for timing verification and the simulation time

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- Hierarchical design environment for supporting large-scale circuits
- Simulation (before layout) considering the input slew rate and detailed RC delay calculation (after layout) , supporting development with minimized timing trouble after trial manufacture
- Support for memory (RAM/ROM) SCAN
- Support for memory (RAM) BIST
- Support for boundary SCAN
- Support for path delay test
- A variety of package options (TQFP, HQFP, EBGA, FBGA, TAB-BGA, FCBGA, LQFP)

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells (about 400 types)

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- SCAN Flip Flop
- ENOR
- AND-OR
- Decoder
- Non-SCAN Flip Flop
- Inverter
- Buffer
- OR-AND
- OR-AND Inverter
- OR
- Selector
- BUS Driver
- EOR
- Others

2. IP macros

CPU/DSP	FR, SPARClite, ARM7, ARM9, Communications DSP, DSP for AV and others
High speed interface macros	622 Mbps to 780 Mbps, 2.5 Gbps to 3.125 Gbps
Interface macro	PCI, IEEE1394, USB, IrDA, and others
Multimedia processing macros	JPEG, MPEG, and others
Mixed signal macros	ADC, DAC, OPAMP, and others
Compiled macros	RAM, ROM, multiplier, adder, multiplier-accumulator, and others
PLL	Analog PLL, digital PLL

3. Special I/O interface macros

- T-LVTTL
- LVDS
- IEEE1394
- SSTL
- PCI
- SDRAM-I/F
- HSTL
- AGP
- P-CML
- USB

■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS81 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 RW)

• High density type/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

• High speed type

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 144 K	64 to 2 K	4 to 72	bit

• Large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	24.5 K to 1179 K	4 K to 16 K	6 to 72	bit

2. Clock synchronous dual-port RAM (2 addresses : 1 RW, 1 R)

• High density type/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

3. Clock synchronous register file (3 addresses : 1 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64	1 to 72	bit

4. Clock synchronous register file (4 addresses : 2 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64	1 to 72	bit

5. Clock synchronous ROM (1 addresses, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 512 K	128 to 4 K	2 to 128	bit

6. Clock synchronous delay line memory (2 addresses : 1 W, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 32 K	32 to 1 K	8 to 32	bit
16	384 to 32 K	64 to 2 K	6 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage*1	V_{DD}	−0.5	+2.5*2	V
			+4.0*3	
Input voltage*1	V_I	−0.5	V_{DD}+0.5 (≤ 2.5 V) *2	V
			V_{DD}+0.5 (≤ 4.0 V) *3	
Output voltage*1	V_O	−0.5	V_{DD}+0.5 (≤ 2.5 V) *2	V
			V_{DD}+0.5 (≤ 4.0 V) *3	
Storage temperature	Tst	−55	+125	°C
Junction temperature	T_j	−40	+125	°C
Output current*4	I_O	—	±4	mA
Input signal transmitting rate	R_I	—	Clock input*5 : 200 Normal input : 100	Mbps*6
Output signal transmitting rate	R_O	—	100	Mbps*6
Output load capacitance	C_O	—	3000/R_O	pF
Supply pin current	I_D	—	*7	mA

*1 : V_{SS} = 0 V

*2 : Internal gate part in case of single power supply or dual power supply

*3 : I/O part in case 3.3 V I/F or 2.5 V I/F is used by dual power supply.

*4 : DC current which continues more than 10 ms, or average DC current

*5 : in case of I/O cell for clock input

*6 : bps = bit per second

*7 : Supply pin current for one V_{DD}/GND pin

Frame	Source type	Maximum current [mA]		Number of layer
		Standard source	Additional source	
YS, YI	V_{DDE}, V_{DDI}, V_{DD}, V_{SS}	68	68	4, 5
	V_{DDE}	39	39	3
	V_{DDI}, V_{DD}, V_{SS}	68	68	
B	V_{DDE}, V_{DDI}, V_{DD}, V_{SS}	43	30	—

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

- **Single power supply (V_{DD} = +1.8 V ± 0.15 V)**

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage (1.8 V supply voltage)	V_{DD}	1.65	1.8	1.95	V
"H" level input voltage (1.8 V CMOS)	V_{IH}	V_{DD} × 0.65	—	V_{DD} + 0.3	V
"L" level input voltage (1.8 V CMOS)	V_{IL}	–0.3	—	V_{DD} × 0.35	V
Junction temperature	T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = +3.3 V ± 0.3 V, V_{DDI} = +1.8 V ± 0.15 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage	1.8 V supply voltage	V_{DDI}	1.65	1.8	1.95	V
	3.3 V supply voltage	V_{DDE}	3.0	3.3	3.6	
"H" level input voltage	1.8 V CMOS	V_{IH}	V_{DDI} × 0.65	—	V_{DDI} + 0.3	V
	3.3 V CMOS		2.0	—	V_{DDE} + 0.3	
"L" level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	V_{DDI} × 0.35	V
	3.3 V CMOS		–0.3	—	+0.8	
Junction temperature		T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = +3.3 V ± 0.3 V, V_{DDI} = +1.5 V ± 0.1 V / +1.1 V ± 0.1 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.0	1.1	1.2	V
			1.4	1.5	1.6	V
"H" level input voltage	3.3 V CMOS	V_{IH}	2.0	—	V_{DDE} + 0.3	V
"L" level input voltage	3.3 V CMOS	V_{IL}	–0.3	—	+0.8	V
Junction temperature		T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = +2.5 V ± 0.2 V, V_{DDI} = +1.8 V ± 0.15 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	1.65	1.8	1.95	V
"H" level input voltage	1.8 V CMOS	V_{IH}	$V_{DDI} \times 0.65$	—	$V_{DDI} + 0.3$	V
	2.5 V CMOS		1.7	—	$V_{DDE} + 0.3$	V
"L" level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	$V_{DDI} \times 0.35$	V
	2.5 V CMOS		–0.3	—	+0.7	V
Junction temperature		T_j	–40	—	+125	°C

- **Dual power supply (V_{DDE} = +2.5 V ± 0.2 V, V_{DDI} = +1.5 V ± 0.1 V / +1.1 V ± 0.1 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	1.0	1.1	1.2	V
			1.4	1.5	1.6	V
"H" level input voltage	2.5 V CMOS	V_{IH}	1.7	—	$V_{DDE} + 0.3$	V
"L" level input voltage	2.5 V CMOS	V_{IL}	–0.3	—	+0.7	V
Junction temperature		T_j	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC characteristics

- **Signal power supply** : V_{DD} = **1.8 V**

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply Current	I_{DDS}	—	—	—	*	mA
"H" level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = +100 µA	0	—	0.2	V
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	Pull up V_{IL} = 0 Pull down V_{IH} = V_{DD}	—	18	—	kΩ

* : For details of YS, YI, B frame of CS81 series, contact Fujitsu.

- **Dual power supply** : V_{DDE} = **3.3 V**, V_{DDI} = **1.8 V**
  (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V / 1.5 V ± 0.1 V / 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply Current	I_{DDS}	—	—	—	*1	mA
"H" level output voltage	V_{OH4}	3.3 V Output I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL4}	3.3 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	V
"H" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V	*2			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	—			—
"L" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V	*2			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	—			—
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	1.8 V Pull up V_{IL}=0 Pull down V_{IH}=V_{DDI}	—	18	—	kΩ
		3.3 V Pull up V_{IL}=0 Pull down V_{IH}=V_{DDE}	10	33	80	

*1 : For details of YS, YI, B frame of CS81 series, contact Fujitsu.

*2 : Refer to the Fig.1 to 2.

- **Dual power supply** : V_{DDE} = **2.5 V**, V_{DDI} = **1.8 V** / **1.5 V** / **1.1 V**
  (V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.8 V ± 0.15 V / 1.5 V ± 0.1 V / 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply Current	I_{DDS}	—	—	—	*	mA
"H" level output voltage	V_{OH3}	2.5 V Output I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL3}	2.5 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	V
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	2.5 V Pull up V_{IL}=0 Pull down V_{IH}=V_{DDE}	—	25	—	kΩ
		1.8 V Pull up V_{IL}=0 Pull down V_{IH}=V_{DDI}	—	18	—	

* : For details of YS, YI, B frame of CS81 series, contact Fujitsu.

• **V-I Characteristics**

Conditions (Fig 1, 2) Min : Process = Slow, T_j = +125 °C, V_{DD} = 3.6 V
Typ : Process = TYPICAL, T_j = +25 °C, V_{DD} = 3.3 V
Max : Process = FAST, T_j = –40 °C, V_{DD} = 3.0 V

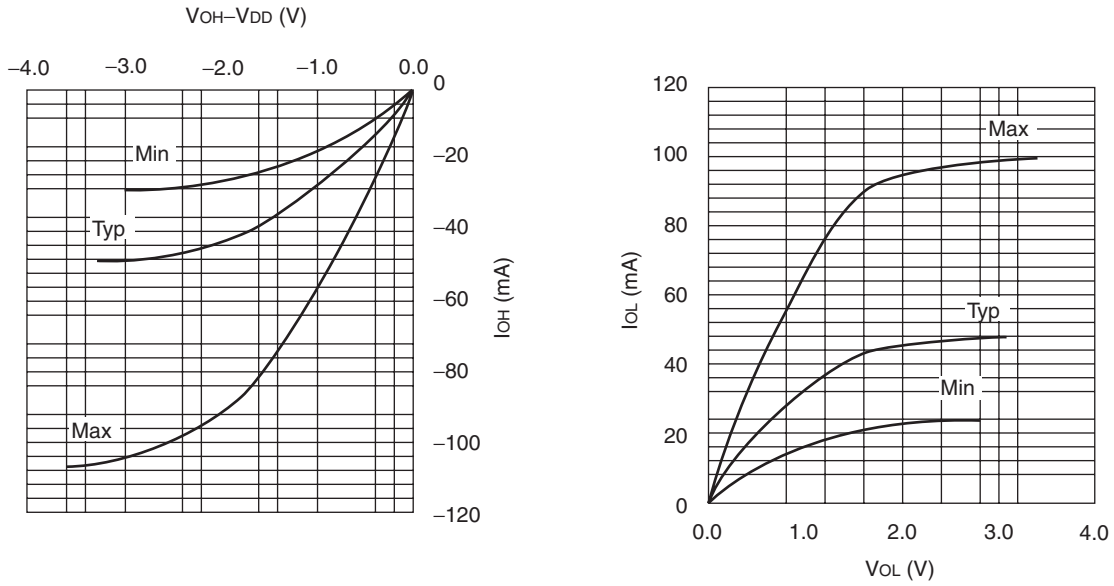

Fig.1 V-I characteristics (3.3 V normal I/O L, M type)

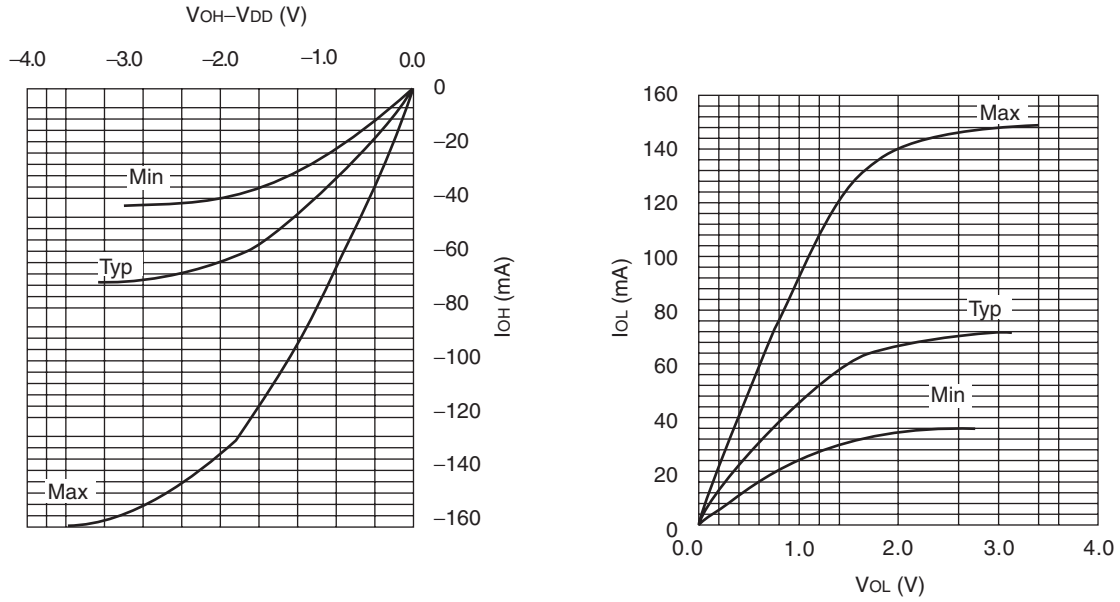

Fig.2 V-I characteristics (3.3 V normal I/O H, V type)

2. AC characteristics

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max*	
Delay time	t_{pd}*1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

*1 : Delay time = propagation delay time, enable time, disable time

*2 : “typ” is calculated based on the cell specifications.

*3 : Measurement conditions.

Measurement condition	tmin	ttyp	tmax
V_{DD} = 1.8 V±0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.64	1.00	1.58
V_{DD} = 1.5 V±0.10 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.83	1.31	2.05
V_{DD} = 1.1 V±0.10 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	1.37	2.45	4.88

Note : $t_{pd\ max}$ is calculated according to the maximum junction temperature (T_j) .

■ INPUT/OUTPUT PIN CAPACITANCE

(T_j = +25 °C, V_{DD} = V_I = 0 V, f = 1 MHz)

Parameter	Symbol	Requirements	Unit
Input pin	C_{IN}	Max 16	pF
Output pin	C_{OUT}	Max 16	pF
I/O pin	$C_{I/O}$	Max 16	pF

Note : Capacitance varies according to the package and the location of the pin.

■ DESIGN METHOD

SCCAD2 is the standard cell integrated design environment providing three major functions, enabling high-quality, large-scale system LSIs to be developed in a shorter period of time. They include: the timing driven layout function for automatic placement/routing based on timing constraints to prevent timing problems after layout, the function for shortening the development cycle time by dividing a large-scale circuit and performing simultaneous logical/physical design of multiple circuits, and the function for automatically generating power/signal wiring patterns while evaluating the supply voltage drop, signal noise, delay penalty, and crosstalk (Contact your nearest Fujitsu office for more information and availability).

■ PACKAGES

The table below lists the package types available.

Consult Fujitsu for the combination of each package and the time of availability.

Package	Pin count	Material
TAB-BGA	304 352 480 560 660 720	Plastic Plastic Plastic Plastic Plastic Plastic
EBGA	576 660 672	Plastic Plastic Plastic
HQFP	208 240 256 304	Plastic Plastic Plastic Plastic
TQFP	100 120	Plastic Plastic
LQFP	144 176 208	Plastic Plastic Plastic
FBGA	288	Plastic
FCBGA	1089 1225 1369 1681 1849 2116	Plastic Plastic Plastic Plastic Plastic Plastic

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