



A5N:3000.XXH

VOLTAGE RATINGS

Part Number	V _{RRM} , V _R (V) Max. rep. peak reverse voltage		V _{RSM} , V _R (V) Max. non-rep. peak reverse voltage
	T _J = 0 to 125°C	T _J = -40 to 0°C	
	T _J = 25 to 125°C		
A5N:3000.16H	1600	1600	1700
A5N:3000.18H	1800	1800	1900
A5N:3000.20H	2000	2000	2100
A5N:3000.22H	2200	2200	2300

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T _J Junction Temperature	-40 to 125	°C	-
T _{stg} Storage Temperature	-40 to 150	°C	-
I _{F(AV)} Max. Av. current @ Max. T _C	3000	A	180° half sine wave
	70	°C	
I _{F(RMS)} Nom. RMS current	4700	A	-
I _{FSM} Max. Peak non-rep. surge current	53.3	KA	50 Hz half cycle sine wave Initial T _J = 125°C, rated V _{RRM} applied after surge.
	56		60 Hz half cycle sine wave
	63.3		50 Hz half cycle sine wave Initial T _J = 125°C, no voltage applied after surge.
	66.5		60 Hz half cycle sine wave
I ² t Max. I ² t capability	12020	kA ² s	t = 10ms Initial T _J = 125°C, rated V _{RRM} applied after surge.
	13065		t = 8.3 ms
	16992		t = 10ms Initial T _J = 125°C, no voltage applied after surge.
	18470		t = 8.3 ms
I ² t ^{1/2} Max. I ² t ^{1/2} capability	202350	kA ² s ^{1/2}	Initial T _J = 125°C, no voltage applied after surge. I ² t for time t _x = I ² t ^{1/2} * t _x ^{1/2} . (0.1 < t _x < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	800	A/μs	T _J = 125°C, V _D = V _{DRM} , I _{TM} = 1600A. Gate pulse: 20V, 20Ω, 10μs, 0.5μs rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P _{GM} Max. Peak gate power	16	W	t _p < 5 ms
P _{G(AV)} Max. Av. gate power	3.0	W	-
+I _{GM} Max. Peak gate current	4	A	t _p < 5 ms
-V _{GM} Max. Peak negative gate voltage	15	V	-
F Mounting Force	4550	N.m	Non lubricated threads



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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	1.54	1.62	V	Initial $T_J = 25^\circ\text{C}$, 50-60Hz half sine, $I_{peak} = 9425\text{A}$.
$V_{T(TO)1}$ Low-level threshold	---	---	0.921	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$
$V_{T(TO)2}$ High-level threshold	---	---	0.737		
r_{T1} Low-level resistance	---	---	0.079	m Ω	Use low values for $I_{TM} < \pi$ rated $I_{T(AV)}$
r_{T2} High-level resistance	---	---	0.063		
I_L Latching current	---	270	---	mA	$T_C = 25^\circ\text{C}$, 12V anode. Gate pulse: 10V, 20 Ω , 100 μs .
I_H Holding current	---	100	500	mA	$T_C = 25^\circ\text{C}$, 12V anode. Initial $I_T = 10\text{A}$.
t_d Delay time	---	0.5	1.5	μs	$T_C = 25^\circ\text{C}$, $V_D =$ rated V_{DRM} , 50A resistive load. Gate pulse: 10V, 20 Ω , 10 μs , 1 μs rise time.
t_q Turn-off time	---	---	100	μs	$T_J = 125^\circ\text{C}$, $I_{TM} = 500\text{A}$, $di/dt = 25\text{A}/\mu\text{s}$, $V_R = 50\text{V}$. $dv/dt = 200\text{V}/\mu\text{s}$ lin. To 80% rated V_{DRM} . Gate: 0V, 100 Ω .
dv/dt Critical rate-of-rise of off-state voltage	500	700	---	V/ μs	$T_J = 125^\circ\text{C}$. Exp. to 100% or lin. Higher dv/dt values To 80% V_{DRM} , gate open. available.
	1000	---	---		$T_J = 125^\circ\text{C}$, Exp. To 67% V_{DRM} , gate open.
I_{RM} , I_{DM} Peak reverse and off-state current	---	80	200	mA	$T_J = 125^\circ\text{C}$, Rated V_{RRM} and V_{DRM} , gate open.
I_{GT} DC gate current to trigger	---	---	500	mA	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
	75	150	250		
V_{GT} DC gate voltage to trigger	---	---	3.3	V	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$
	---	1.2	2.5		
V_{GD} DC gate voltage not to trigger	---	---	0.3	V	$T_C = 25^\circ\text{C}$, Max. Value which will not trigger with rated V_{DRM} anode-to-cathode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.011	$^\circ\text{C}/\text{W}$	DC operation.
	---	---	0.012	$^\circ\text{C}/\text{W}$	180 $^\circ$ sine wave, double side coolde.
	---	---	0.013	$^\circ\text{C}/\text{W}$	120 $^\circ$ rectangular wave, double side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.006	$^\circ\text{C}/\text{W}$	Mtg. Surface smooth, flat and greased.
wt Weight	---	1590 (56)	---	g(oz.)	---
Case Style	TO-200AE			JEDEC	---

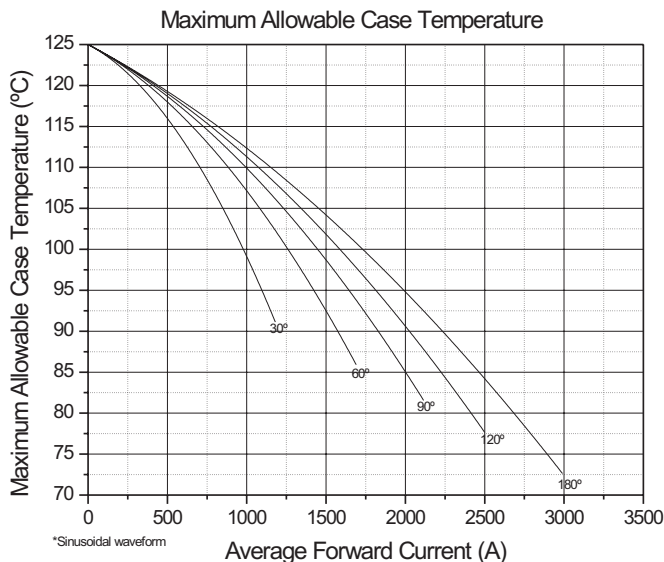


Fig. 1 - Current Ratings Characteristics

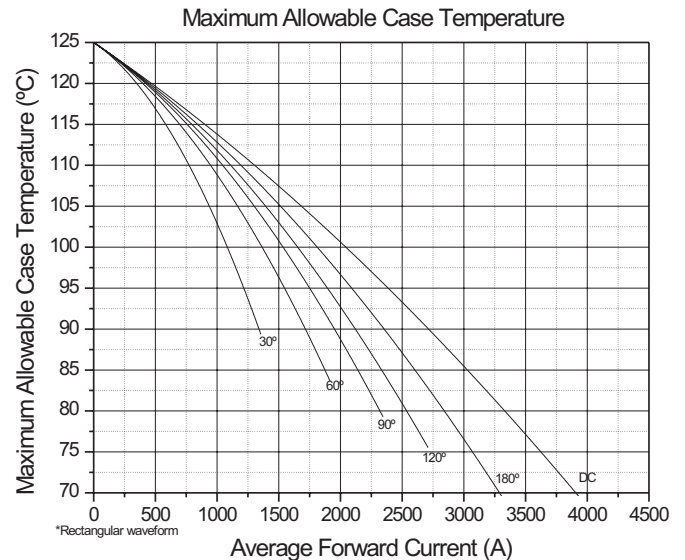


Fig. 2 - Current Ratings Characteristics



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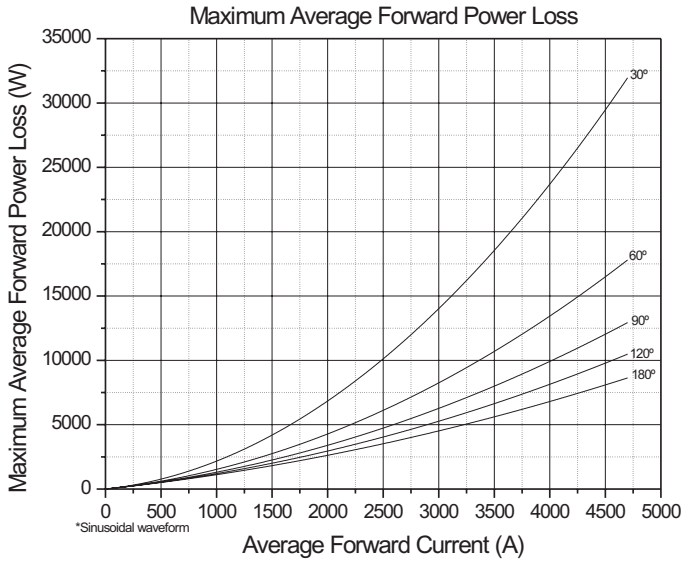


Fig. 3 - Forward Power Loss Characteristics

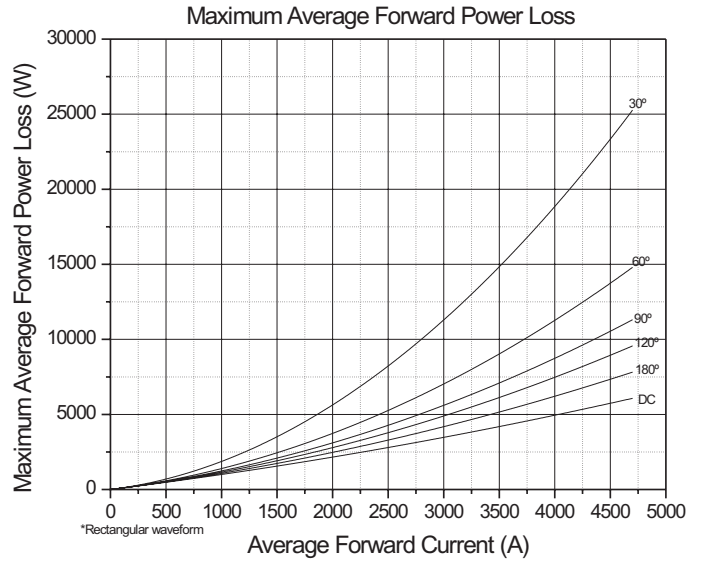


Fig. 4 - Forward Power Loss Characteristics

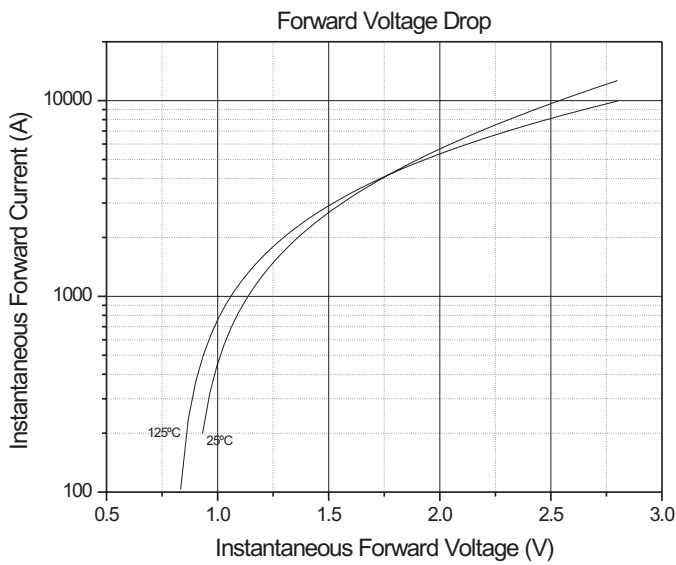


Fig. 5 - Forward Voltage Drop Characteristics

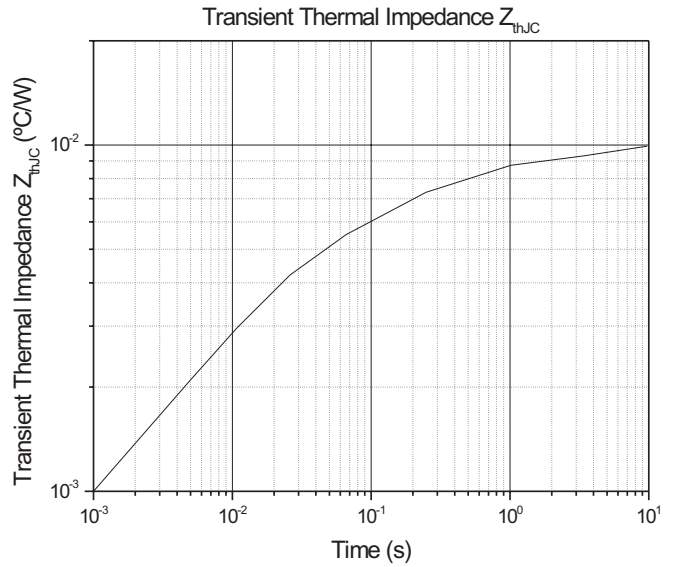


Fig. 6 - Transient Thermal Impedance Characteristics



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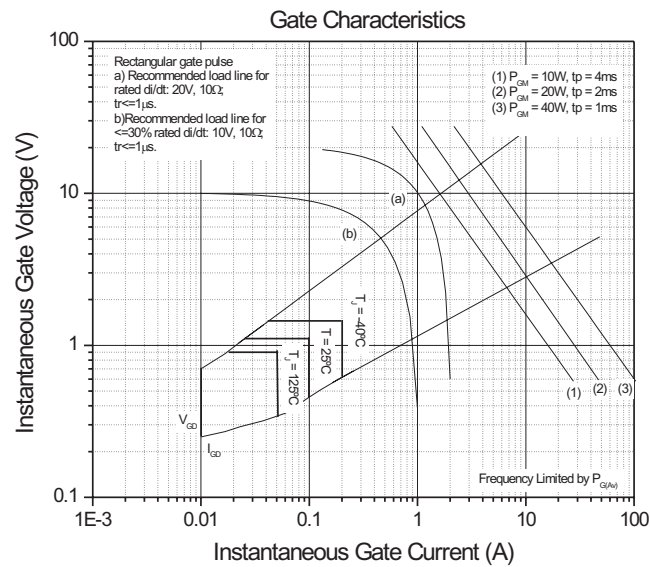


Fig. 7 - Gate Trigger Characteristics

TO-200AE

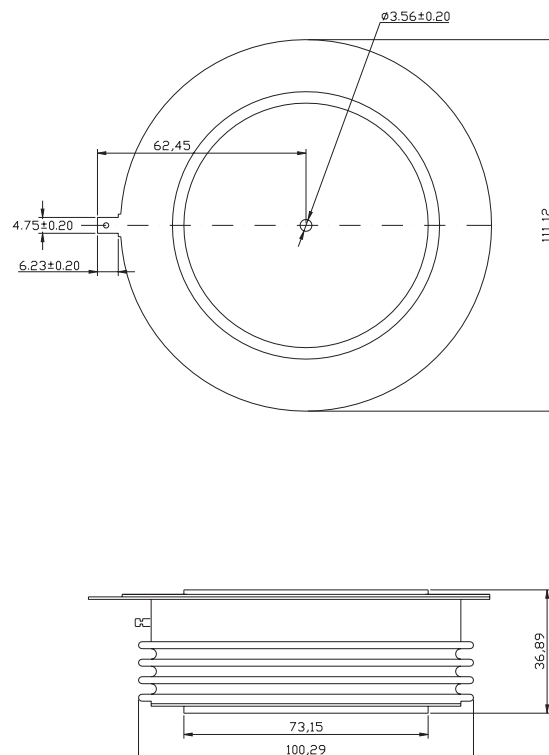


Fig. 8 - Outline Characteristics