TH8061

Voltage Regulator with integrated LIN Transceiver

Features

- o Compatible to LIN Specification 1.3, 2.0 and SAE J2602
- o Operating voltage V_S = 5.5 ... 18 V
- o Low standby current consumption of < 50 μA in sleep mode
- o Linear low drop voltage regulator 5V/50mA
    - Output current limitation
- o LIN-Bus Transceiver
    - Compatible to ISO9141 functions
    - Baud rate up to 20 kBaud
    - Slew rate control for best EME behavior
    - High EMI immunity
    - High signal symmetry for using in RC – based slave nodes up to 2% clock tolerance
- o Wake-up via LIN bus traffic
- o Reset output (100ms/4.65V)
- o Overtemperature shutdown
- o Automotive Temperature Range of –40°C to 125°C
- o CMOS compatible interface to microcontroller
- o Load dump protected (40V)
- o Small SOIC8 package

Ordering Information

Part No.	Temperature Range	Package	Revision
TH8061 KDC A	K (-40 to 125 °C)	DC (SOIC8)	A

General Description

The TH8061 consists of a low-drop voltage regulator 5V/50mA and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 1.3, 2.0 and SAE J2602.
The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

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2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device cannot be guaranteed if any of these limits are exceeded.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{SUP}	5.25	18	V
Output voltage	V_{CC}	4.95	5.05	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature	T_J		+150	°C

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VSUP [1]	V_{SUP}		-1.0	18	V
		$T \leq 60\,s$	-	30	
		$T \leq 500\,ms$	-	40	
Input voltage at pin BUS [1]	V_{BUS}		-24	30	V
		$T \leq 500\,ms$	-	40	
Difference VSUP-VCC	$V_{SUP}-V_{CC}$		-0.3	40	V
Input voltage at pin EN	V_{INEN}		-0.3	$V_{SUP}+0.3$	V
Input voltage at pin TxD, RxD, RESET	V_{IN}		-0.3	$V_{CC}+0.3$	V
Input current at pin EN, TxD, RxD, RESET	I_{IN}		-25	25	mA
Input current for short circuit of pin VSUP and VCC	I_{INSH}		-500	500	mA
ESD Capability on any pin	ESD_{HB}	Human body Modell, 100pF via 1.5kΩ	-2	2	kV
Power dissipation	P_0		Internal limited [2]		
Thermal resistance from junction to ambient(SOIC8)	R_{THJA}			160	K/W
Junction temperature [2]	T_J			150	°C
Storage temperature	T_{STG}		-55	150	°C

[1]   The voltage values are valid independent from each other.
[2]   See chapter 4.1 Power Dissipation and operating range

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_{SUP} = 5.25 to 18V and T_{AMB} = -40 to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VSUP						
Operating voltage	V_{SUP}		5.25	12	18	V
Supply current, VCC „noload" [3]	I_{Snl}	V_{EN} = V_{SUP} = 12V, V_{BUS} > V_{SUP}-0.5V, Pins 4 to 8 open			110	µA
Supply current, „sleep mode"	I_{Ssleep}	V_{SUP} = 12V, V_{EN} = 0V, V_{BUS} > V_{SUP}-0.5V		35	50	µA
V_{SUP} under voltage reset "off"	V_{SUVR_OFF}	V_{SUP} ramp up	3.1	3.5	3.9	V
V_{SUP} under voltage reset "on"	V_{SUVR_ON}	V_{SUP} ramp down	2.7	3.0	3.3	V
V_{SUP} under voltage reset hysteresis	V_{SUVR_HYS}	V_{SUVR_OFF} - V_{SUVR_ON}	0.2			V
VCC						
Output voltage VCC	V_{CCn}	$5.5V \leq V_{SUP} \leq 18V$ T_A = 25°C	4.95	5.0	5.05	V
	V_{CCt}	$5.5V \leq V_{SUP} \leq 18V$	4.90	5.0	5.10	V
	V_{CCh}	V_{SUP} > 18V	4.90	5.0	5.25	V
	V_{CCl}	3.3 V< V_{SUP}< 5.5 V	V_{SUP}-V_D		5.1	V
Drop-out voltage [4]	V_D	I_{VCC} = 20mA			150	mV
		I_{VCC} = 50mA			500	mV
Output current VCC	I_{VCC}	$V_{SUP} \geq 3.0V$	50			mA
Current limitation VCC	I_{LVCC}	V_{SUP} > 0V			150	mA
Load capacity [5]	C_{load}	See chapter 4.2 Low Dropout Regulator	4.7			µF
Reset threshold	V_{RES}	refered to V_{CC}, V_{SUP} > 4.6V	4.5	4.65	4.8	V
Master reset threshold (internal signal) [1]	V_{MRes}		3.0	3.15	3.3	V
Enable Input EN						
Input voltage low	V_{ENL}		-0.3		1.6	V
Input voltage high	V_{ENH}		2.5		V_{SUP} +0.3	V
Hysteresis [1]	V_{ENHYS}		100			mV
Pull-down current EN	I_{pdEN}	V_{EN} > V_{ENH}	1.0	4.0	7.0	µA
		V_{EN} < V_{ENL}	70	100	130	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output RESET						
Output voltage low	V_{OL}	I_{OUT} = 1 mA, V_{SUP} > 5.5 V			0.8	V
		10 kΩ RESET to VCC V_{SUP} = V_{CC} = 0.8 V			0.2	V
Pull-up current	I_{pu}		-500	-375	-250	µA
LIN BUS Interface						
Receive threshold	V_{thr_rec}, V_{thr_dom}		0.4* V_{SUP}		0.6* V_{SUP}	
Center point of receive threshold $V_{thr\_cnt} = (V_{thr\_rec}+V_{thr\_dom})/2$	V_{thr_cnt}	7.0 V ≤ V_{SUP} ≤ 18 V	0.475* V_{SUP}	0.5* V_{SUP}	0.525* V_{SUP}	V
Hysteresis of receive threshold $V_{thr\_hys} = V_{thr\_rec}-V_{thr\_dom}$	V_{thr_hys}		0.12* V_{SUP}	0.135* V_{SUP}	0.15* V_{SUP}	
Input current BUS (recessive) [3]	I_{INBUSR}	8.0 ≤ V_{BUS} ≤ 18 V, V_{SUP}= V_{BUS} - 0.7V, TxD = 5V			20	µA
Input current BUS (recessive)	$-I_{INBUSR}$	V_{SUP}= 0V, V_{BUS} =- 12V	-1			mA
Pull up resistor bus	R_{BUSpu}		20	30	47	kΩ
Output voltage BUS (dominant) [3]	V_{BUSdom}	7.0 ≤ V_{SUP} ≤ 18 V, TxD = 0V, R_L = 500Ω			1.2	V
Output voltage BUS (recessive) [2] [3]	V_{BUSrec}	7.0 ≤ V_{SUP} ≤ 18 V, TxD = 5V	0.8*V_{SUP}			V
Current limitation BUS	I_{LIM}	V_{BUS} > 2.5V, TxD = 0V	40		120	mA
Input TxD						
Pull-up resistor	R_{pu_TxD}	V_{IN} = 0V	9.5	15	21	kΩ
Input low level TxD	V_{IL}				0.25	V_{CC}
Input high level TxD	V_{IH}		0.75			V_{CC}
Output RxD						
Output voltage Low RxD	V_{OL}	I_{OUT} = 1 mA			0.8	V
Output voltage High RxD	V_{OH}	I_{OUT} = -1 mA	V_{CC} - 0.3			V
Thermal Protection						
Thermal shutdown [1]	T_{JSHD}		155		175	°C
Thermal recovery [1]	T_{JREC}		126		150	°C

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[1]   No production test, guaranteed by design and qualification
[2]   The recessive voltage at pin BUS should be less than 80% of the voltage at V_{BAT}. The voltage at V_{SUP} results with consideration of reverse diode V_{SUP} = V_{BAT} - 0,7V
[3]   See chapter 2.6 Test Circuit for Dynamic and Static Characteristics
[4]   The nominal V_{CC} voltage is measured at V_{SUP} =12V. If the V_{CC} voltage is 100mV below its nominal value then the voltage drop is V_D = V_{SUP} – V_{CC}.
[5]   See chapter 4 for application hints.

2.4 Dynamic Characteristics

$7V \leq V_{SUP} \leq 18V$, $-40°C \leq T_A \leq 125°C$, unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RESET						
Reset time	t_{Res}		70	100	140	ms
Reset rising time [1]	t_{rr}		3.0	7.5	15	µs
Debouncing time BUS [1]	t_{deb_BUS}		1.5	2.8	4.0	µs
Wake up time	t_{wake_BUS}		25	60	120	µs
General LIN BUS parameter						
Transmit propagation delay TxD -> BUS [2] [3]	t_{dr_TXD}, t_{df_TXD}	R_L/C_L at BUS 1kΩ/1nF 660Ω/6.8nF 500Ω/10nF			4	µs
Symmetry of propagation delay BUS -> RxD [2]	t_{dsym_TXD}	$t_{dr\_TXD} - t_{df\_TXD}$	-2		2	µs
Receiver propagation delay BUS -> RxD [2] [3]	t_{dr_RXD} t_{df_RXD}	$C_{L(RXD)} = 50pF$			6	µs
Symmetry of propagation delay TxD -> BUS [2]	t_{dsym_RXD}	$t_{dr\_RXD} - t_{df\_RXD}$	-2		2	µs
Slew rate BUS rising edge [1]	dV/dT_{rise}	$20\% \leq V_{BUS} \leq 80\%$ $C_{BUS} = 100$ pF	1.0	1.7	2.5	V/µs
Slew rate BUS falling edge [1]	dV/dT_{fall}	$20\% \leq V_{BUS} \leq 80\%$ $100pF \leq C_{BUS} \leq 10nF$	-2.5	-1.7	-1.0	V/µs
LIN BUS parameter according to LIN Spec. Rev. 1.3						
Slope time, transition from recessive to dominant [2] [3]	t_{sdom}	$V_{SUP} = 8$ V $R_L = 500Ω / C_L = 10nF$			12	µs
		$V_{SUP} = 18$ V $R_L = 500Ω / C_L = 10nF$			18	
Slope time, transition from dominant to recessive [2] [3]	t_{srec}	$V_{SUP} = 8$ V $R_L = 500Ω / C_L = 10nF$			12	µs
		$V_{SUP} = 18$ V $R_L = 500Ω / C_L = 10nF$			18	
Slope time symmetry	t_{ssym}	$V_{SUP} = 8$ V $R_L = 500Ω / C_L = 10nF$ $T_{ssym} = t_{sdom} - t_{srec}$	-7		1	µs
		$V_{SUP} = 18$ V $R_L = 500Ω / C_L = 10nF$ $T_{ssym} = t_{sdom} - t_{srec}$	-5		5	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN BUS parameter according to LIN Spec. Rev. 2.0						
Conditions: $\quad$ VSUP =7.0V to 18V; BUS loads: 1kΩ/1nF;660Ω/6.8nF;500Ω/10nF $\quad$ TxD signal: t_{Bit} = 50µs, t_{wH} = T_{wL} = t_{Bit}; t_{rise} = t_{fall} < 100ns						
Minimal recessive bit time [2] [3]	$t_{rec(min)}$		40	50	58	µs
Maximum recessive bit time [2] [3]	$t_{rec(max)}$		40	50	58	µs
Dyty cycle 1	D_1	$D_1 = t_{rec(min)} / (2 \cdot t_{Bit})$	0.396			
Dyty cycle 2	D_2	$D_2 = t_{rec(max)} / (2 \cdot t_{Bit})$			0.581	

[1] $\quad$ No production test, guaranteed by design and qualification
[2] $\quad$ See chapter 2.5 Timing Diagrams
[3] $\quad$ See chapter 2.6 Test Circuit for Dynamic and Static Characteristics

2.5 Timing Diagrams
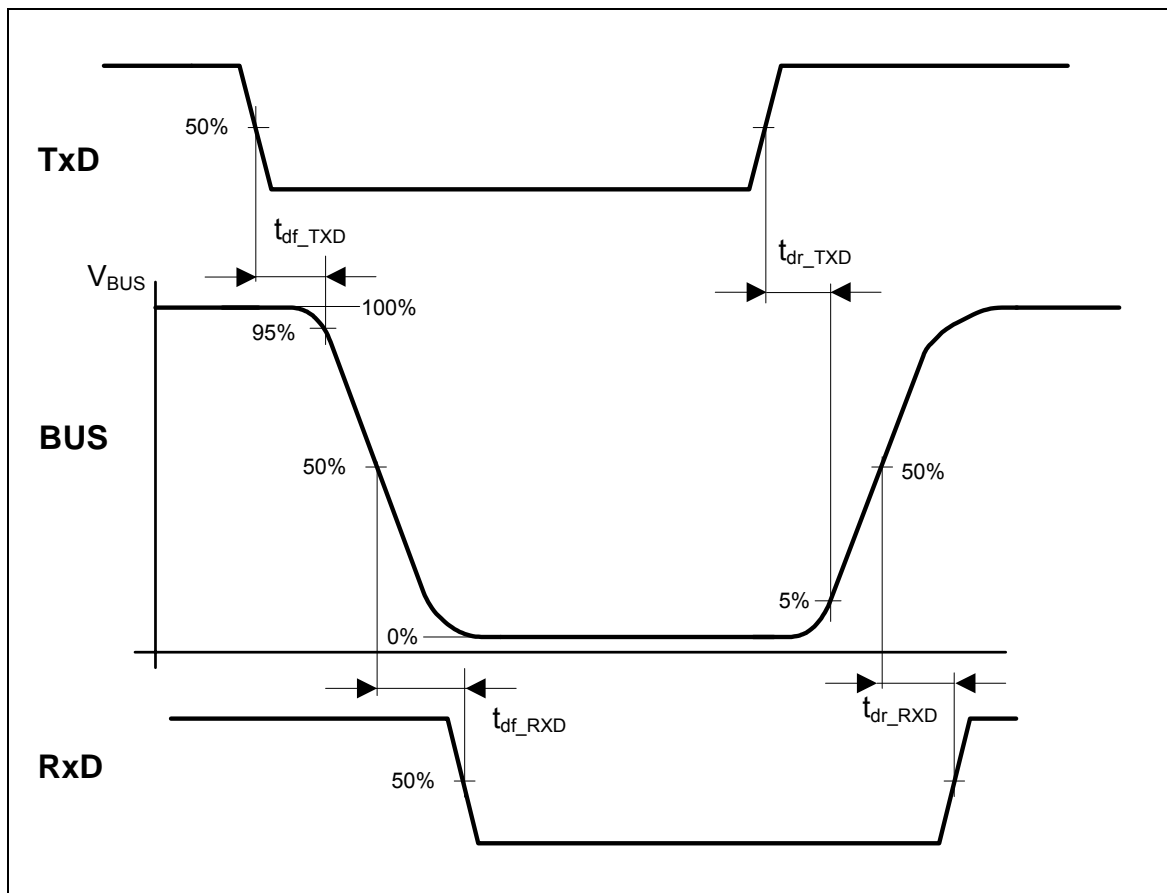
Figure 2 - Timing diagram for propagation delay acc. to LIN 1.3 and 2.0
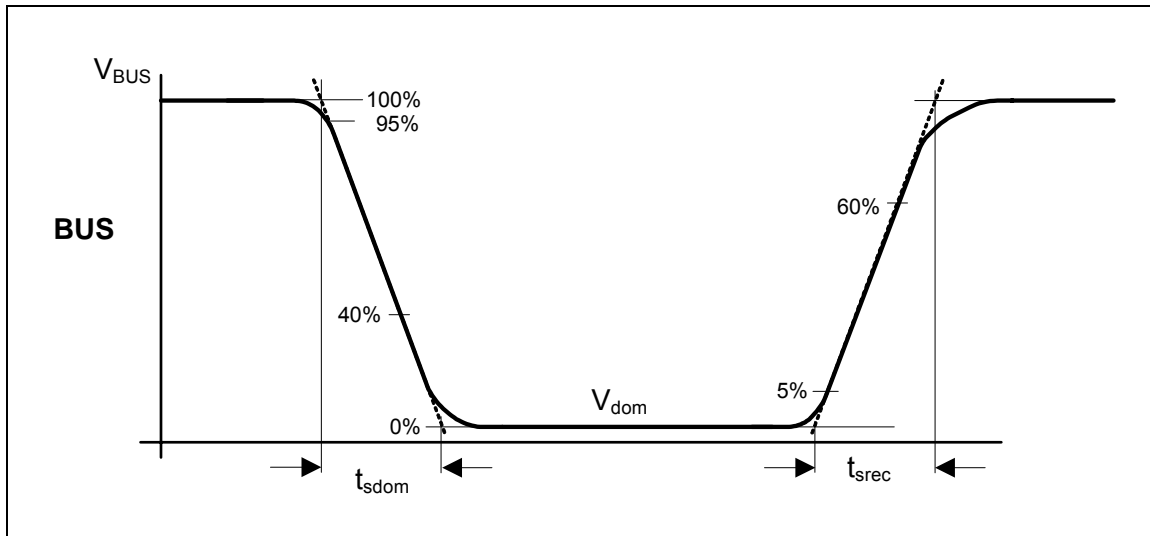
Figure 3 - Timing diagram for slope times acc. to LIN 1.3
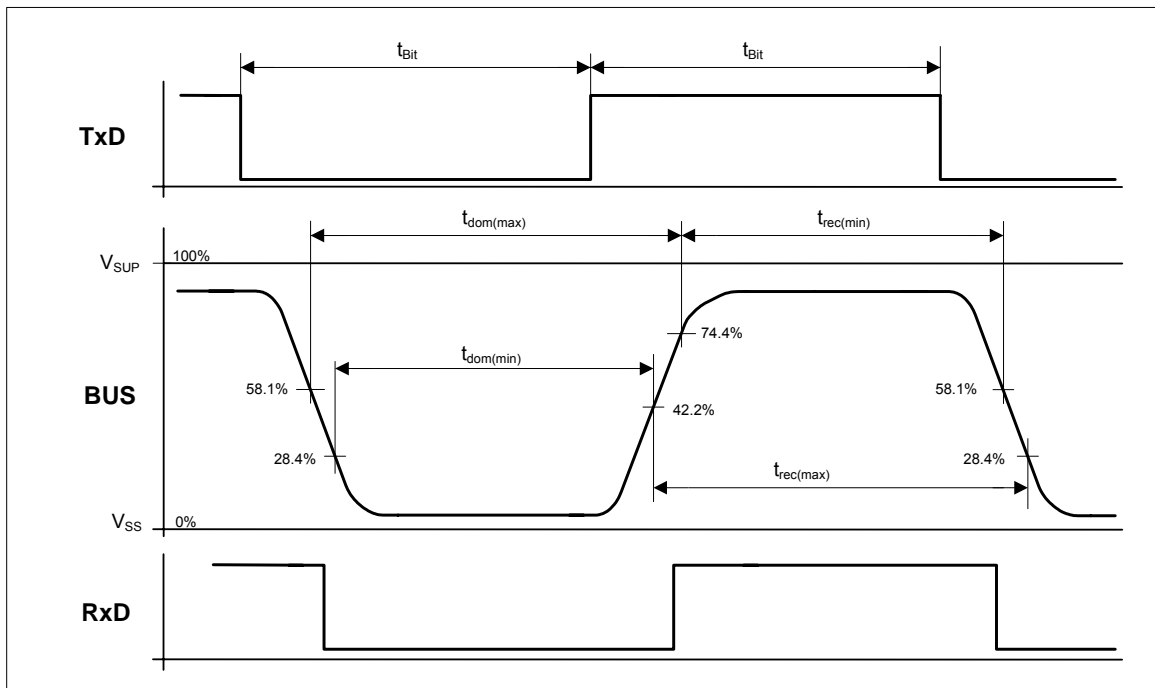
Figure 4 - Timing diagram for duty cycle acc. to LIN 2.0

2.6   Test Circuit for Dynamic and Static Characteristics
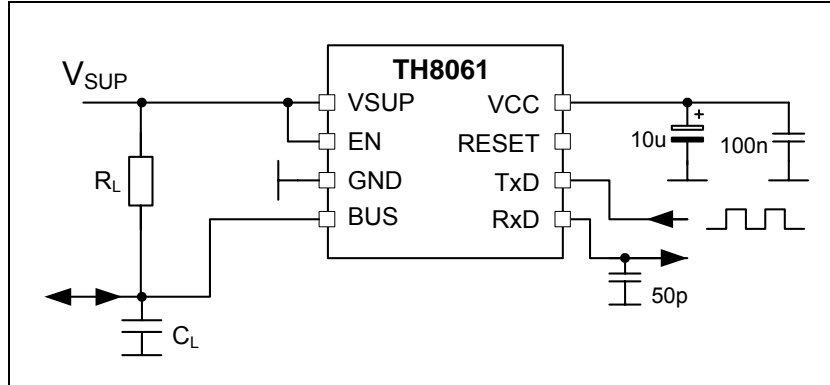
Figure 5 - Test circuit for delay-, slope times and duty cycles
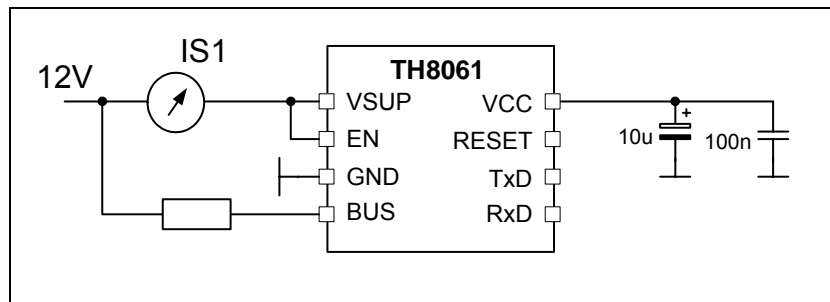
Figure 6 - Test circuit for supply current I_{Snl}
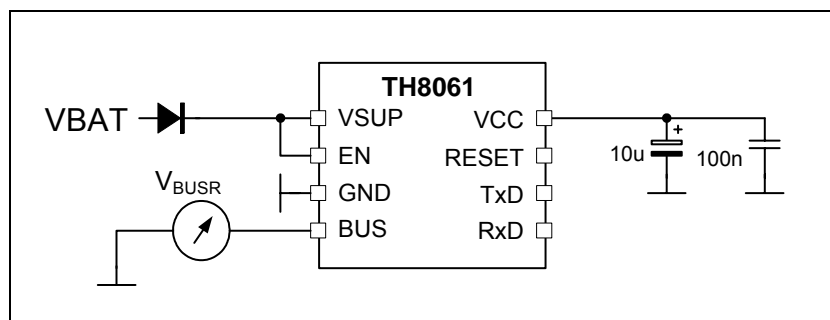
Figure 7 - Test circuit for bus voltage "recessiv" V_{BUSrec}
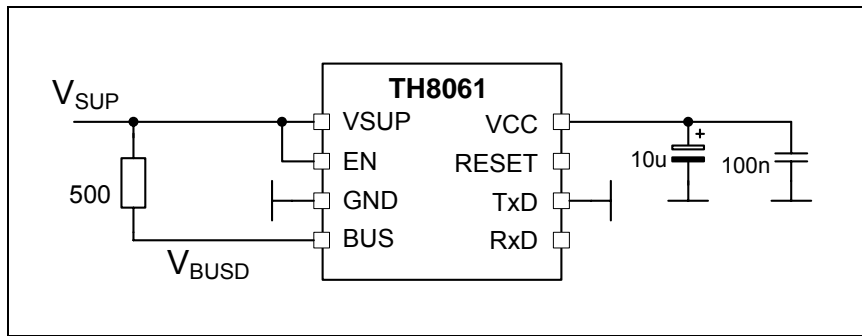
Figure 8 - Test circuit for bus voltage "dominant" V_{BUSdom}
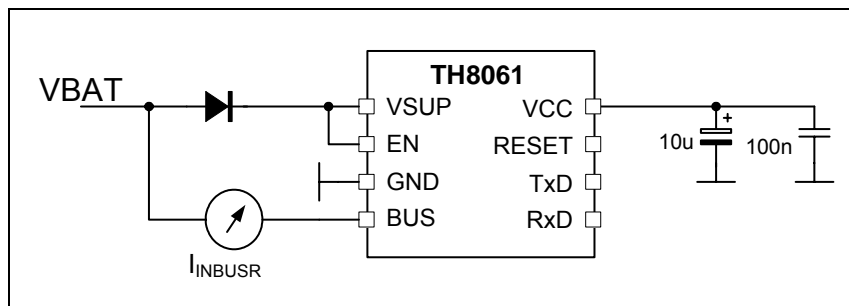
Figure 9 - Test circuit for bus current "recessiv" I_{INBUSR}

3. Functional Description

The TH8061 consists of a low drop voltage regulator 5V/50mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller.
Additionally integrated is a RESET output with a reset delay of 100ms and a fixed threshold of 4.65V.

3.1 Operating Modes

The TH8061 provides two main operating modes "normal" and "sleep" and the intermediate states "POR", "Ini-state" and "thermal shutdown". The main modes are fixed states defined by basic actions (VSUP start, EN or wake-up). The intermediate states are soft states. They aren't defined by logical actions but by changes of voltage (VSUP, VCC) or junction temperature.
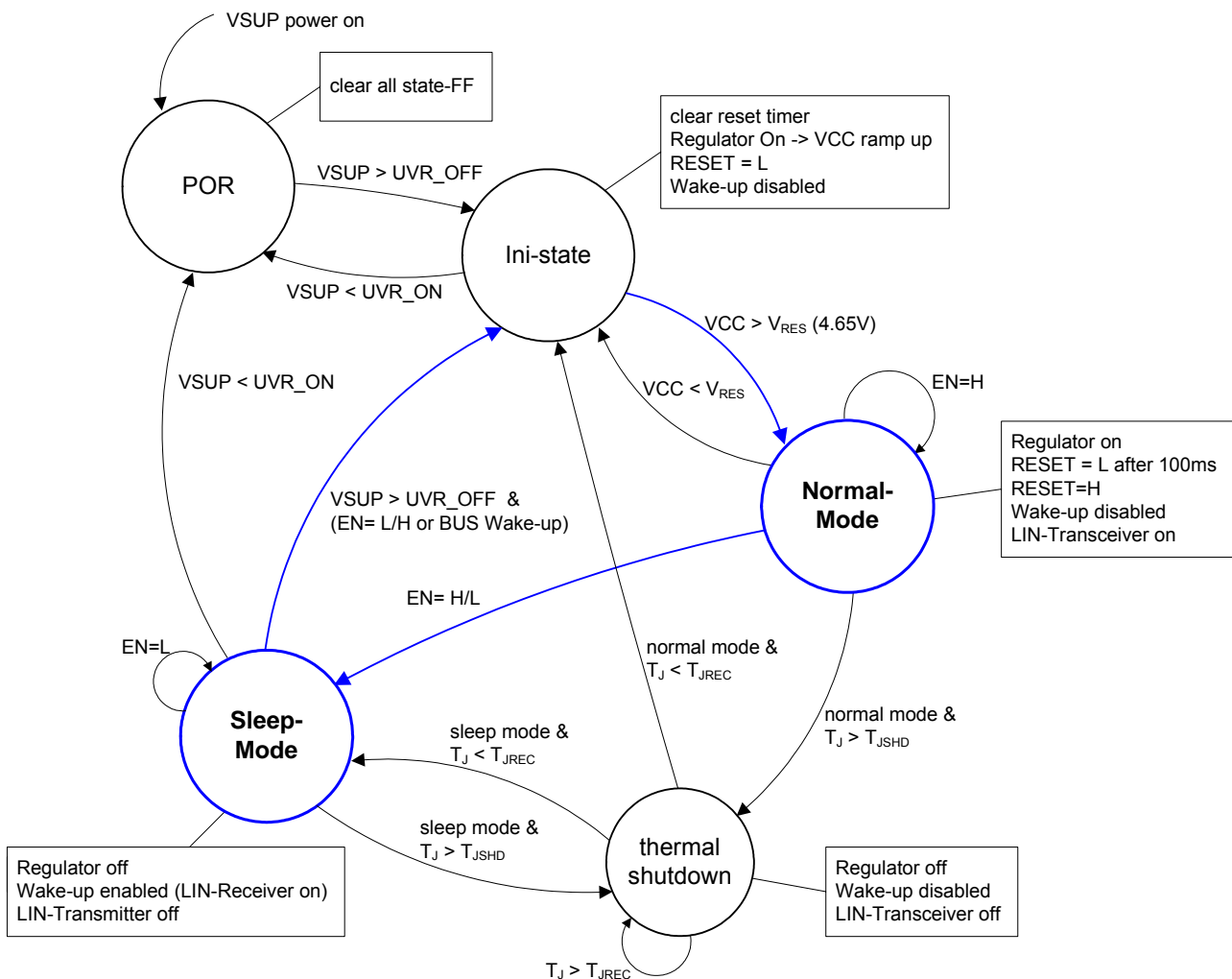
Figure 10 - State diagram of operating modes

Normal Mode

The whole TH8061 is active. Switching to normal mode can be done via the following actions:
- Start of V_{SUP} or after under voltage reset
- Rising edge at EN (EN=high)   (local wake-up)
- Activity on the LIN bus   (remote wake-up)

Sleep Mode

Sleep mode is most current saving. With a falling edge on EN (EN=low) the TH8061 is switched from normal mode into sleep mode. The voltage regulator will be switched off and the LIN transceiver is in recessive state.

Switching into sleep mode can be done independently from the current transceiver state. That means if the transmitter is in dominant state this state will be cancelled and it will be switched to recessive state.

POR-state

This is the power-on-reset state of the TH8061, while Vsup < V_{SUVR_OFF}. If the prior state was sleep mode, the TH8061 switches via the ini-state to normal mode.

Ini-state

This is an intermediate state, which will pass through after switch on of VSUP or VCC. The TH8061 remains in this state if VCC is below V_{RES} (Reset output = L) and Vsup > V_{SUVR_ON}.

Thermal Shutdown

If the junction temperature T_J is higher than T_{JSHD} (>155°C), the TH8061 will be switched into the thermal shutdown mode. The behaviour within this mode is comparable with the sleep mode except for LIN transceiver operating. The transceiver is completely disabled, no wake-up functionality is available.

If T_J falls below the thermal recovery temperature T_{JREC} (typ. 140°C) the TH8061 will be recover to the previous state (normal or sleep).

3.2 Initialization

Initialization is started if the power supply is switched on as well as every rising edge on of the TH8061 via the EN pin.

VSUP- Power-ON

If V_{SUP} is switched on the TH8061 starts to normal mode via the POR- and Ini-state. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the TH8061 into normal mode. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operates independent from each other, which secures the independence from the rise time of VSUP. During fast VSUP edges the power-on reset will be active. If the increasing of VSUP is very slow (> 1ms/V) the under voltage reset unit initializes the voltage regulator if V_{SUP} > V_{SUVR_OFF} (typ. 3.5V).

The effects of both POR circuits at different VSUP slopes will shown in Figure 11.
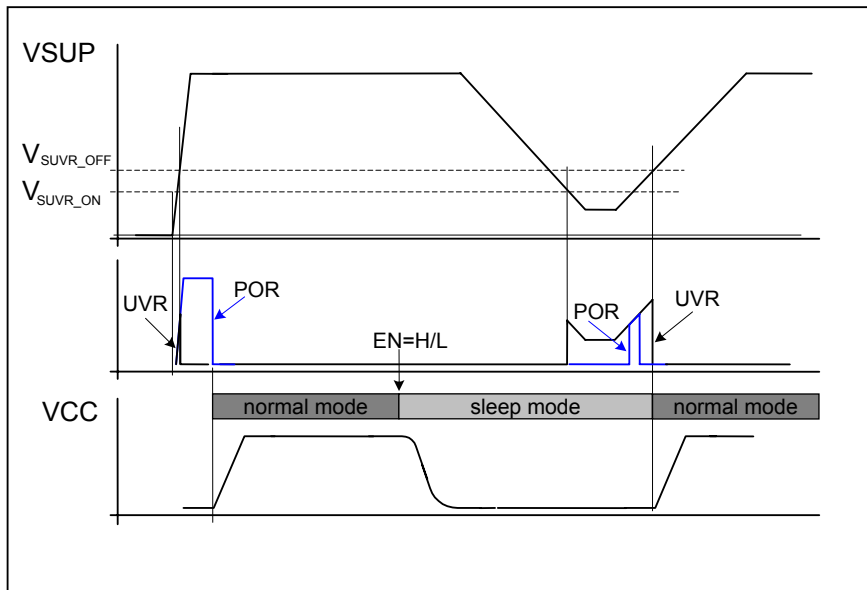
Figure 11 - Operating of power-on and under-voltage reset

After POR the voltage regulator starts and VCC will be output. If $V_{CC} > V_{MRes}$ the bus interface will be activated. If the V_{CC} voltage level is higher than V_{RES}, the reset time t_{Res} = 100ms is started. After t_{Res} the RESET output switches from low to high (see Figure 16).

Start of Linear Regulator via Wake-up

The initialization is only being done for the VCC circuitry parts. This procedure begins with leaving the master reset state ($V_{CC} > V_{MRes}$) and runs in the same manner as the VSUP-Power-On.

3.3   Wake-Up

If the regulator is put into sleep mode it can be wake up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. $60\mu s$ switches on the regulator.
After the BUS has wake up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

3.4 VSUP under voltage reset

The under voltage detection unit inhibit an undefined behaviour of the TH8061 under low voltage condition. If VSUP drops below V_{SUVR_ON} (typ. 3V) the under voltage detection becomes active and the IC will be switched to POR state. The following increasing of VSUP above V_{SUVR_OFF} (typ. 3.5V) cancels this POR state and the voltage regulator starts with the initialization sequence.

VSUP under voltage in Normal Mode

Supply Voltages below V_{SUVR_OFF} don't influence the voltage regulator. The output voltage Vcc follows VSUP.

VSUP under voltage in Sleep Mode

No exit from the sleep mode will take place if the VSUP voltage drops down to V_{SUVR_ON} (typ. 3V). The under voltage reset becomes active (POR-state). As a result of this operating, the sleep mode is left to the normal mode. If VSUP rises again above V_{SUVR_OFF} (typ. 3.5V) the IC initialize the voltage regulator and continue to work with the normal mode.

The under voltage reset unit secures stable operating in the under voltage range of VSUP down to GND level. The dynamic Power-On-Reset secures a defined internal state independent from the duration of the VSUP drop, which secures a stable restart.

3.5 Overtemperature Shutdown

If the junction temperature is 155°C < T_J < 170°C the over-temperature recognition will be activated and the regulator voltage will be switched off. The V_{CC} voltage drops down, the reset state is entered and the bus-transceiver is switched off (recessive state).
After T_J falls below 140°C the TH8061 will be initialized again (see Figure 16) independently from the voltage levels on EN and BUS. Within the thermal shutdown mode the transceiver can't be switched to the normal mode neither with local nor with remote wake-up.
The operation of the TH8061 is possible between T_{Amax} (125°C) and the switch off temperature, but small parameter differences can appear.
After over-temperature switch-off the IC behaves as described in chapter 3.8 RESET.

3.6   LIN BUS Transceiver

The TH8061 is a bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.

The transceiver consists of a pnp-driver (1.2V@40mA) with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a debouncing unit.

Transmit Mode

During transmission the data at the pin TxD will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:
- Sleep mode
- Thermal Shutdown active
- Master Reset (V_{CC} < 3.15V)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of V_{BUS} during differential voltage between VSUP and BUS (V_{BUS}>V_{SUP}).

No additional termination resistor is necessary to use the TH8061 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit (τ = 2.8µs).
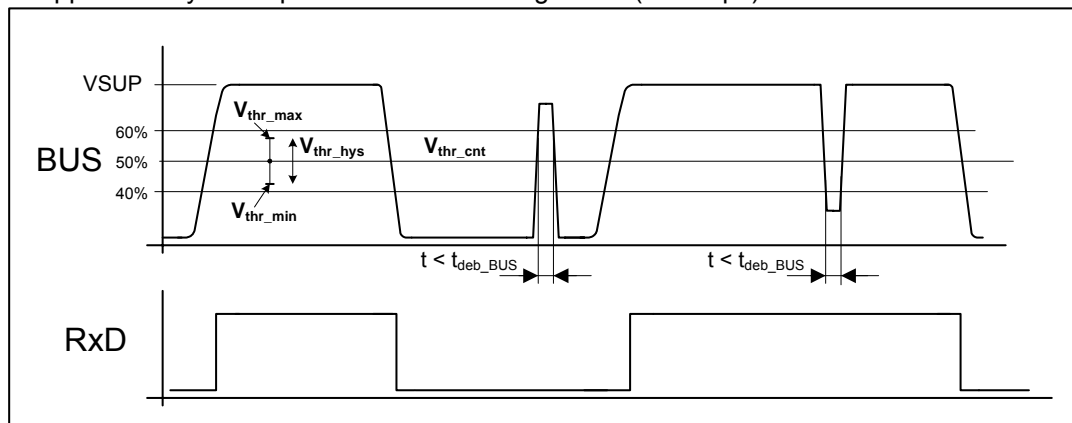
Figure 12 - Receive mode impulse diagram

The receive threshold values V_{thr_max} and V_{thr_min} are symmetrical to the centre voltage of 0.5*V_{SUP} with a hysteresis of 0.135*V_{SUP}. Including all tolerances the LIN specific receive threshold values of 0.4*V_{SUP} and 0.6*V_{SUP} will be securely observed.

Datarate

The TH8061 is a ***constant slew rate*** transceiver which means that the bus driver works with a fixed slew rate range of 1.0 V/µs ≤ $\Delta V/\Delta T$ ≤ 2.5V/µs. This principle secures a very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}). The TH8061 guarantees data rates up to 20kbit within the complete bus load range under worst case conditions. The constant slew rate principle is very robust against voltage drops and can operate with RC-oscillator systems with a clock tolerance up to ±2% between 2 nodes.

Input TxD

The 5V input TxD controls directly the BUS level:

TxD = low	->	BUS = low (dominant level)
TxD = high	->	BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to VCC. This guarantees that an open TxD pin generates a recessive BUS level.
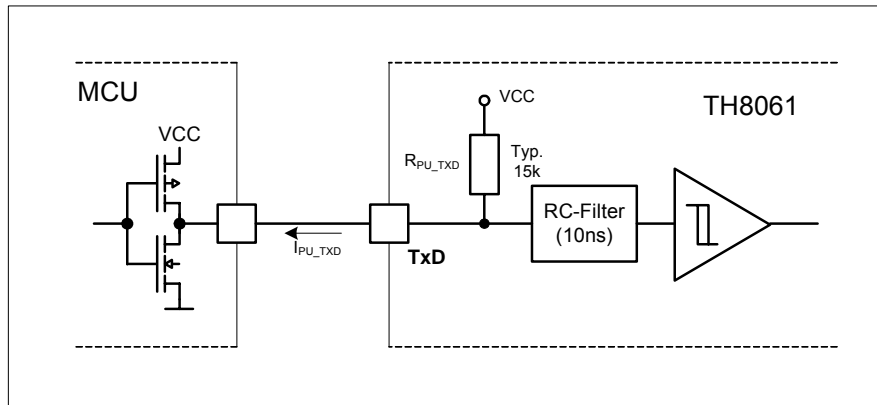
Figure 13 - TxD input circuitry

Output RxD

The received BUS signal will be output to the RxD pin:

BUS < $V_{thr\_cnt} - 0.5 * V_{thr\_hys}$	->	RxD = low
BUS > $V_{thr\_cnt} + 0.5 * V_{thr\_hys}$	->	RxD = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.
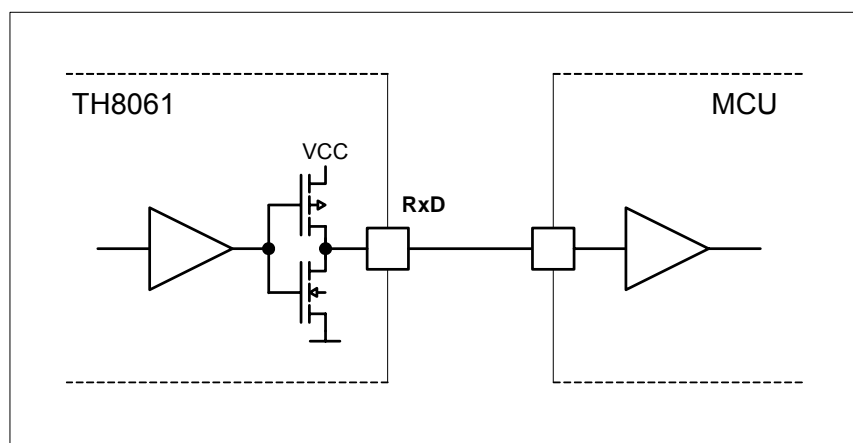
Figure 14 - RxD output circuitry

3.7 Linear Regulator

The TH8061 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±2% and a current of ≤50mA within an input voltage range of 5.5V ≤ V_{SUP} ≤ 18V. The current limitation unit limits the output current for short circuits or overload to 100mA respectively drop-down of the V_{CC} voltage.
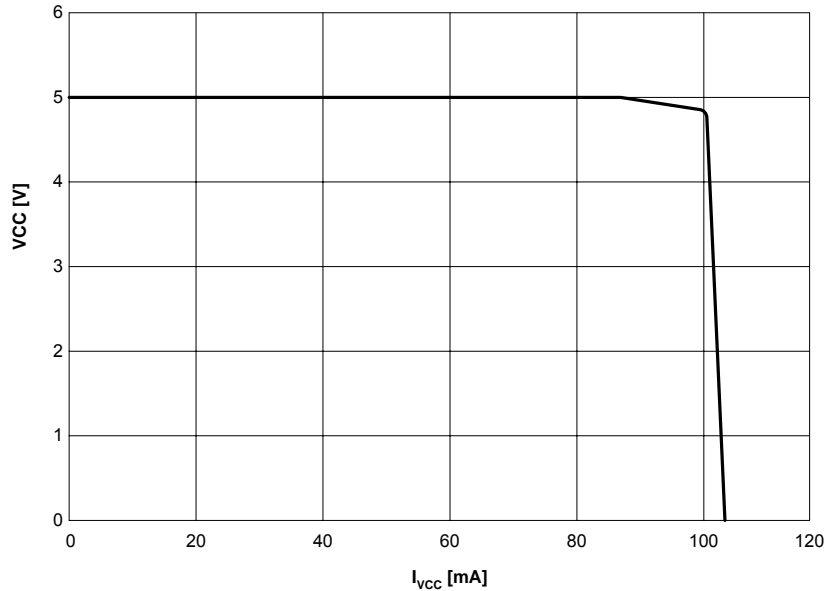
Figure 15 - Characteristic of current limitation VCC = f(I_{vCC})

3.8 RESET

The RESET pin outputs the reset state of the TH8061. This output is switched from low to high if V_{SUP} is switched on and V_{CC}>V_{RES} after the time t_{Res}.
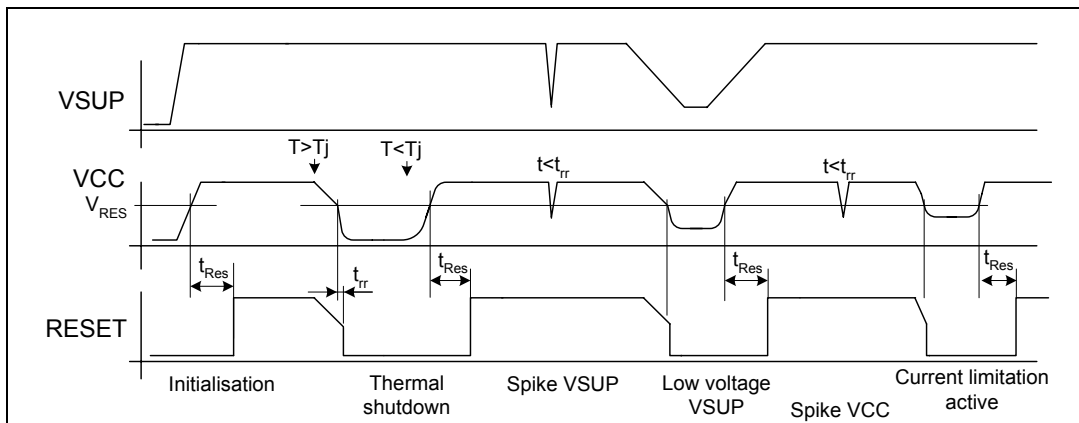
Figure 16 - Reset behaviour

If the voltage V_{CC} drops below V_{RES} then the RESET output is switched from high to low after the time t_{rr} has been reached. For this reason short breaks of the V_{CC} voltage and uncontrolled reset generations will be inhibited. The circuitry of the RESET output driver guarantees, that the reset low level during decreasing of the V_{CC} voltage will be hold sure (s.a.Figure 17).
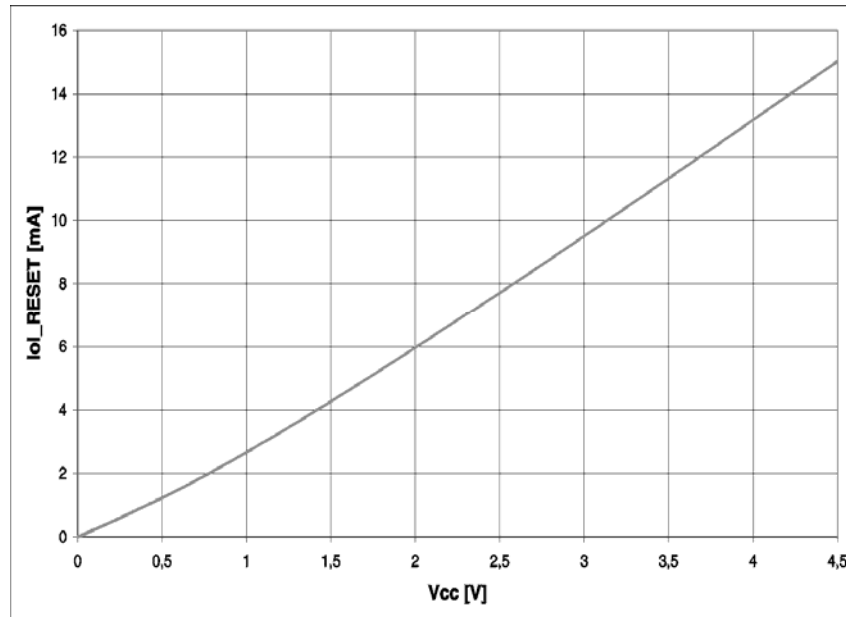
Figure 17 - Output current of reset output vs. VCC voltage

3.9   Mode Input EN

The TH8061 is switched into the sleep mode with a falling edge and into normal mode with a rising edge at the EN pin. The normal mode will be kept as long as EN = high.

The deactivation of TH8061 with a falling edge at EN can be done independently from the state of the bus-transceiver.
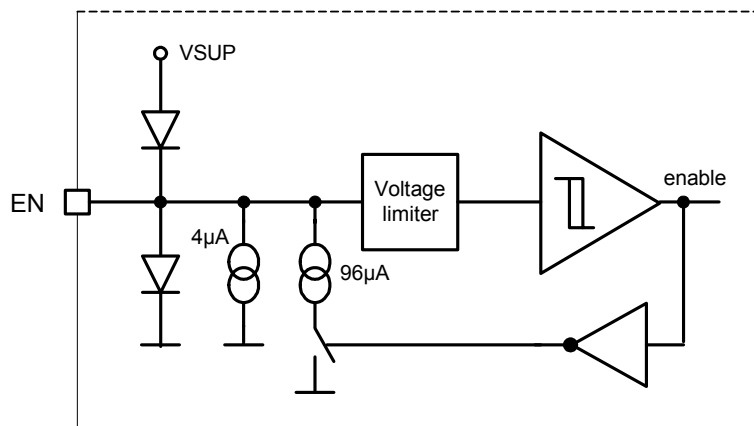
Figure 18 - EN input circuitry

The maximum input voltage is VSUP. The threshold is typ. 2.1V and therefore also CMOS levels can be used as input signal. Figure 18 shows the internal circuitry of the EN pin.

The EN input is internally pulled down to secure that if this pin is not connected a low level will be generated. It will be used two different pull down current sources for high and low level to minimize the sleep mode current.

The 4µA pull down current source is used if the input voltage V_{IN} > high level voltage V_{ENH}. If the input voltage drops below the low level of EN V_{ENL} additional the second current source is used. The resulting pull down current in this case is 100µA.
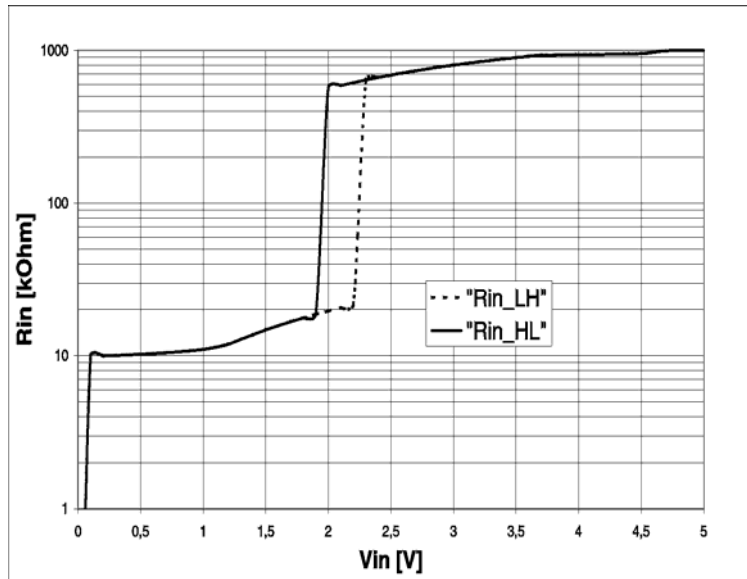
Figure 19 - R$_{IN}$ characteristics of EN-input

The wide input voltage range allows different EN control possibilities. If the EN input is connected to an CMOS output of the MCU, a falling edge switches the TH8061 into sleep mode (the regulator is also switched off). The wake up is only possible via the bus line.
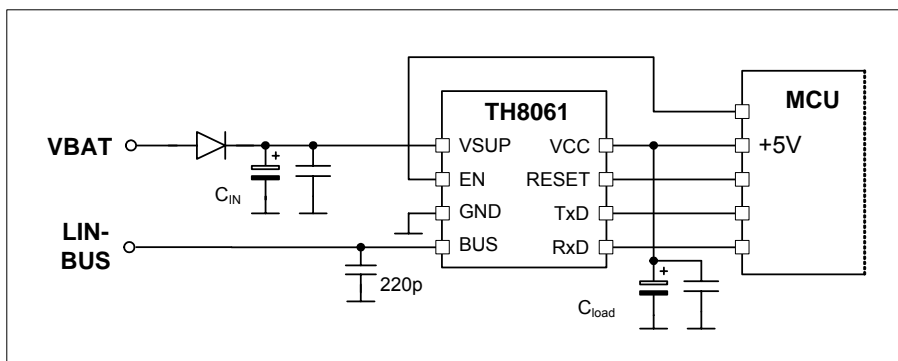
Figure 20 - EN controlled via MCU

If the application don't needs the wake up capability of the TH8061 a direct connection EN to VSUP is possible. In this case the TH8061 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via a VBAT signal.
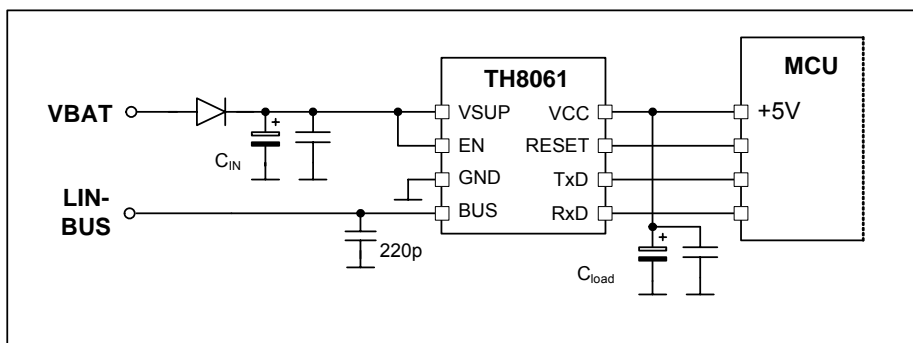
Figure 21 - Permanent normal mode

4. Application Hints

4.1 Power Dissipation and operating range

The maximum power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.
The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{CC}) * I_{VCC} + P_{D\_TX}$$

The power dissipation of the transmitter P_{D_TX} depends on the transceiver configuration and its parameters as well as on the bus voltage $V_{BUS}=V_{BAT}-V_D$, the resulting termination resistance R_L, the capacitive bus load C_L and the bit rate. Figure 22 shows the dependence of power dissipation of the transmitter as function of V_{SUP}. The conditions for calculation of the power dissipation is $R_L=500\Omega$, $C_L=10nF$, bit rate=20kbit and duty cycle on TxD of 50%
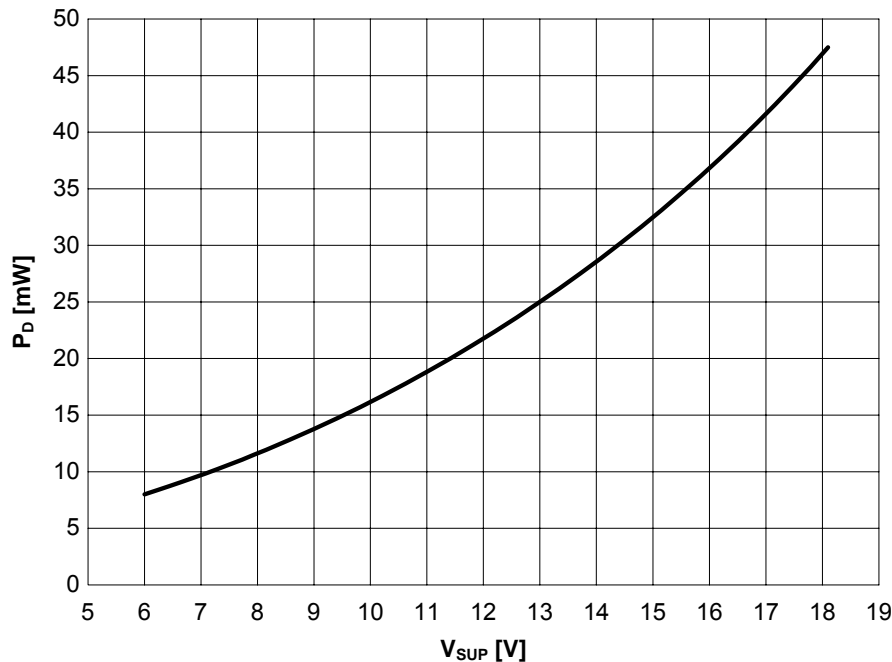
Figure 22 - Power dissipation LIN transceiver @ 20kbit

The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_j - T_A}{R_{THJ-A}}$$

If we consider that $P_{D\_TX\_max}= f(V_{SUP})$ the max output current I_{VCC} on V_{CC} can be calculated:

$$I_{VCCmax} = \frac{\dfrac{T_j - T_A}{R_{THJ-A}} - P_{D\_TX\_max} @ VSUP}{VSUP - VCC}$$

$T_J - T_A$ is the temperature difference between junction and ambient and R_{th} is the thermal resistance of the package. The thermal energy is transferred via the package and the pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

Figure 23 - Save operating area

The linear regulator of the TH8061 operates with input voltages up to 18V and can output a current of 50mA. The maximum power dissipation limits the maximum output current at high input voltages and high 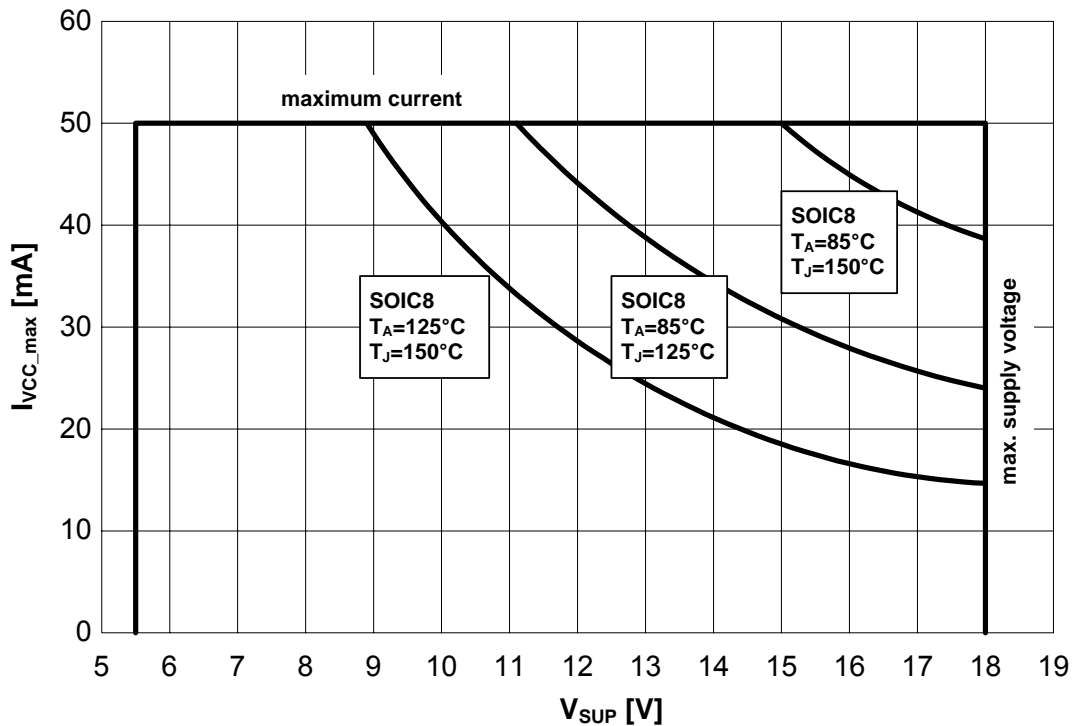ambient temperatures. The output current of 50mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between V_{SUP} and V_{CC}. See Figure 23 for safe operating areas for different ambient and junction temperatures.

4.2 Low Dropout Regulator

The voltage regulator of theTH8061 is a low dropout regulator (LDO) with a p-MOSFET as driving transistor. This kind of regulator has a standard pole, generated from the internal frequency compensation and an additional pole, which is dependent from the load and the load capacity. This additional pole can cause an instable behaviour of the regulator! It is required a zero point to compensate this additional pole. It can be realised via an additional load resistor in series with a load capacity. It is used for this compensation the equivalent series resistance (ESR) of the load capacity. Every real capacity is characterized with an ESR value. With the help of this ESR value an additional zero point is implemented into the amplification loop and therefore the result of the negative phase shift is compensated.
Because of this correlation the regulator has a stable operating area which is defined by the load resistance R_L, the load capacity C_L and the corresponding ESR value. The load resistance resp. load current is defined by the application itself and therefore the compensation of the pole can only be done via variation of the load capacity and ESR value.

Input Capacity on VSUP C_{IN}

It is necessary an input capacity of $C_{IN} \geq 4.7\mu F$. Higher capacity values improves the line transient response and the supply noise rejection behaviour. The combination of electrolytic capacity (e.g.100µF) in parallel with a ceramic RF-capacity (e.g.100nF) archives good disturbance suppressing.
The input capacity should be as closed as possible (< 1cm) placed to the VSUP pin.

Load Capacity on VCC C_L

The regulator is stabilized by the output capacitor C_L. The TH8061 requires a minimum of 4.7µF capacity connected to the 5V output to insure stability. This capacitor should maintain its ESR in the stable region of the ESR curve (See Figure 24) over the full operating temperature range of the application. The capacity value and the ESR of a capacitor changes with temperature. The minimal capacity value must be kept within the whole operating temperature range.
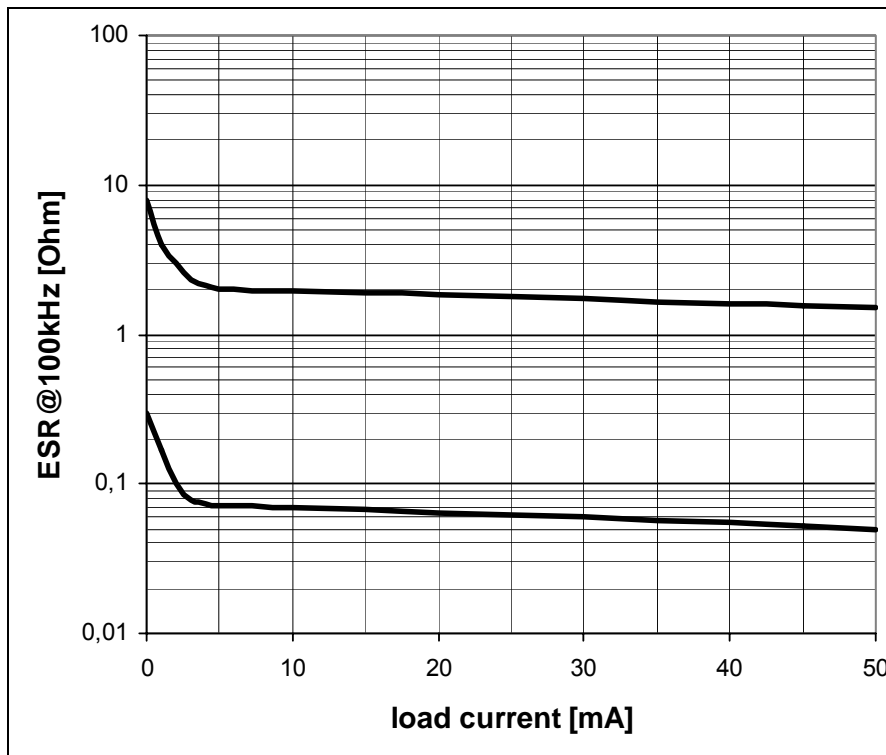

Figure 24 - ESR Curves for 6.8µF ≤ C_L ≤ 100µF and Frequency of 100kHz

The value and type of the output capacitor can be selected using the diagram shown in Figure 24.

Capacity Value

The capacity value of an electrolytic capacitor is dependence from the voltage, temperature and the frequency. The temperature coefficient of the capacity value is positive, that means that the value increases with increasing of the temperature. The capacity value decreases with increasing of the frequency. This behavior of a capacitor can cause that at T_A=-40°C the capacity value falls below the minimum required capacity for the regulator. In this case the regulator becomes instable, which means the regulator starts oscillation. The nominal value of the capacitor at T_A=25°C have to be chosen with enough margin under consideration of the capacitor specification. The instable behavior will be amplified because of the decreasing of the capacity with this oscillation.

ESR

The equivalent serial resistance is the resistor part of the equivalent circuit diagram of a capacitor. The ESR value is dependent from the temperature and frequency. Normally the specified ESR values for a capacitor is valid at a temperature of T_A=25°C and a frequency of f=100kHz.
The temperature coefficient is negative, which means with increasing of the temperature the ESR value decreases. In the choice of the capacity has to be taken into account that the ESR can decrease at T_A=-40°C dramatically that the valid operating area can be left, which causes that the regulator will be instable.

Tantalum Capacitors

This type of capacitor has a low dependence of the capacity and the ESR from the temperature and is therefore well suitable as VCC load capacity.

Aluminum Capacitors

These capacitors show a strong influence of the capacity and the ESR from the temperature. These characteristic restrains the usability as load capacity for the low drop regulator of TH8061.

4.3 Application Circuitry
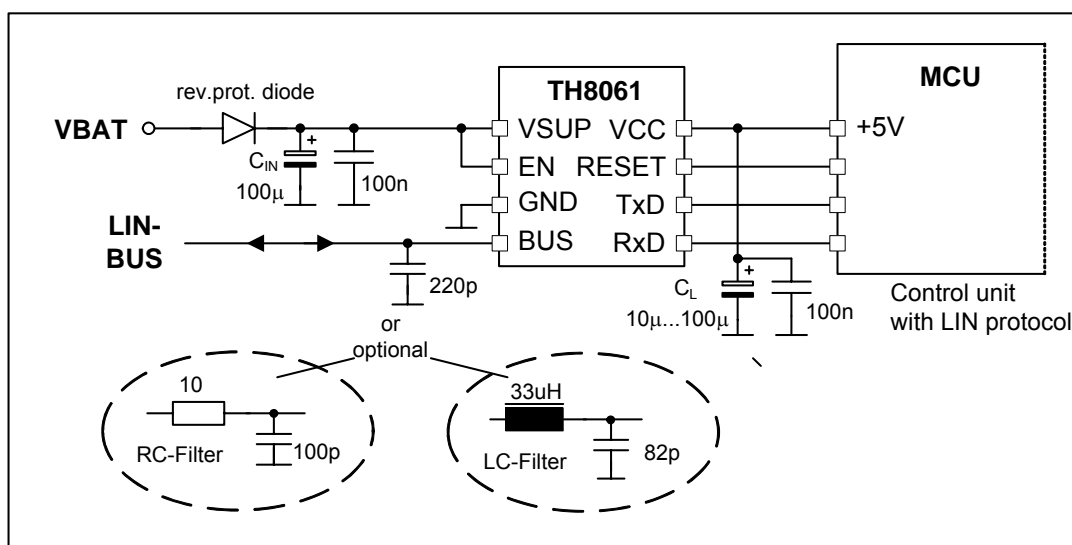
Figure 25 - Application circuit (slave node)

4.4 EMI Supressing

To minimize the influence of EMI on the bus line a 220pF capacitor should be connected directly to the BUS pin (see Figure 25). This EMI-Filter makes sure that the RF imissions into the IC from the BUS line have no affect resp. will be limited.

The value of the filter capacity can be adjusted to the size of the LIN network. 220pF should be used for bigger networks. Values from 333pF up to 1nF should be used for middle to small LIN networks. Finally the size of the filter capacity influences the effectiveness of the EMI suppressing in observation of the maximum LIN bus capacity of 10nF.

Alternatively to a pure C-filter it is also possible to use LC- or RC-filter. The dimension of C, L or R, L depends on the corner frequency, the maximum LIN bus capacity (10nF) and the compliance with the DC- and AC LIN bus parameters.
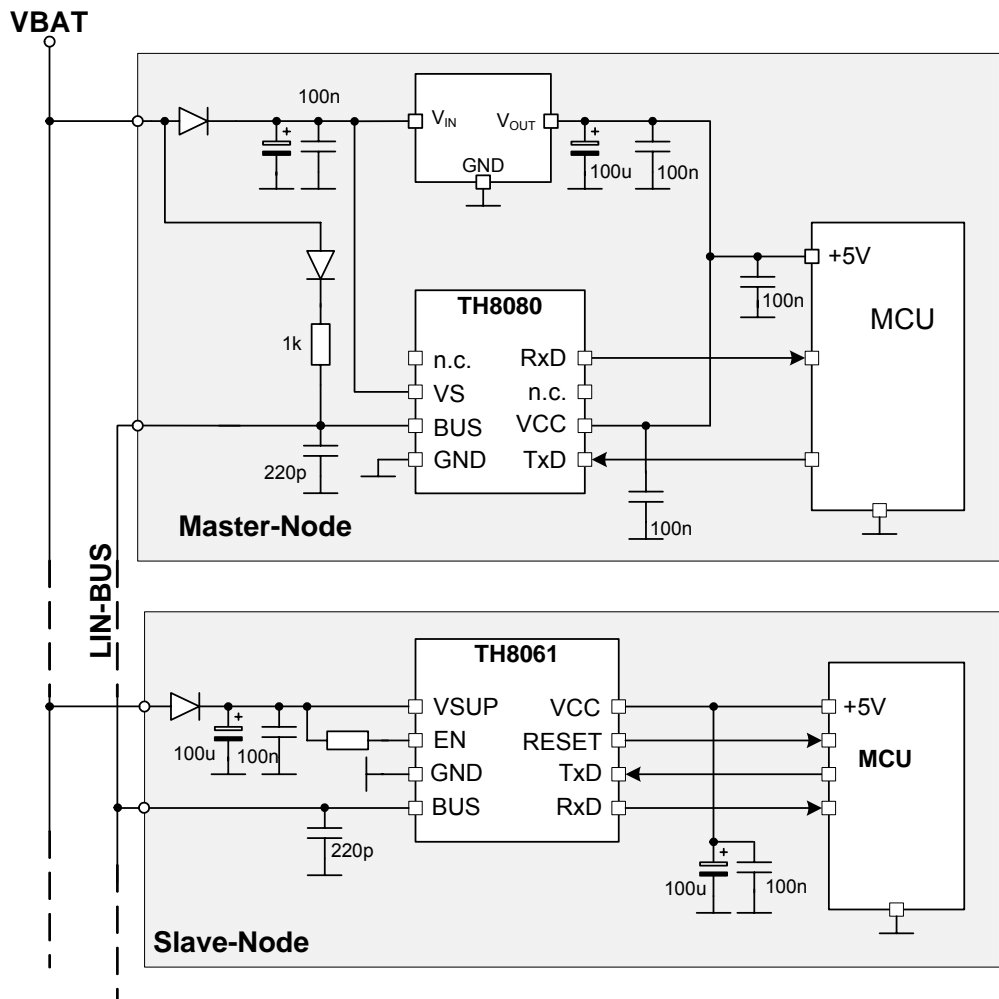
Figure 26 - Application circuit for LIN subbus with TH8061 as slave node

4.5 Connection to Flash-MCU

While programming a flash MCU the TH8061 should be disconnected from the MCU. This can be done via disconnecting the supply voltage from the TH8061 or by switching off with the EN pin. The reverse current supply of the IC via the RxD pin, if the connected MCU pin is used as normal signal input and programming input, must be inhibited via a decoupling diode. In this case the MCU must be supplied via the programming interface.

Prog.-Data

10u...47u

TH8061

MCU

VCC

47n...100n

RESET

TxD

RxD

0.7V

$V_{high\_RxD} >= 4.7V$ at $V_{CC} = 5V$
$V_{low\_RxD} = 0.8V$

$V_{high} = 4V$ at $V_{CC} = 5V$

Figure 27 – Example circuitry for connection of RxD to MCU for flash programming

The programming of the Flash is also possible via the LIN pin, if the MCU supports this kind of flash mode.

5. Operating during Disturbance

5.1 Operating without VSUP or GND

The absence of V_{SUP} or GND connection will not influence or disturb the communication between other bus nodes. No reverse supply of the IC can appear if without GND or VSUP connection the BUS pin is on VBAT level.

5.2 Short Circuit BUS against VBAT

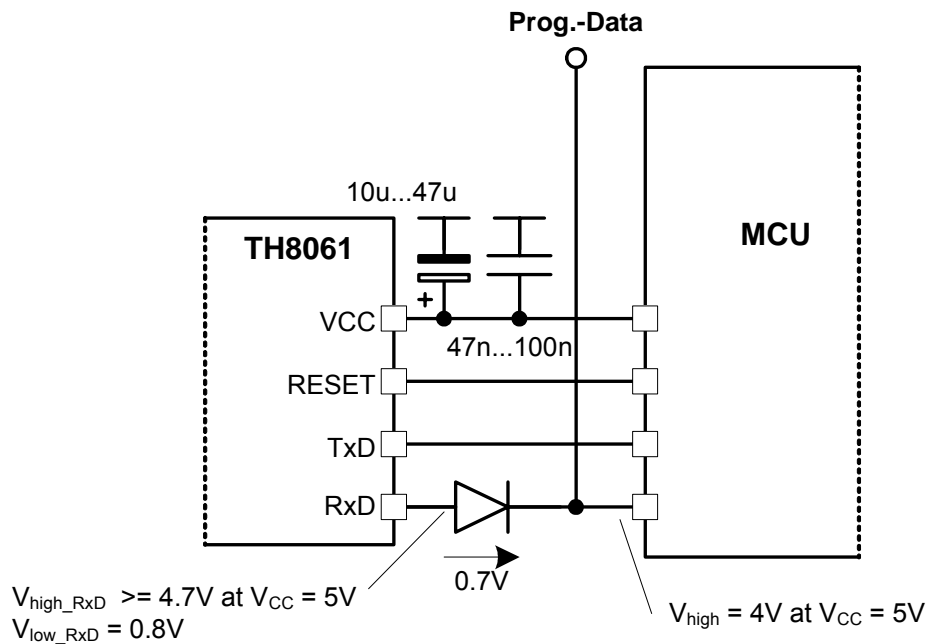The reaction of the IC depends on the send state of the transceiver:
- Recessive   LIN bus is blocked, no influence to the TH8061
- Dominant   Current limitation, thermal shut down of TH8061 if power dissipation will make an overrun of T_J

5.3 Short Circuit BUS against GND

LIN bus is blocked. No influence on the TH8061.

5.4 Short Circuit TxD against GND

The LIN transceiver is permanently in the dominant state, that means the whole LIN bus. This state can only be detected from the LIN controller. In this case the controller must switch off the LIN node via the EN input of the TH8061. A thermal shut down of TH8061 will appear if the power dissipation and will make an overrun of T_J.

5.5 TxD open

The internal pull-up resistor forces the LIN node to the recessive state. The communication between the other bus-nodes will not be disturbed.

5.6 Short Circuit VCC against GND

The VCC pin is protected via a current limitation. This state is comparable with the behaviour in the sleep mode.

5.7 Overload of VCC

Thermal switch off

The power dissipation is increasing if the load current is between I_{VCC_max} and I_{LVCC}. If the max junction temperature of >155°C is reached, the IC will be switched off. The voltage regulator will also be switched off and a reset signal is forced.

Over current

If the current limitation is active the voltage on VCC drops down. If this voltage under-runs the threshold V_{RES}, a reset will be forced.

5.8 Undervoltage VSUP, VCC

The reset unit ensures the correct behaviour of the driver during under-voltage. The BUS pin generates the recessive state if $V_{CC} < V_{MRes}$. The inputs EN and TxD have pull-up and pull-down characteristics.
If $V_{MRes} \le V_{CC} \le 4.5V$ the TxD signal is transmitted to the bus. The receive mode is also active.

5.9 Short circuit RxD, RESET against GND or VCC

Both outputs are short circuit proof to VCC and ground.

6. PIN Description

```
        VSUP  ┌1      8┐  VCC
          EN  ┌2      7┐  RESET
                 TH8061
         GND  ┌3      6┐  TxD
         BUS  ┌4      5┐  RxD
```
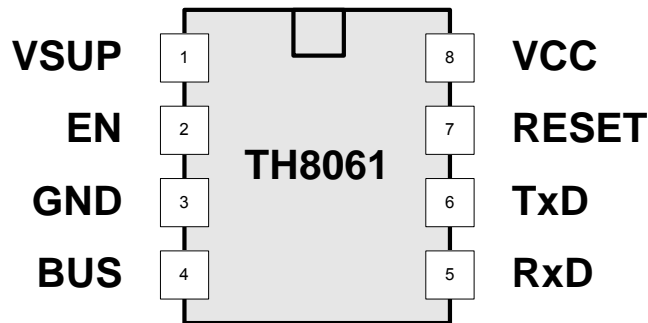
Pin	Name	IO-Typ	Description
1	VSUP		Supply voltage
2	EN	I	Enable Input voltage regulator, HV-pull-down-Input, High-active
3	GND		Ground
4	BUS	I/O	LIN bus line
5	RxD	O	Receive Output, 5V-push-pull
6	TxD	I	5V-Transmit Input, pull-up-Input
7	RESET	O	Reset 5V-output, active low
8	VCC	O	Regulator output 5V/50mA

7. Mechanical Specification
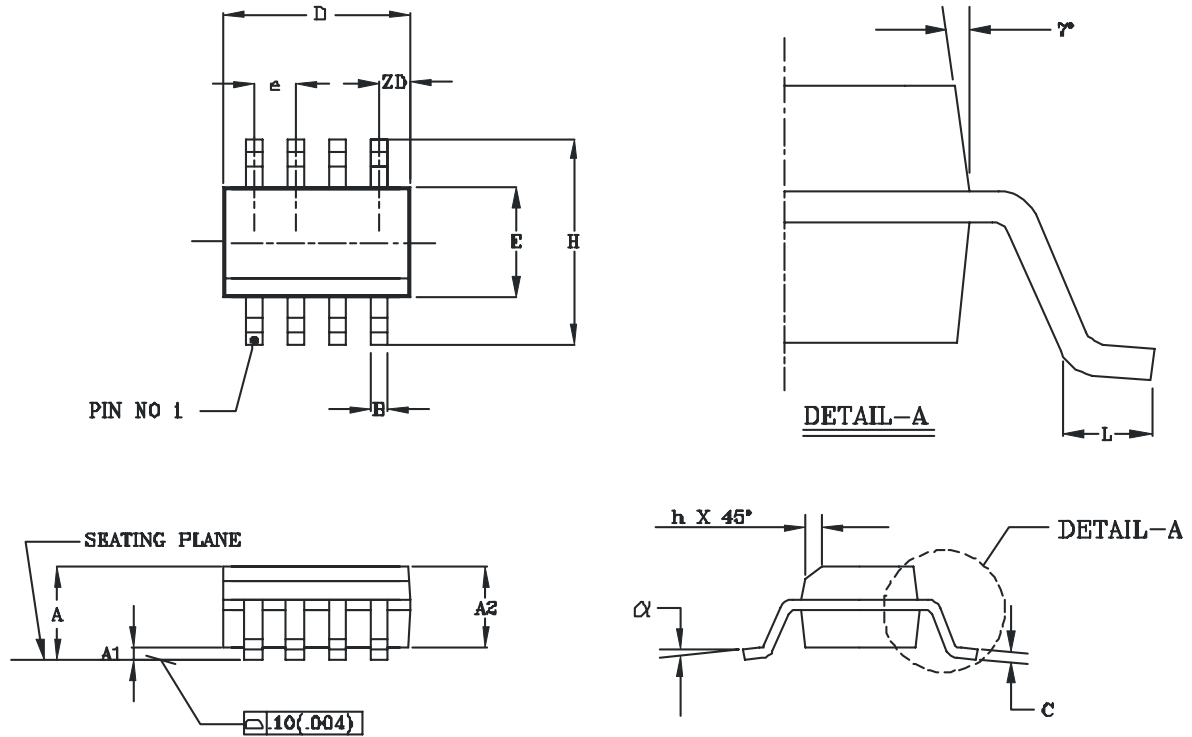
Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min max	0.10 0.25	0.36 0.46	0.19 0.25	4.80 4.98	3.81 3.99	1.27	5.80 6.20	0.25 0.50	0.41 1.27	1.52 1.72	0° 8°	0.53	1.37 1.57
All Dimension in inch, coplanarity < 0.004″													
min max	0.004 0.0098	0.014 0.018	0.0075 0.0098	0.189 0.196	0.150 0.157	0.050	0.2284 0.244	0.0099 0.0198	0.016 0.050	0.060 0.068	0° 8°	0.021	0.054 0.062

8. Tape and Reel Specification

8.1 Tape Specification

max. 10°

IC pocket

Top View

max. 10°

Sectional View

R min.

T₂ notation: figure with labels T_2, T, K_0, B_1, T_1, Cover Tape, G_1, G_2, D_0, P_0, P_2, $< A_0 >$, B_0, E, F, W, P_1, D_1
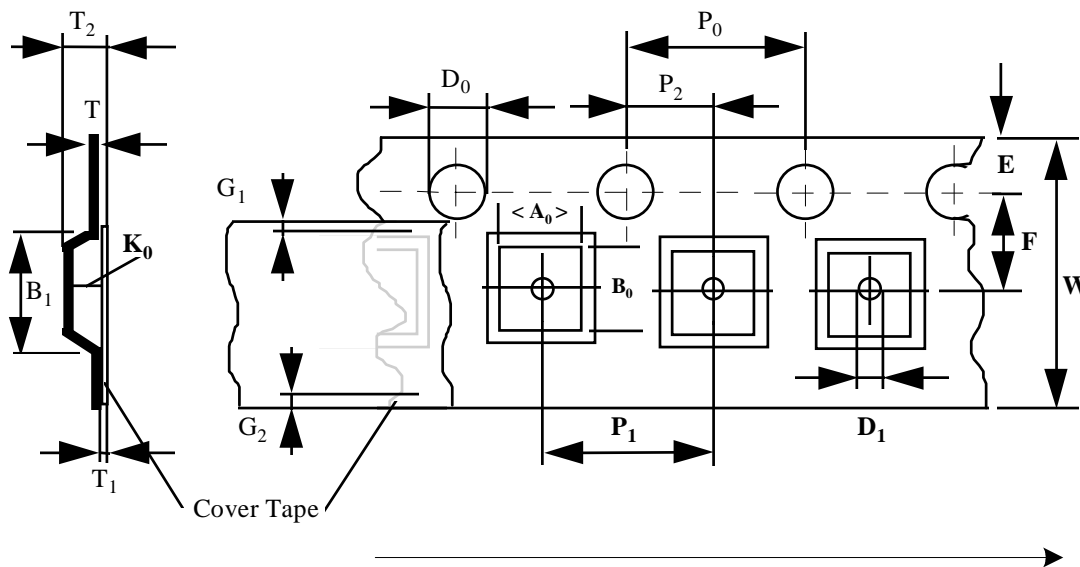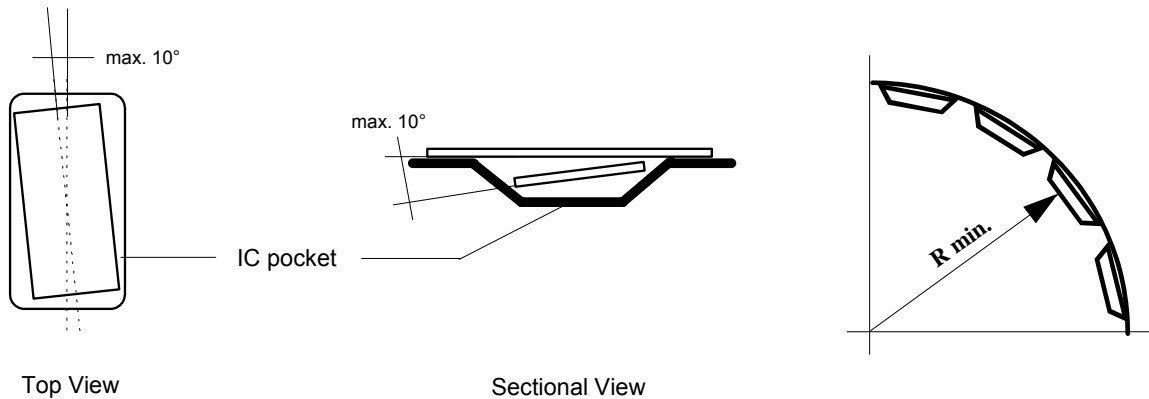
Standard Reel with diameter of 13″

Package	Parts per Reel	Width	Pitch
SOIC8	2500	12 mm	8 mm

D_0	E	P_0	P_2	T_{max}	$T_{1\ max}$	$G_{1\ min}$	$G_{2\ min}$	$B_{1\ max}$	$D_{1\ min}$	F	P_1	R_{min}	$T_{2\ max}$	W
1.5 +0.1	1.75 ±0.1	4.0 ±0.1	2.0 ±0.05	0.6	0.1	0.75	0.75	8.2	1.5	5.5 ±0.05	4.0 ±0.1	30	6.5	12.0 ±0.3

A_0, B_0, K_0 can be calculated with package specification.
Cover Tape width 9.2 mm.

8.2 Reel Specification
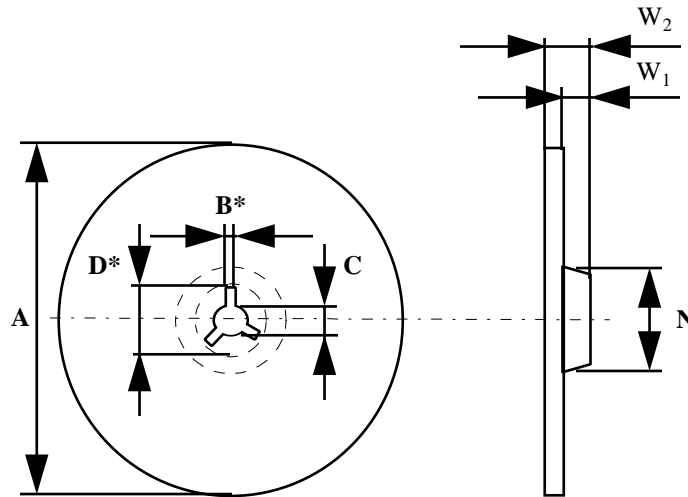
A_{max}	B^*	C	D^*_{min}
330	2.0 ±0.5	13.0 +0,5/-0,2	20.2

Width of half reel	N_{min}	W_1	$W_{2\ max}$
4 mm	100,0	4,4	7,1
8 mm	100,0	8,4	11,1

9. ESD/EMC Remarks

9.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

9.2 ESD-Test

The TH8061 is tested according MIL883-3015.7 (human body model).

9.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

Power Supply pin VSUP:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	5000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	5000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms / U_P+U_S = 40 V	10 pulses every 1min

Data- and signal pins EN, BUS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	1000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	1000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1000 burst

10. Revision History

Version	Changes	Remark	Date
1.0		Preliminary Release	Sep. 2000
1.2a		First official release	Feb. 2001
002	- General changes to new document layout - Improved features description - Added detailed block diagram - Changed LIN Bus static and dynamic parameters to be conform to LIN specification 1.2 and future 1.3 - Added static parameters for pin TxD and RxD - Add timing diagram for slope time - Improved functional description - Added chapter "Operating during Disturbance" - Added chapter "Application Hints" - Added chapter "ESD/EMC Remarks" - Added chapter "Reliability Information" - Added chapter "Disclaimer"	Complete rework of datasheet	Aug. 2002
003	- Added chapter "LIN System Parameters" - Added chapter "Min/max slope time calculation"		Sep. 2002
004	- Added chapter "Revision History"		Nov. 2002
005	- Add compatibility to LIN 1.3		Jan. 2003
006	- Changed ESR values in chapter 2.3 Static Characteristics - Update of chapter 0 - Add chapter "Tape and Reel Specification"		Sep.2003
007	- Update of "Block diagram" - Update of "Dynamic characteristic" with LIN 2.0 parameters - Update of chapter "Initialisation" - Update of chapter "Functional description TxD, RxD, Reset and EN" - Update of chapter "Low drop regulator" - Add chapter "Under voltage reset" - Deleted chapter "Recommandations for system design" - Delete of chapter "Min/Max slope time calculation"		Jun 2004

11. Assembly Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)
- CECC00802
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- EIA/JEDEC JESD22-B106
  Resistance to soldering temperature for through-hole mounted devices
- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices
- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a roadmap to qualify their package families for lead free processes also.
Various lead free generic qualifications are running, current results on request.

For more information on Melexis lead free statement see quality page at our website:
http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf

12. Disclaimer

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E-mail: sales_europe@melexis.com

All other locations:
Phone: +1 603 223 2362
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