SONY

CXD2931R-9/GA-9

1 chip GPS LSI

Description

The CXD2931R-9/GA-9 is a dedicated LSI for the GPS (Global Positioning System) satellite-based position measurement system.

This LSI contains a 32-bit RISC CPU, 2M-bit MASK ROM, RAM, UART, timer, and others.

This LSI, used together with the RF LSI (CXA1951AQ), enables the configuration of a 2-chip system capable of measuring its position anywhere on the globe.
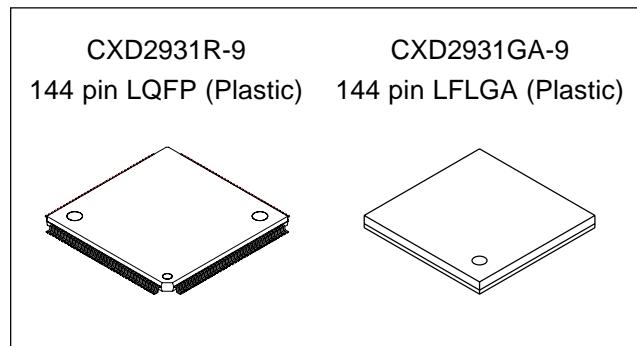
Features

- 16-channel GPS receiver capable of simultaneously receiving 16 satellites
- Supports differential GPS
  —Comforms to RTCM SC-104 Ver. 2.1
  —Supports DARC
- All-in-view measurement
- 2-satellite measurement
- Timer supporting GPS time
- High performance 32-bit RISC CPU
- 256K-byte program ROM
- 36K-byte RAM
- 3-channel UART
  —Baud rate generator
  —Supports 1.2K, 2.4K, 4.8K, 9.6K, 19.2K and 38.4K baud
  —Supports 1/2/4-byte buffer mode
- 23-bit general-purpose I/O port capable of defining input/output independently for each bit
- 8-bit successive approximation system A/D converter

Structure

Silicon gate CMOS IC

CXD2931R-9
144 pin LQFP (Plastic)

CXD2931GA-9
144 pin LFLGA (Plastic)

Absolute Maximum Ratings

- Supply voltage V_{DD} $V_{SS} - 0.5$ to 4.6 V
- Input voltage V_I $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Output voltage V_O $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Operating temperature
  T_{opr} -40 to $+85$ °C
- Storage temperature
  T_{stg} -50 to $+150$ °C

Recommended Operating Conditions

- Supply voltage V_{DD} 3.0 to 3.6 V
- Operating temperature
  T_{opr} -40 to $+85$ °C

Input/Output Pin Capacitance

- Input capacitance C_{IN} 9 (Max.) pF
- Output capacitance C_{OUT} 11 (Max.) pF
- I/O capacitance $C_{I/O}$ 11 (Max.) pF
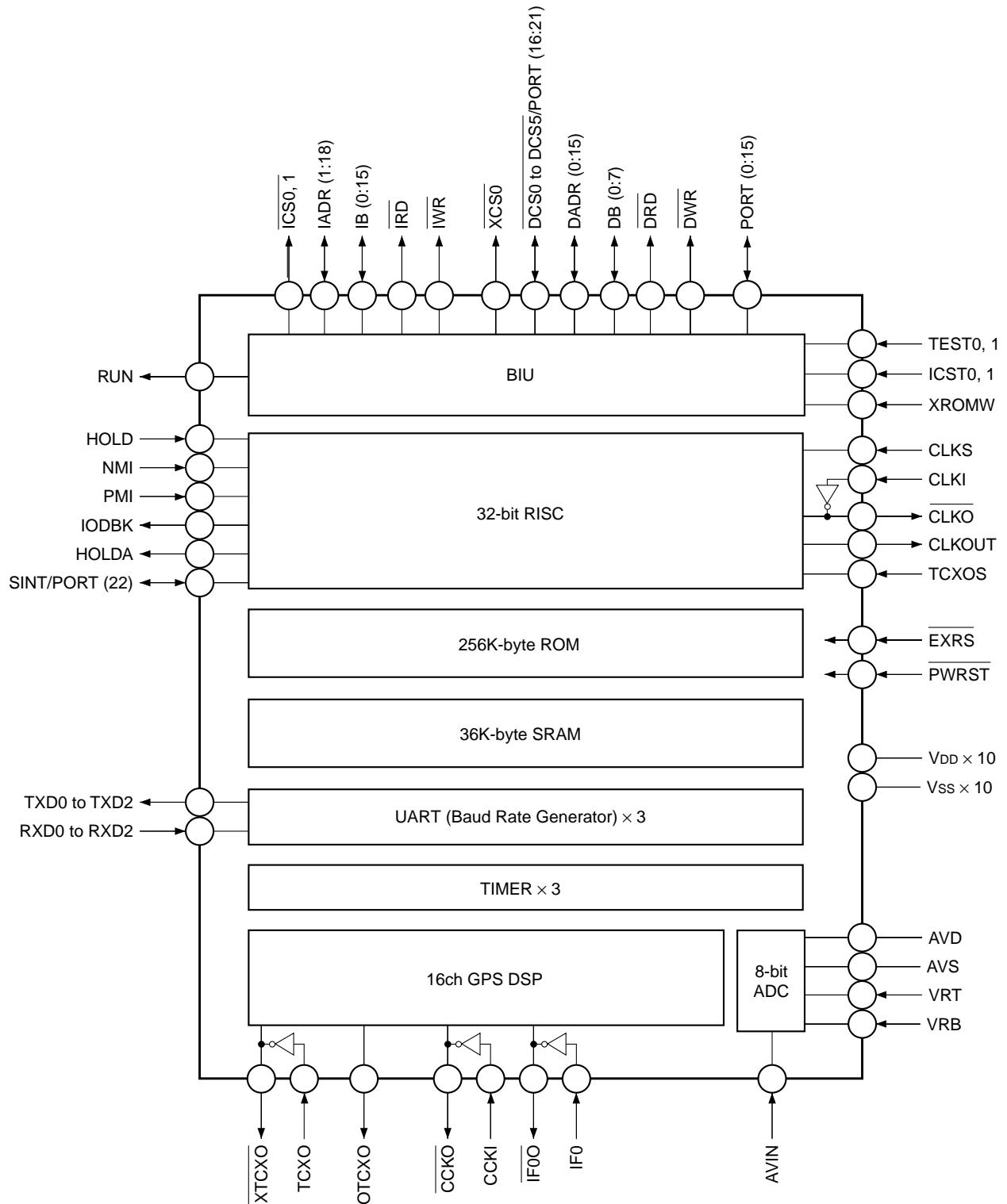
E01Z12A22-PS
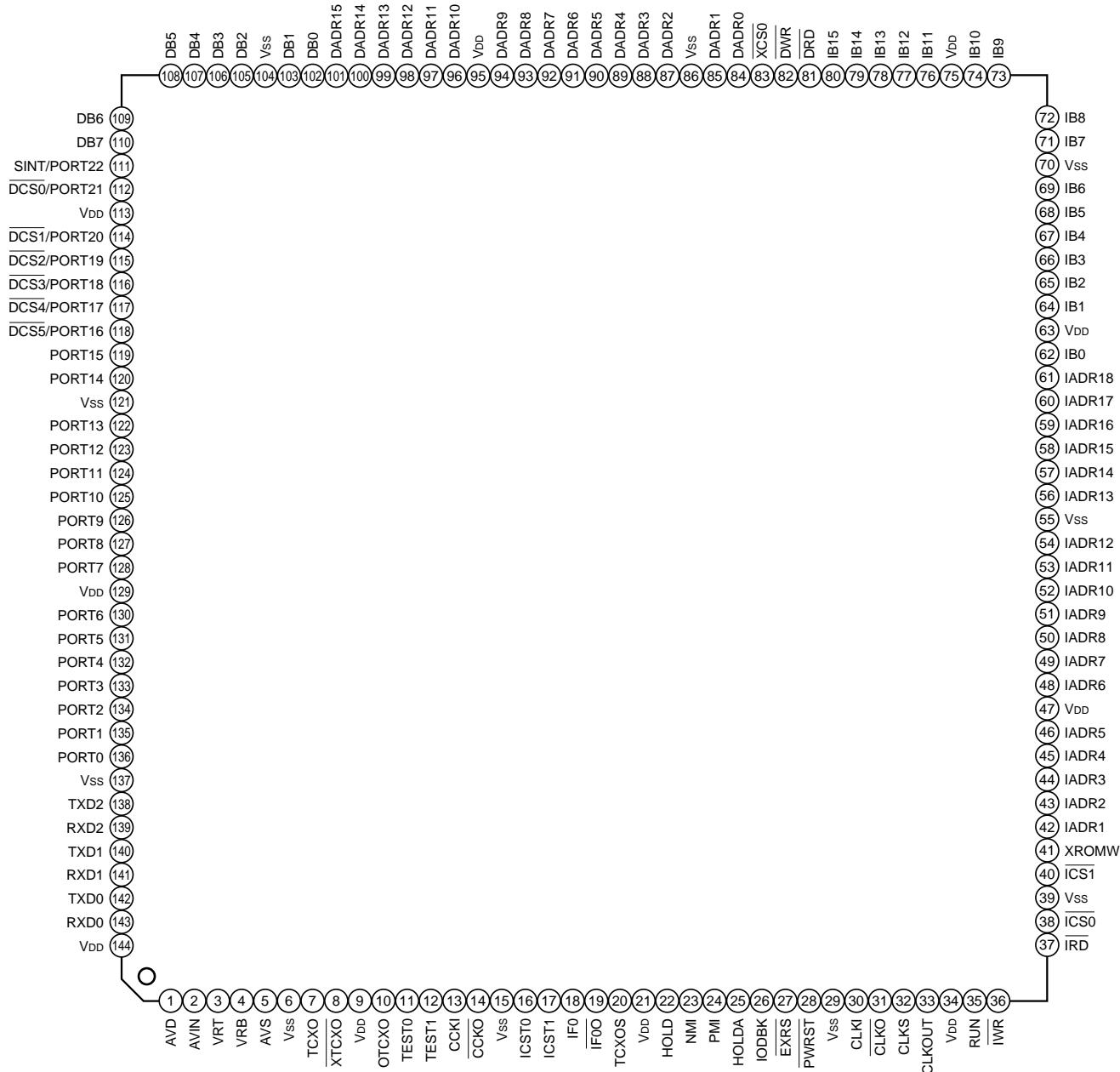
Performance

• 16-channel GPS receiver

• High performance 32-bit RISC CPU

• Receiver frequency: 1575.42MHz (L1 band, CA code)

• Reception sensitivity
    Tracking sensitivity: −145dBm (typ.) when using the antenna of 25dBi, NF = 2dB and the RF amplifier
                                     with the 25dB gain
    * Reference data using the Sony's reference board.
        This value is not guaranteed, depending on the conditions.

• Time to First Fix (time until initial measurement after power-on)
    Cold Start (without both ephemeris and almanac):   27 to 58s
    Warm Start (without ephemeris with almanac):   23 to 45s
    Hot Start (with both ephemeris and almanac):   6 to 17s
    * Reference data with elevation angle of 5° or more and no interception environment on Nov., 2001.
        Positioning time with 90% possibility.
        These values are not guaranteed, depending on the conditions.

• Positioning accuracy
    2DRMS: approx. 12m
    * Reference data with elevation angle of 5° or more and no interception environment.
        This value is not guaranteed, depending on the conditions.

• Measurement data update time
    1s

• Interfece format
    NMEA0183 (4800bps)

• Communication method
    Start-stop synchronization

• All-in-view
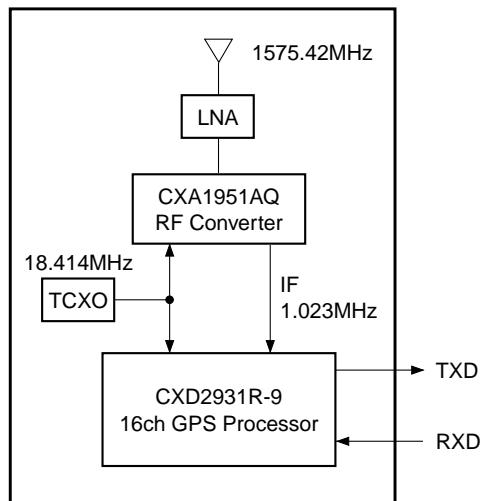
GPS receiver system block diagram using the CXD2931R-9

Block Diagram

Pin Configuration (CXD2931R-9)

Top pins (left to right):
DB5 (108), DB4 (107), DB3 (106), DB2 (105), Vss (104), DB1 (103), DB0 (102), DADR15 (101), DADR14 (100), DADR13 (99), DADR12 (98), DADR11 (97), DADR10 (96), VDD (95), DADR9 (94), DADR8 (93), DADR7 (92), DADR6 (91), DADR5 (90), DADR4 (89), DADR3 (88), DADR2 (87), Vss (86), DADR1 (85), DADR0 (84), XCS0 (83), DWR (82), DRD (81), IB15 (80), IB14 (79), IB13 (78), IB12 (77), IB11 (76), VDD (75), IB10 (74), IB9 (73)

Left side pins (top to bottom):
DB6 (109)
DB7 (110)
SINT/PORT22 (111)
DCS0/PORT21 (112)
VDD (113)
DCS1/PORT20 (114)
DCS2/PORT19 (115)
DCS3/PORT18 (116)
DCS4/PORT17 (117)
DCS5/PORT16 (118)
PORT15 (119)
PORT14 (120)
Vss (121)
PORT13 (122)
PORT12 (123)
PORT11 (124)
PORT10 (125)
PORT9 (126)
PORT8 (127)
PORT7 (128)
VDD (129)
PORT6 (130)
PORT5 (131)
PORT4 (132)
PORT3 (133)
PORT2 (134)
PORT1 (135)
PORT0 (136)
Vss (137)
TXD2 (138)
RXD2 (139)
TXD1 (140)
RXD1 (141)
TXD0 (142)
RXD0 (143)
VDD (144)

Right side pins (top to bottom):
IB8 (72)
IB7 (71)
Vss (70)
IB6 (69)
IB5 (68)
IB4 (67)
IB3 (66)
IB2 (65)
IB1 (64)
VDD (63)
IB0 (62)
IADR18 (61)
IADR17 (60)
IADR16 (59)
IADR15 (58)
IADR14 (57)
IADR13 (56)
Vss (55)
IADR12 (54)
IADR11 (53)
IADR10 (52)
IADR9 (51)
IADR8 (50)
IADR7 (49)
IADR6 (48)
VDD (47)
IADR5 (46)
IADR4 (45)
IADR3 (44)
IADR2 (43)
IADR1 (42)
XROMW (41)
ICS1 (40)
Vss (39)
ICS0 (38)
IRD (37)

Bottom pins (left to right):
AVD (1), AVIN (2), VRT (3), VRB (4), AVS (5), Vss (6), TCXO (7), XTCXO (8), VDD (9), OTCXO (10), TEST0 (11), TEST1 (12), CCKI (13), CCKO (14), Vss (15), ICST0 (16), ICST1 (17), IF0 (18), IF0O (19), TCXOS (20), VDD (21), HOLD (22), NMI (23), PMI (24), HOLDA (25), IODBK (26), EXRS (27), PWRST (28), Vss (29), CLKI (30), CLKO (31), CLKS (32), CLKOUT (33), VDD (34), RUN (35), IWR (36)

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Pin Configuration (CXD2931GA-9)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	(70) Vss	(67) IB4	(64) IB1	(62) IB0	(59) IADR16	(58) IADR15	(55) Vss	(54) IADR12	(51) IADR9	(50) IADR8	(47) VDD	(45) IADR4	(42) IADR1	(39) Vss	(34) VDD	R
	(75) VDD	(71) IB7	(68) IB5	(66) IB3	(63) VDD	(60) IADR17	(56) IADR13	(53) IADR11	(49) IADR7	(46) IADR5	(43) IADR2	(41) XROMW	(38) ICS0	(35) RUN	(31) $\overline{\text{CLKO}}$	P
	(78) IB13	(74) IB10	(72) IB8	(69) IB6	(65) IB2	(61) IADR18	(57) IADR14	(52) IADR10	(48) IADR6	(44) IADR3	(40) ICS1	(37) IRD	(36) IWR	(32) CLKS	(28) PWRST	N
	(81) DRD	(77) IB12	(73) IB9										(33) CLKOUT	(30) CLKI	(26) IODBK	M
	(83) XCS0	(79) IB14	(76) IB11										(29) Vss	(27) EXRS	(23) NMI	L
	(86) Vss	(82) DWR	(80) IB15										(25) HOLDA	(24) PMI	(22) HOLD	K
	(87) DADR2	(85) DADR1	(84) DADR0										(21) VDD	(20) TCXOS	(19) IF0O	J
	(90) DADR5	(89) DADR4	(88) DADR3										(16) ICST0	(17) ICST1	(18) IF0	H
	(91) DADR6	(92) DADR7	(93) DADR8										(12) TEST1	(13) CCKI	(15) Vss	G
	(94) DADR9	(96) DADR10	(97) DADR11										(8) $\overline{\text{XTCXO}}$	(10) OTCXO	(14) $\overline{\text{CCKO}}$	F
	(95) VDD	(99) DADR13	(101) DADR15										(4) VRB	(7) TCXO	(11) TEST0	E
	(98) DADR12	(102) DB0	(105) DB2										(1) AVD	(5) AVS	(9) VDD	D
	(100) DADR14	(104) Vss	(108) DB5	(109) DB6	(112) $\overline{\text{DCS0}}$/PORT21	(116) $\overline{\text{DCS3}}$/PORT18	(120) PORT14	(124) PORT11	(129) VDD	(133) PORT3	(137) Vss	(141) RXD1	(144) VDD	(2) AVIN	(6) Vss	C
	(103) DB1	(107) DB4	(110) DB7	(113) VDD	(115) $\overline{\text{DCS2}}$/PORT19	(118) $\overline{\text{DCS5}}$/PORT16	(121) Vss	(125) PORT10	(128) PORT7	(132) PORT4	(135) PORT1	(138) TXD2	(140) TXD1	(143) RXD0	(3) VRT	B
	(106) DB3	(111) SINT/PORT22	(114) $\overline{\text{DCS1}}$/PORT20	(117) $\overline{\text{DCS4}}$/PORT17	(119) PORT15	(122) PORT13	(123) PORT12	(126) PORT9	(127) PORT8	(130) PORT6	(131) PORT5	(134) PORT2	(136) PORT0	(139) RXD2	(142) TXD0	A

Pin Configuration

Pin No.	Symbol	I/O	Description
1	AVD	—	A/D converter power supply.
2	AVIN	I	Analog input.
3	VRT	I	Reference input.
4	VRB	I	
5	AVS	—	A/D converter GND.
6	Vss	—	GND
7	TCXO	I	TCXO binary conversion circuit/crystal oscillator.
8	$\overline{\text{XTCXO}}$	O	
9	VDD	—	Power supply.
10	OTCXO	O	TCXO clock output.
11	TEST0	I	Test. (Low level fixed)
12	TEST1	I	
13	CCKI	I	Timer oscillation. (32.768kHz ± 100ppm)
14	$\overline{\text{CCKO}}$	O	
15	Vss	—	GND
16	ICST0	I	Test. (Low level fixed)
17	ICST1	I	
18	IF0	I	IF signal binary conversion circuit.
19	IF0O	O	
20	TCXOS	I	TCXO select. (Low: TCXO/2, High: TCXO through)
21	VDD	—	Power supply.
22	HOLD	I	Hold input signal. (High: Hold)
23	NMI	I	Non maskable interrupt.
24	PMI	I	Program maskable interrupt.
25	HOLDA	O	Hold acknowledge signal.
26	IODBK	O	Break signal for debugging.
27	EXRS	I	Reset input signal.
28	PWRST	I	Connect to main power supply. Leave open during backup.
29	Vss	—	GND
30	CLKI	I	CPU clock oscillation circuit.
31	$\overline{\text{CLKO}}$	O	
32	CLKS	I	CPU clock select signal. (Low: TCXO, High: CLKI)
33	CLKOUT	O	CPU clock output.
34	VDD	—	Power supply.
35	RUN	O	Signal indicating CPU operating status.
36	IWR	O	Write signal for external expansion memory.
37	IRD	O	Read signal for external expansion memory.

Pin No.	Symbol	I/O	Description
38	ICS0	O	Chip select 0 for external expansion memory.
39	Vss	—	GND
40	ICS1	O	Chip select 1 for external expansion memory.
41	XROMW	I	Wait signal for external expansion memory. (High: Wait)
42	IADR1	I/O	(LSB)
43	IADR2	I/O	
44	IADR3	I/O	Address signal for external expansion memory.
45	IADR4	I/O	
46	IADR5	I/O	
47	VDD	—	Power supply.
48	IADR6	I/O	
49	IADR7	I/O	
50	IADR8	I/O	
51	IADR9	I/O	Address signal for external expansion memory.
52	IADR10	I/O	
53	IADR11	I/O	
54	IADR12	I/O	
55	Vss	—	GND
56	IADR13	I/O	
57	IADR14	I/O	
58	IADR15	I/O	Address signal for external expansion memory.
59	IADR16	I/O	
60	IADR17	I/O	
61	IADR18	I/O	(MSB)
62	IB0	I/O	(LSB) Data bus I/O for external expansion memory.
63	VDD	—	Power supply.
64	IB1	I/O	
65	IB2	I/O	
66	IB3	I/O	Data bus I/O for external expansion memory.
67	IB4	I/O	
68	IB5	I/O	
69	IB6	I/O	
70	Vss	—	GND
71	IB7	I/O	
72	IB8	I/O	Data bus I/O for external expansion memory.
73	IB9	I/O	
74	IB10	I/O	

Pin No.	Symbol	I/O	Description
75	V_{DD}	—	Power supply.
76	IB11	I/O	
77	IB12	I/O	
78	IB13	I/O	Data bus I/O for external expansion memory.
79	IB14	I/O	
80	IB15	I/O	(MSB)
81	DRD	O	Read signal for external expansion data memory.
82	DWR	O	Write signal for external expansion data memory.
83	XCS0	O	Chip select signal for external expansion data memory.
84	DADR0	I/O	(LSB)
85	DADR1	I/O	Address signal for external expansion data memory.
86	Vss	—	GND
87	DADR2	I/O	
88	DADR3	I/O	
89	DADR4	I/O	
90	DADR5	I/O	
91	DADR6	I/O	Address signal for external expansion data memory.
92	DADR7	I/O	
93	DADR8	I/O	
94	DADR9	I/O	
95	V_{DD}	—	Power supply.
96	DADR10	I/O	
97	DADR11	I/O	
98	DADR12	I/O	
99	DADR13	I/O	Address signal for external expansion data memory.
100	DADR14	I/O	
101	DADR15	I/O	(MSB)
102	DB0	I/O	(LSB)
103	DB1	I/O	Data bus I/O for external expansion data memory.
104	Vss	—	GND
105	DB2	I/O	
106	DB3	I/O	
107	DB4	I/O	
108	DB5	I/O	Data bus I/O for external expansion data memory.
109	DB6	I/O	
110	DB7	I/O	(MSB)

Pin No.	Symbol	I/O	Description
111	SINT/PORT22	I/O	External interrupt input signal/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
112	$\overline{DCS0}$/PORT21	I/O	Chip select for external expansion data memory/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
113	V$_{DD}$	—	Power supply.
114	$\overline{DCS1}$/PORT20	I/O	Chip select for external expansion data memory/general-purpose I/O port. These pins can be used as a general-purpose I/O port according to the internal registers.
115	$\overline{DCS2}$/PORT19	I/O	
116	$\overline{DCS3}$/PORT18	I/O	
117	$\overline{DCS4}$/PORT17	I/O	
118	$\overline{DCS5}$/PORT16	I/O	
119	PORT15	I/O	General-purpose I/O port.
120	PORT14	I/O	
121	Vss	—	GND
122	PORT13	I/O	General-purpose I/O port.
123	PORT12	I/O	
124	PORT11	I/O	
125	PORT10	I/O	
126	PORT9	I/O	
127	PORT8	I/O	
128	PORT7	I/O	
129	V$_{DD}$	—	Power supply.
130	PORT6	I/O	General-purpose I/O port.
131	PORT5	I/O	
132	PORT4	I/O	
133	PORT3	I/O	
134	PORT2	I/O	
135	PORT1	I/O	
136	PORT0	I/O	
137	Vss	—	GND
138	TXD2	O	UART transmission data output. (channel 2)
139	RXD2	I	UART reception data input. (channel 2)
140	TXD1	O	UART transmission data output. (channel 1)
141	RXD1	I	UART reception data input. (channel 1)
142	TXD0	O	UART transmission data output. (channel 0)
143	RXD0	I	UART reception data input. (channel 0)
144	V$_{DD}$	—	Power supply.

A/D Converter Characteristics

(0 < VRB < VIN < VRT < AVD = 3.0 to 3.6V, Topr = −40 to +85°C)

Item	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution					8	Bit
Differential linearity error (DLE)		AVD = 3.0V	−0.5		+0.5	LSB
Integral linearity error (ILE)			−2.5		+2.5	LSB
Sampling time		f = 18.414MHz	648			ns
Conversion time			864			ns
Current consumption		AVD = 3.0V		2.0		mA

Electrical Characteristics

DC Characteristics

(V_{DD} = 3.0 to 3.6V, Topr = −40 to +85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Input voltage (1) (CMOS level)	High level	V_{IH} (1)		$0.7 \times V_{DD}$		V_{DD}	V	*1
	Low level	V_{IL} (1)				$0.2 \times V_{DD}$	V	
Input voltage (2) (5V interface)	High level	V_{IH} (2)		$0.7 \times V_{DD}$		5.5	V	*2
	Low level	V_{IL} (2)				$0.2 \times V_{DD}$	V	
Output voltage (1)	High level	V_{OH} (1)	I_{OH} = −4.0mA	V_{DD} − 0.4			V	*3
	Low level	V_{OL} (1)	I_{OL} = 4.0mA			0.4	V	
Output voltage (2)	High level	V_{OH} (2)	I_{OH} = −2.0mA	V_{DD} − 0.8			V	*4
	Low level	V_{OL} (2)	I_{OL} = 4.0mA			0.4	V	
Output voltage (3)	High level	V_{OH} (3)	I_{OH} = −2.0mA	V_{DD} − 0.8			V	*5
	Low level	V_{OL} (3)	I_{OL} = 8.0mA			0.4	V	
Current consumption in standby mode (Using external timer, +85°C)		ISTB	V_{DD} = 3.0V		20	70	µA	—
			V_{DD} = 1.8V		4	50		
Supply current		IDD	f = 18.414MHz		55		mA	—

Applicable pins

*1 Pins 11, 12, 16, 17, 20, 28, 32, 41

*2 Pins 22 to 24, 27, 62, 64 to 69, 71 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122, 128, 130 to 136, 139, 141, 143

*3 Pins 10, 25, 26, 33, 35

*4 Pins 38, 40, 82, 83, 138, 140, 142

*5 Pins 36, 37, 42 to 46, 48 to 54, 56 to 62, 64 to 69, 71 to 74, 76 to 81, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122 to 128, 130 to 136

Battery Backup Mode

The battery backup mode is activated when the power for the GPS receiver is turned off and power-on reset goes to low level. The timer clock continues to operate even when power-on reset goes low, but all other clock are fixed high and the LSI is set to the low power consumption mode. At this time, the RAM data is held and the registers are initialized.
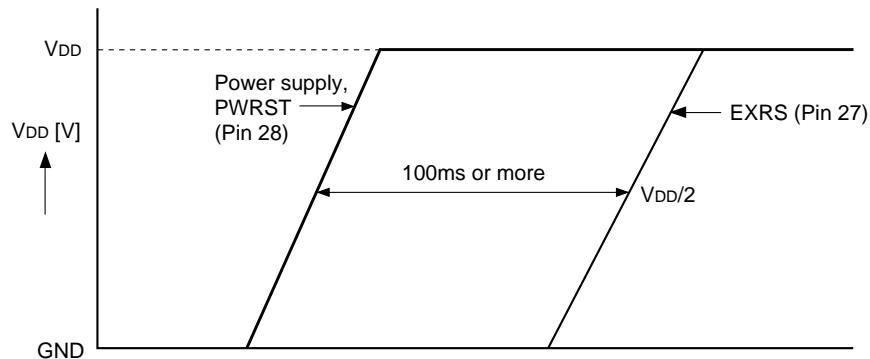
Battery backup mode is canceled by setting power-on reset to high.
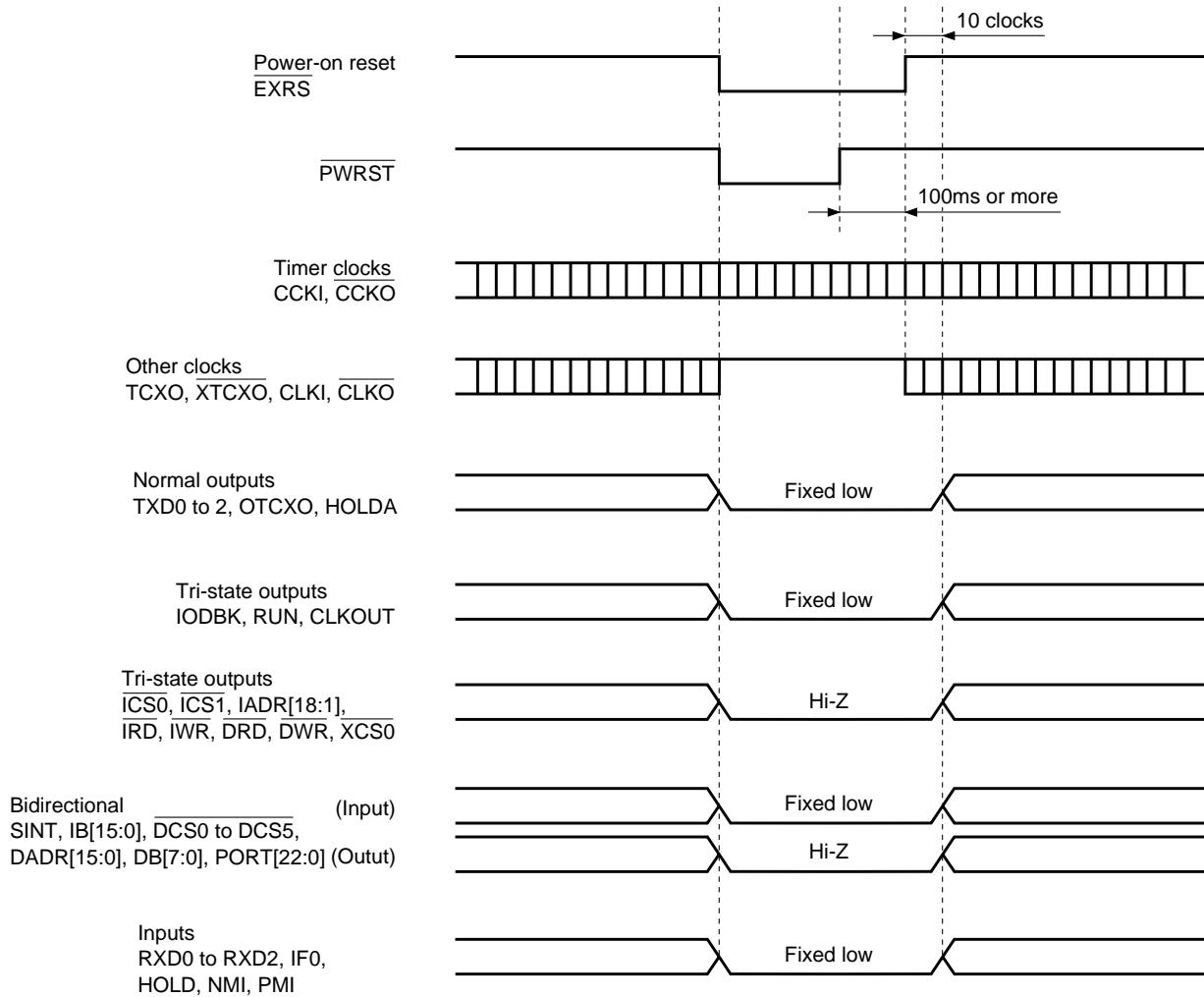
CXD2931R-9/GA-9 Initialization
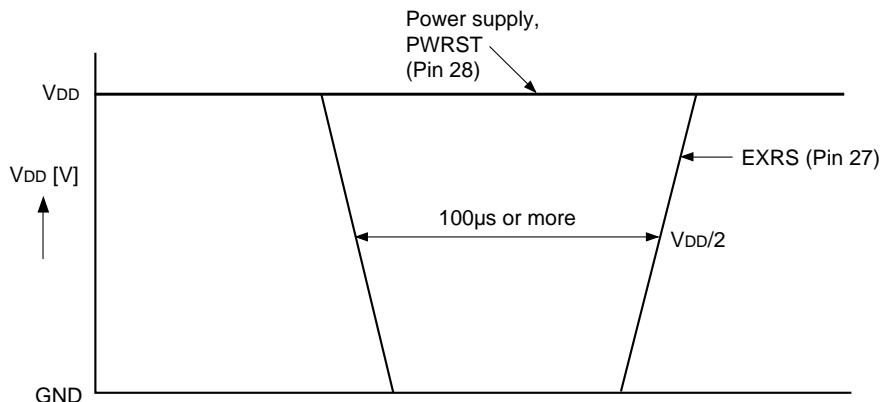
CXD2931R-9/GA-9 initialization is started by setting the reset input signal EXRS (Pin 27) to low level. The timing should satisfy the conditions noted below.

1. During power-on (power-on reset) (V_{DD} = 3.0 to 3.6V, Topr = −40 to +85°C)

The PWRST (Pin 28) signal should rise simultaneously with the power supply. The EXRS (Pin 27) signal should rise 100ms or more after the power supply and the PWRST signal have risen. Note that the PWRST signal should be left open during battery backup.

2. Initialization during operation (V_{DD} = 3.0 to 3.6V, Topr = −40 to +85°C)

The internal registers can be initialized during operation by setting the EXRS (Pin 27) signal to low level for 100μs or more. Keep the PWRST (Pin 28) signal at high level at this time.

• **External Command Fetch Timing (XROMW = 0)**
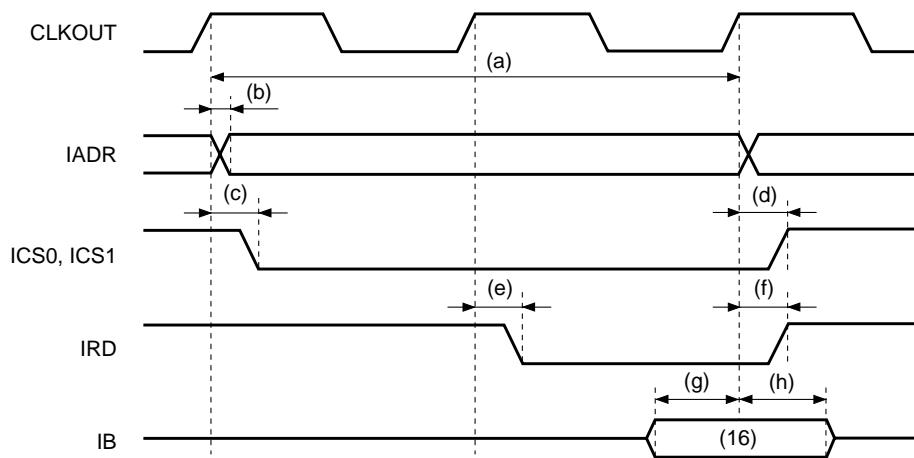
No.	Item	Min.	Typ.	Max.	Unit
(a)	Read cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	10	ns
(e)	Read signal fall delay time	0	—	3	ns
(f)	Read signal rise delay time	0	—	5	ns
(g)	Read data setup time	11	—	—	ns
(h)	Read data hold time	0	—	—	ns

* The load capacitance = 30pF.

• **External Command Fetch Timing (XROMW = 1)**
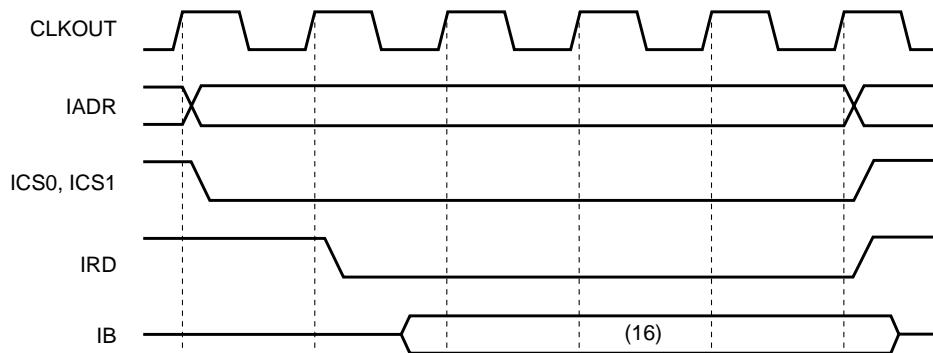
• **External Data Access Timing (ICS0, ICS1/XROMW = 0)**

(1) Read (half-word access/XROMW = 0)
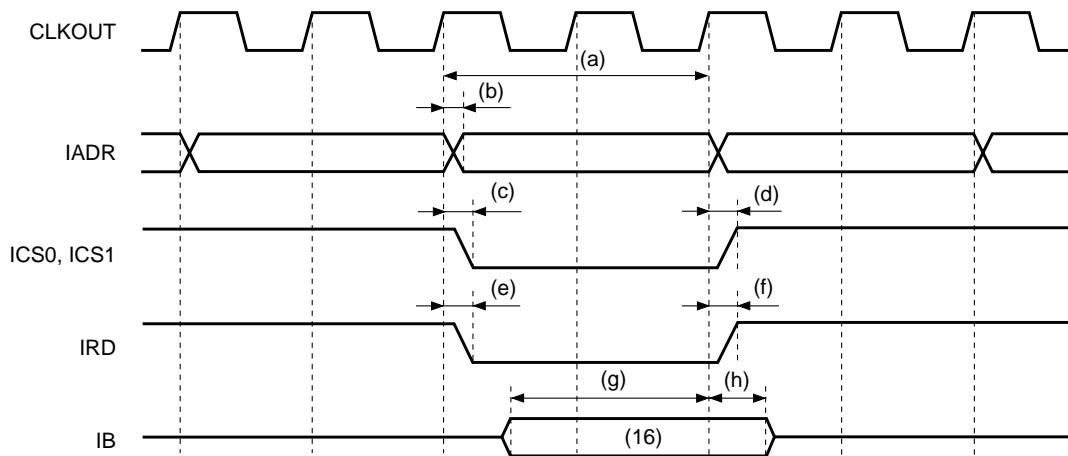
(2) Write (half-word access/XROMW = 0)

No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	10	ns
(e)	Read signal fall delay time	0	—	3	ns
(f)	Read signal rise delay time	0	—	5	ns
(g)	Read data setup time	11	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	5	ns
(l)	Write data hold time	5	—	—	ns

* The load capacitance = 30pF.

(3) Read (word access/XROMW = 0)

CLKOUT	
IADR	
ICS0, ICS1	
IRD	
IB	H (16)　　L (16)

(4) Write (word access/XROMW = 0)

CLKOUT	
IADR	
ICS0, ICS1	
IWR	
IB	L (16)　　H (16)
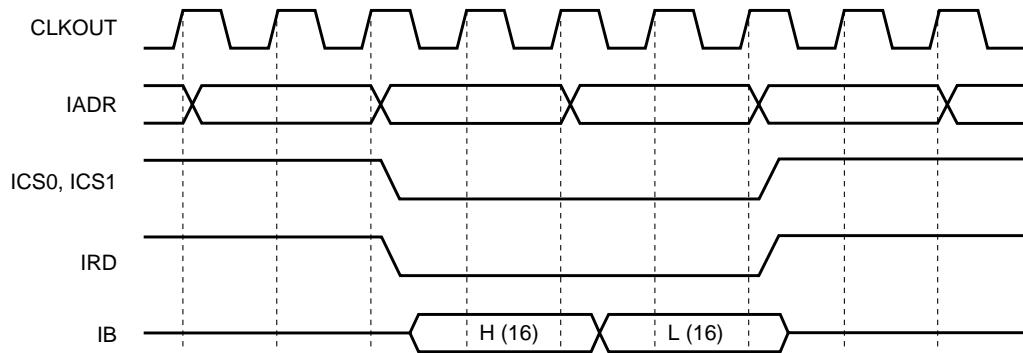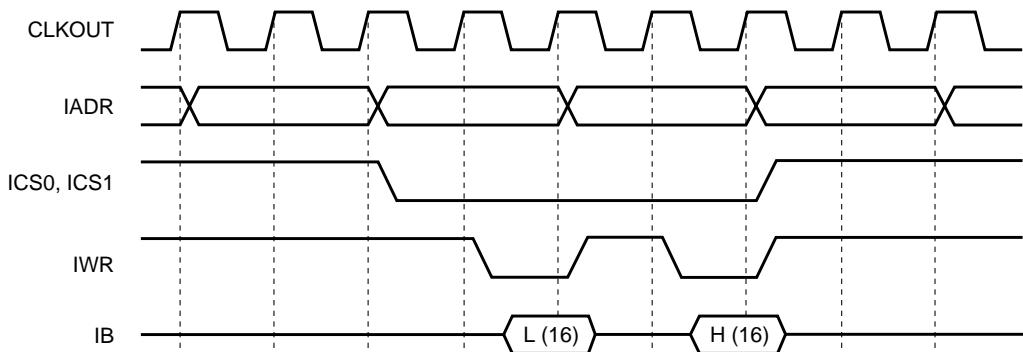
• **External Data Access Timing (ICS0, ICS1/XROMW = 1)**

(1) Read (half-word access/XROMW = 1)

CLKOUT

IADR

ICS0, ICS1

IRD

IB   (16)

(2) Write (half-word access/XROMW = 1)

CLKOUT

IADR

ICS0, ICS1

IWR

IB   (16)

(3) Read (word access/XROMW = 1)

CLKOUT

IADR

ICS0, ICS1

IRD

IB   H (16)   L (16)

(4) Write (word access/XROMW = 1)

CLKOUT

IADR

ICS0, ICS1

IWR

IB   L (16)   H (16)
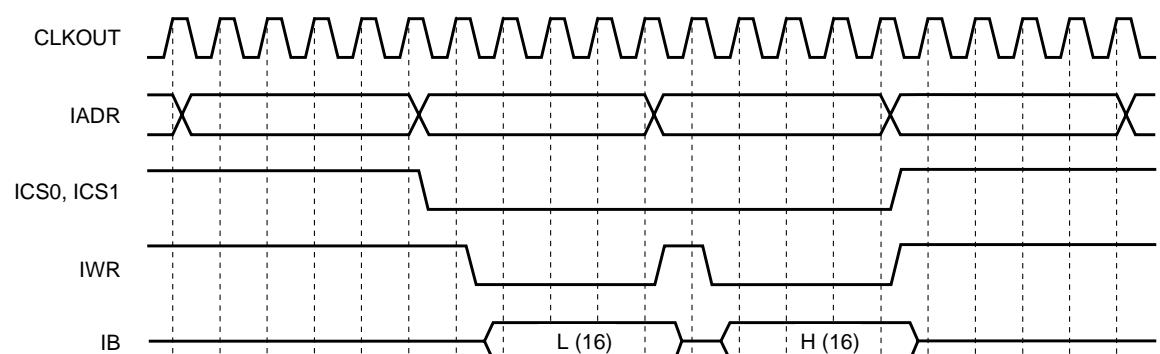
• **External Data Access Timing (XCS0, DCS0 to DCS5/no data wait)**
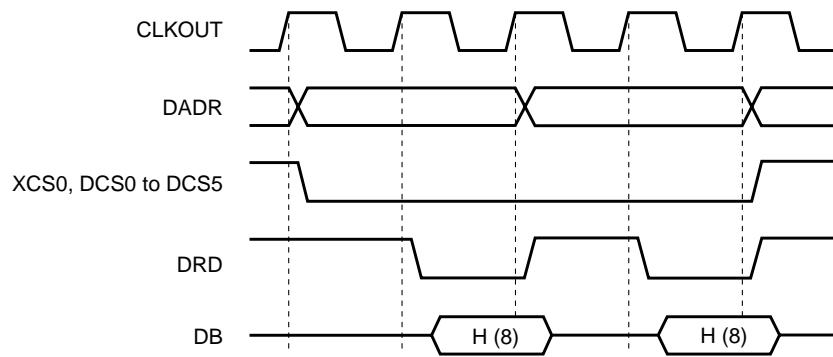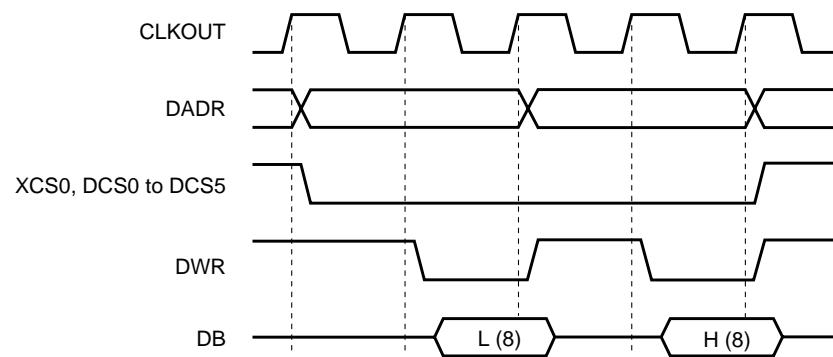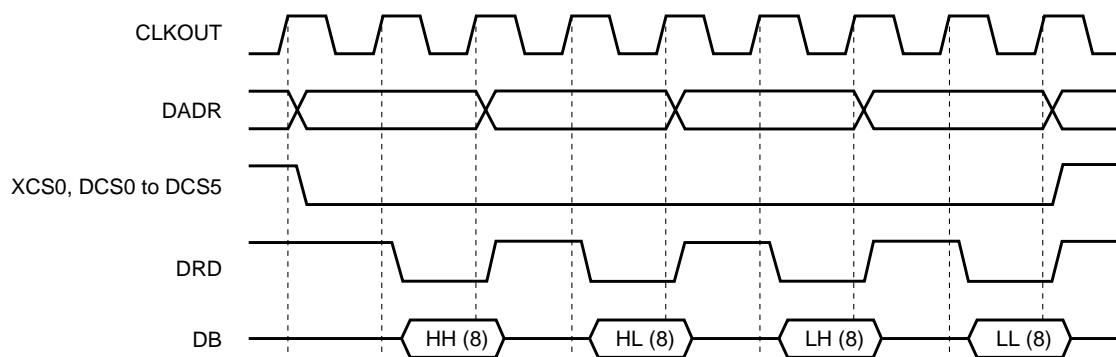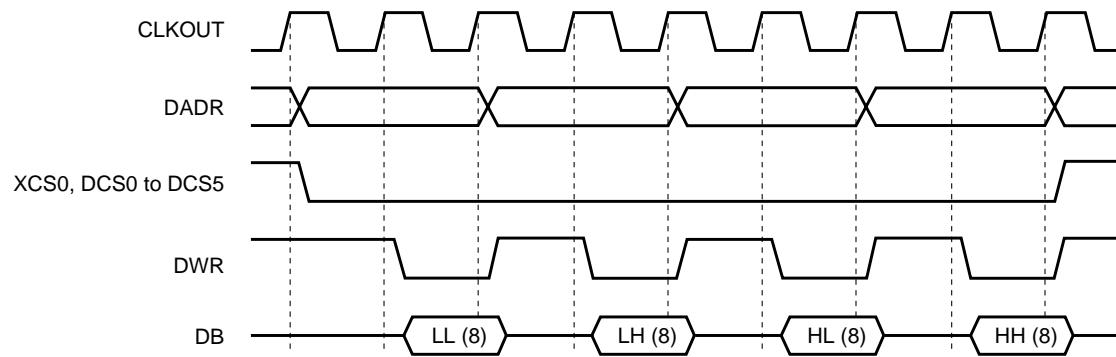
(1) Read (byte access/no data wait)
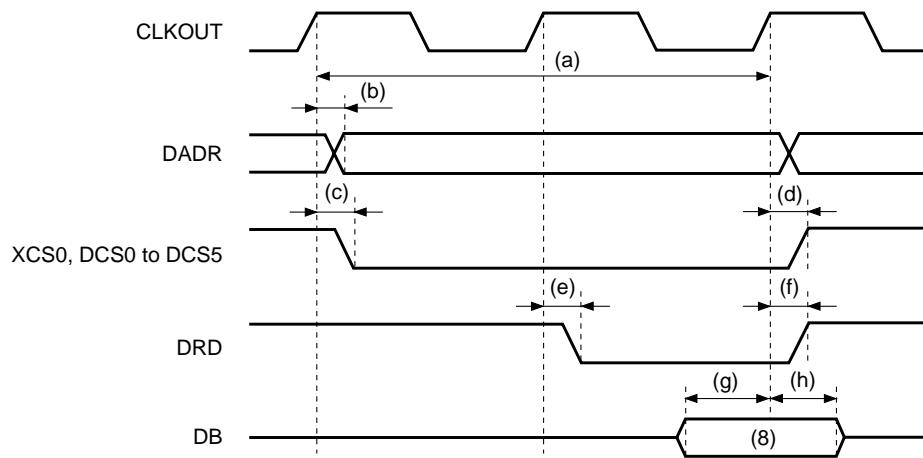
(2) Write (byte access/no data wait)
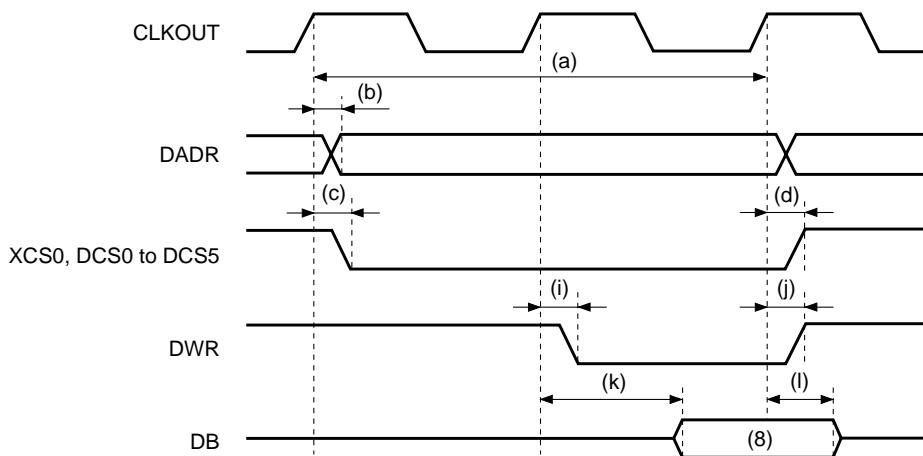
No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	12	ns
(c)	Chip select fall delay time	3	—	13	ns
(d)	Chip select rise delay time	3	—	13	ns
(e)	Read signal fall delay time	2	—	8	ns
(f)	Read signal rise delay time	2	—	10	ns
(g)	Read data setup time	16	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	2	ns
(j)	Write signal rise delay time	0	—	3	ns
(k)	Write data established time	—	—	12	ns
(l)	Write data hold time	5	—	—	ns

* The load capacitance = 30pF.

(3) Read (half-word access/no data wait)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   H (8)   H (8)

(4) Write (half-word access/no data wait)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   L (8)   H (8)

(5) Read (word access/no data wait)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   HH (8)   HL (8)   LH (8)   LL (8)

(6) Write (word access/no data wait)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   LL (8)   LH (8)   HL (8)   HH (8)

• **External Data Access Timing (XCS0, DCS0 to DCS5/data wait = 1)**

(1) Read (byte access/data wait = 1)
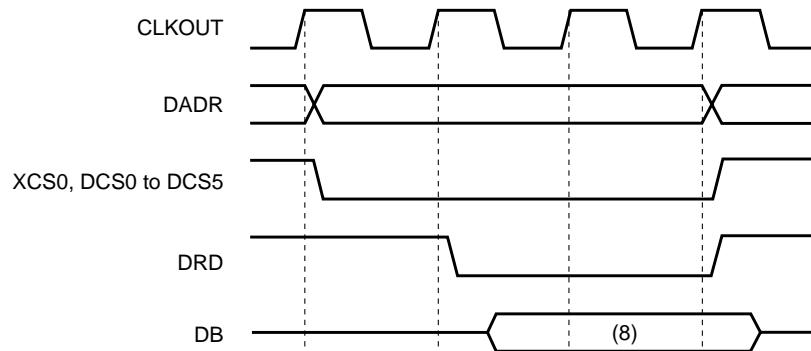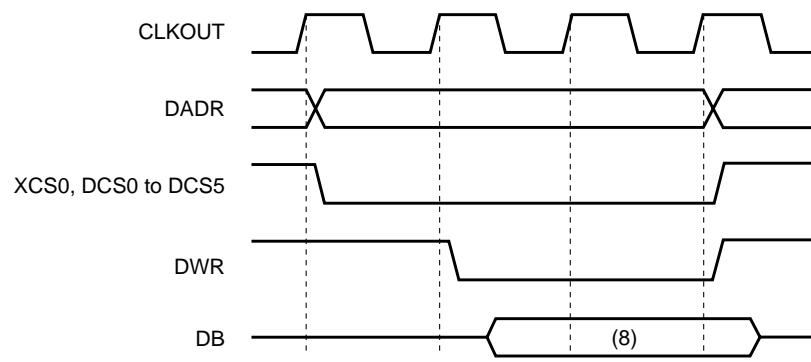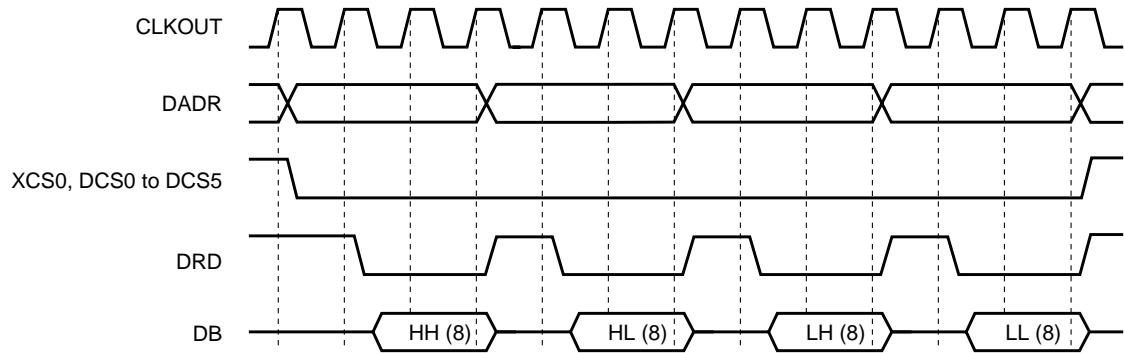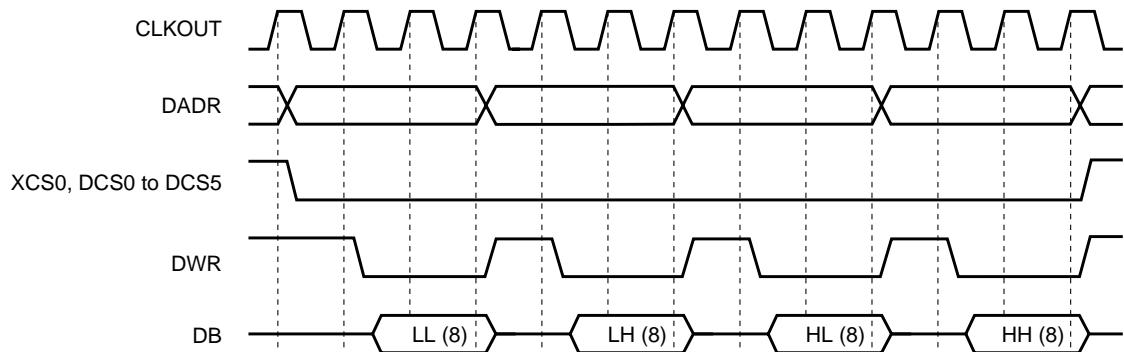
CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   (8)

(2) Write (byte access/data wait = 1)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   (8)

(3) Read (half-word access/data wait = 1)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   H (8)   L (8)

(4) Write (half-word access/data wait = 1)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   L (8)   H (8)

(5) Read (word access/data wait = 1)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB — HH (8) — HL (8) — LH (8) — LL (8) —

(6) Write (word access/data wait = 1)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB — LL (8) — LH (8) — HL (8) — HH (8) —
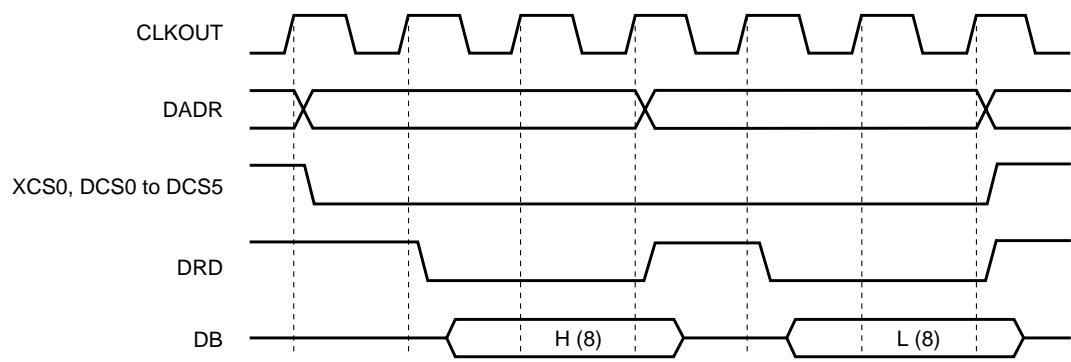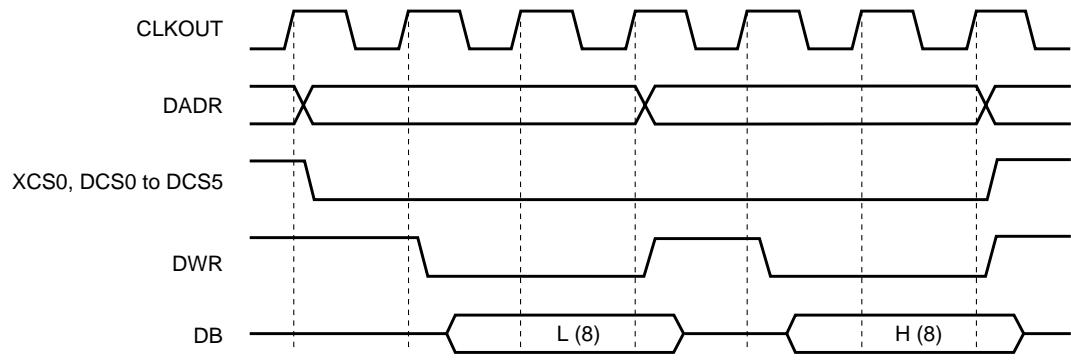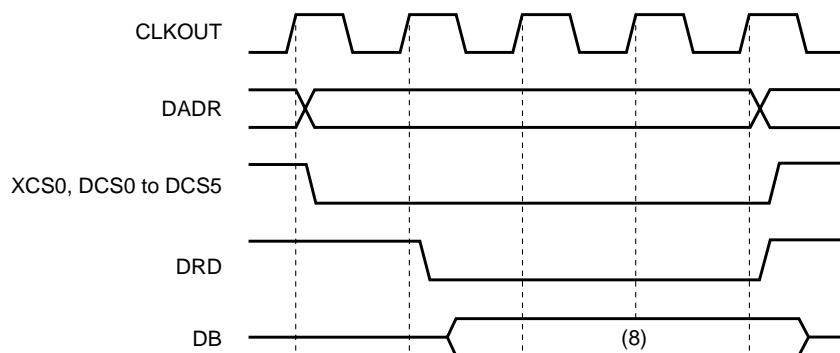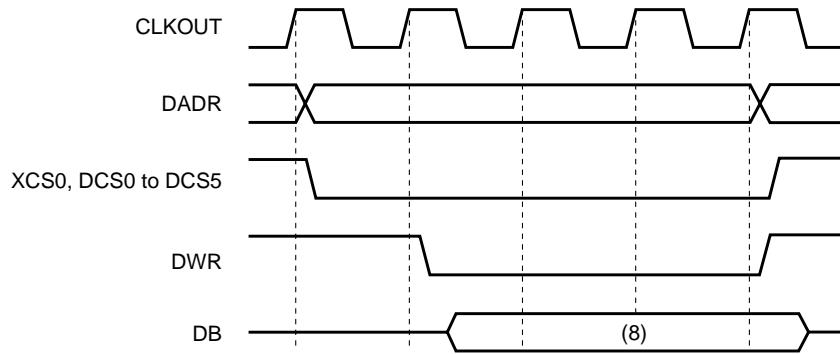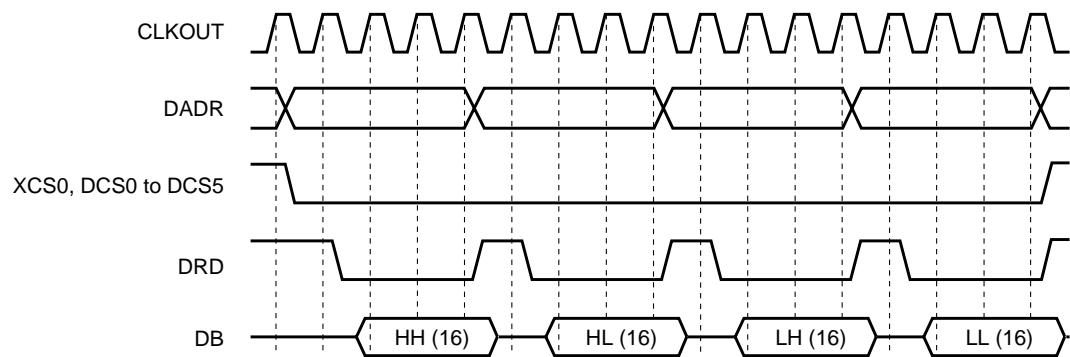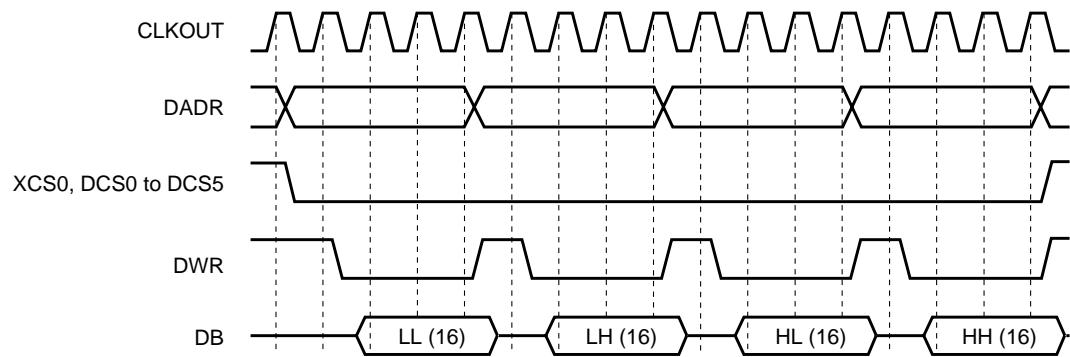
• **External Data Access Timing (XCS0, DCS0 to DCS5/data wait = 2)**

(1) Read (byte access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB — (8) —

(2) Write (byte access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB — (8) —

(3) Read (half-word access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   H (8)   L (8)

(4) Write (half-word access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   L (8)   H (8)

(5) Read (word access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DRD

DB   HH (16)   HL (16)   LH (16)   LL (16)

(6) Write (word access/data wait = 2)

CLKOUT

DADR

XCS0, DCS0 to DCS5

DWR

DB   LL (16)   LH (16)   HL (16)   HH (16)
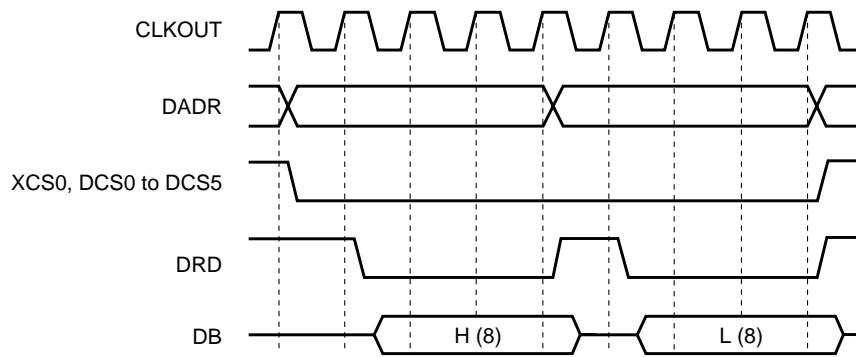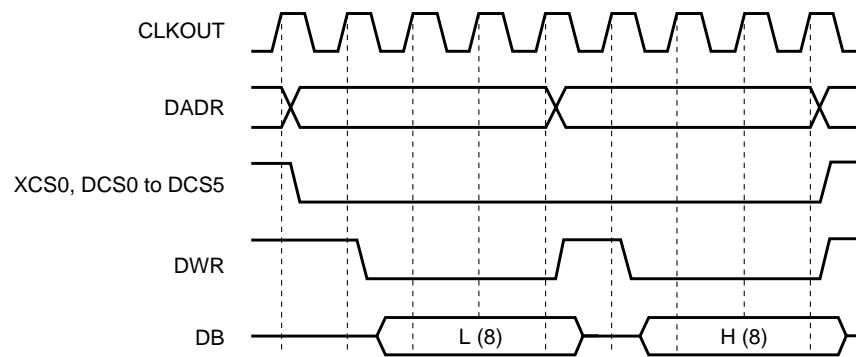
Application Notes

The constants shown in the circuits below are the examples, and do not guarantee the circuit operation.

1. TCXO input

(1) When inputting the binary-converted signal
     The TCXO (Pin 7) input signal should be 18.414MHz ± 3ppm.

Input ——— (7)

Open (8)
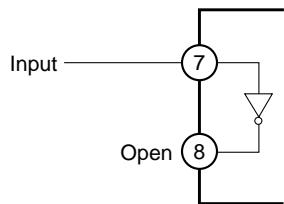
(2) When performing the self-oscillation with the TCXO and XTCXO pins (Pins 7 and 8)
     The TCXO (Pin 7) input signal should be 18.414MHz ± 3ppm.

0.01µF
TCXO —||— (7)

1MΩ

(8)
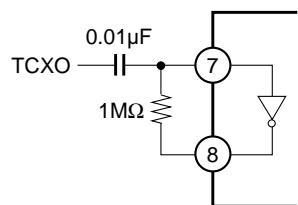
2. CPU clock generation
     Pin 32 is used to select that TCXO is used or that the self-oscillation is performed with the MCKI and
     $\overline{\text{MCKO}}$ pins (Pins 30 and 31).

(1) TCXO solution (TCXO is used for CPU clock)
     Set Pin 32 to low.
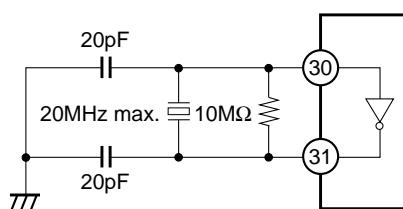
   Pin 30: Low
         Pin 31: Open

(2) When performing the self-oscillation with the MCKI and $\overline{\text{MCKO}}$ pins (Pins 30 and 31)
     Set Pin 32 to high.
     The crystal frequency should be less than 20MHz.
     The following circuit is just a reference, and is not guaranteed.

20pF
—||—   (30)
20MHz max. 10MΩ
—||—   (31)
20pF

(3) Using internal clock

Set PORT5 (Pin 131) to high.

Connect the external parts as follows when performing the self-oscillation with the CCKI and CCKO pins (Pins 13 and 14).

(4) Input IF signal

SONY
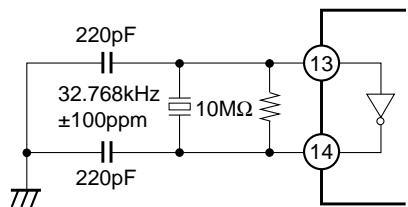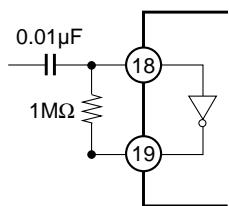
Description of Application Circuit

See the Application Circuit when using the CXD2931R-9/GA-9 to configure a GPS receiver.
Points for caution are as follows.

1. Unused pins
   Software processing is performed to prevent undesired current from flowing to unused pins in the circuit diagram, so leave these pins open.

2. TCXO input
   The TCXO frequency is 18.414MHz ± 3ppm. Signals that have not been binary-converted should be input via a DC filter capacitor (C19 in the circuit diagram). Input binary-converted signals directly to Pin 7 (TCXO) without passing through C19 or R1 in the circuit diagram.
   Make sure the input level at this time satisfies the Electrical Characteristics.

3. IF input
   The CXD2931R-9/GA-9 interface is 1.023MHz, and does not accept other frequencies. Signals that have not been binary-converted should be input via a DC filter capacitor (C20). Input binary-converted signals directly to Pin 18 (IF0) without passing through C20 or R3 in the circuit diagram.
   Make sure the input level at this time satisfies the Electrical Characteristics.

4. TXD (SIO output)
   The TXD amplitude low level is 0.4V or less, and the high level is V_{DD} – 0.4V (V_{DD} = 3.0 to 3.6V) or more. When the LSI, etc., connected to TXD operates at 5V and has a CMOS input level, perform 3 to 5V conversion before inputting the signal.

5. Real-time clock
   The current software version uses an external real-time clock. Consult your Sony representative beforehand when using the internal real-time clock. When using an external real-time clock, connect Pin 13 (CCKI) to GND.

Application Circuit

Recommended components
IC1: CXD2931R-9/GA-9
IC2: Real-time clock
    Made by RICOH (RS5C313)
IC3: Voltage regulator (for step-down transformation)
    Made by SEIKO INSTRUMENTS (S81218SG,
    steps down 3V to 1.8V)
TCXO: Made by Tokyo Denpa
    Oscillator frequency: 18.414MHz ± 3ppm
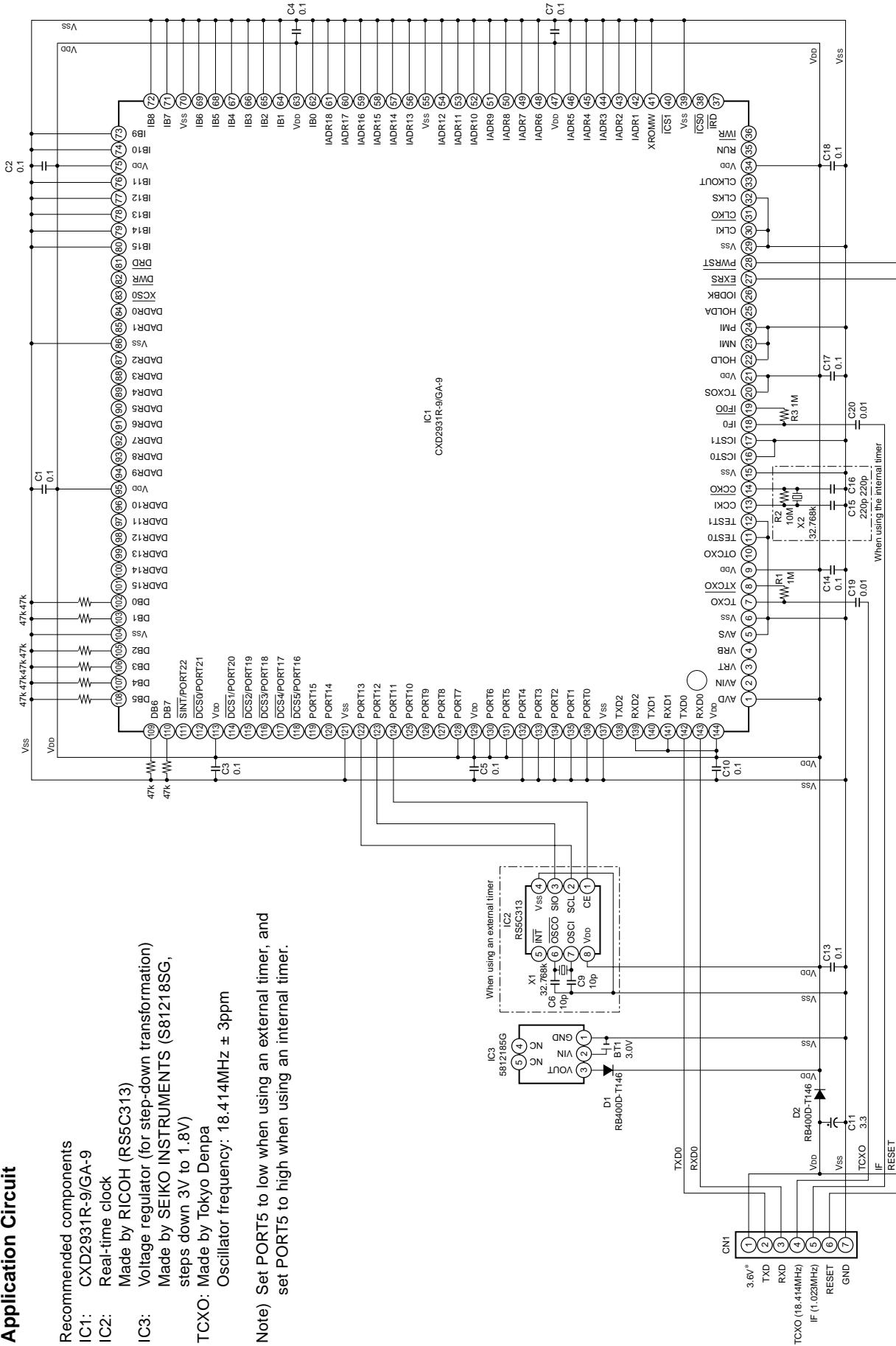
Note) Set PORT5 to low when using an external timer, and
    set PORT5 to high when using an internal timer.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

* Input 3.6V in consideration of voltage step-down by diode (D2).

Package Outline   Unit: mm

CXD2931R-9

144PIN LQFP (PLASTIC)

□ 22.0 ± 0.2
□ 20.0 ± 0.1
1.7 MAX
1.4 ± 0.1

108   73
109   72
144   37
1   0.5   36

b

⊕ | 0.08 Ⓜ | S

⌒ | 0.1 | S

S

0.1 ± 0.05

(21.0)

0˚ to 10˚

0.5 ± 0.15

DETAIL **A**

b = 0.20 ± 0.03

0.125 ± 0.04

DETAIL **B**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.3 g

SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

Package Outline   Unit: mm

CXD2931GA-9

144PIN LFLGA

DETAIL **X**
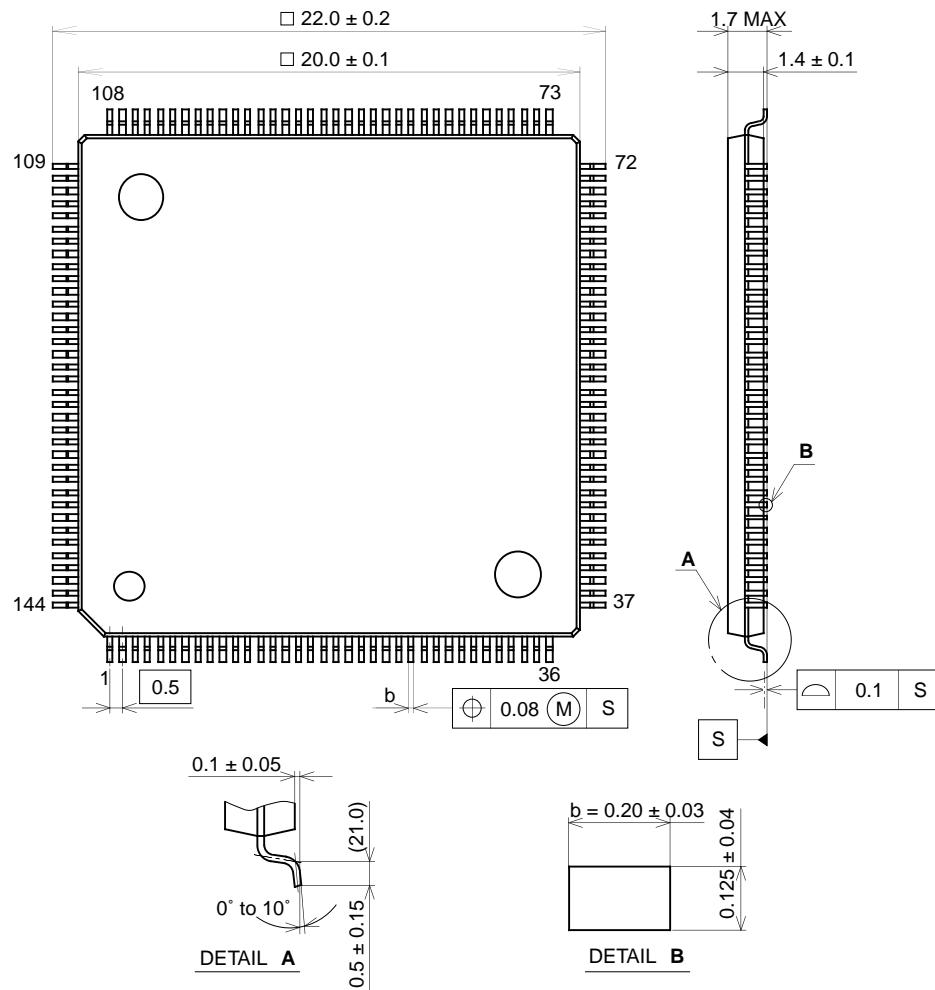
PACKAGE STRUCTURE

SONY CODE	LFLGA-144P-01
EIAJ CODE	P-LFLGA144-13x13-0.8
JEDEC CODE	————

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.5g