

## 74AC377, 74ACT377 Octal D-Type Flip-Flop with Clock Enable

### Features

- $I_{CC}$  reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

### General Description


The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ( $\overline{CE}$ ) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{CE}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

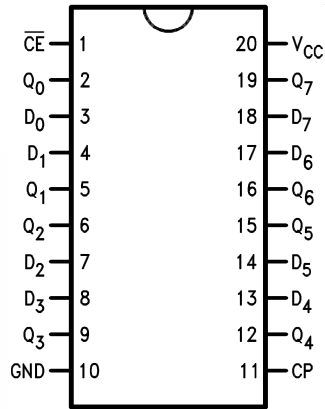
### Ordering Information

Order Number	Package Number	Package Description
74AC377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

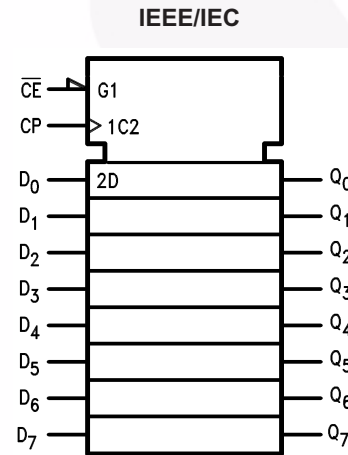
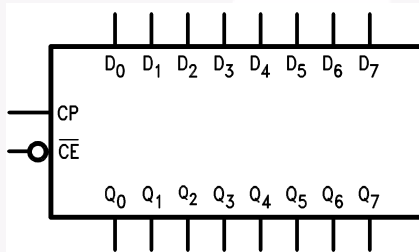
### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs
CP	Clock Pulse Input

### Logic Symbols



### Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D <sub>n</sub>	Q <sub>n</sub>
Load '1'	↗	L	H	H
Load '0'	↗	L	L	L
Hold (Do Nothing)	↗	H	X	No Change
	X	H	X	No Change

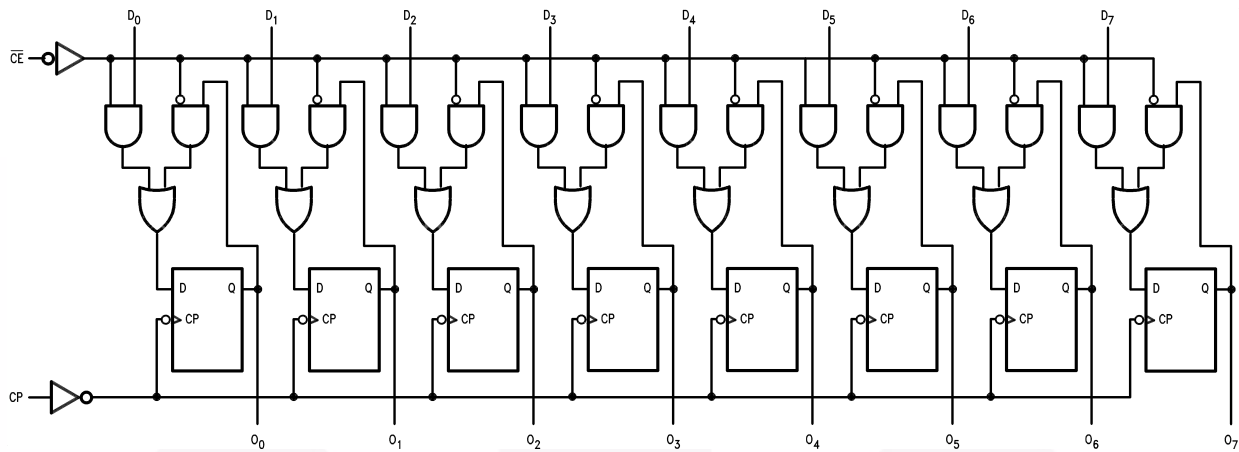
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -12mA		2.56	2.46			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1		V	
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA		0.36	0.44			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44		
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA	
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA	

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	± 1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max. V <sub>OHD</sub> = 3.85V Min.			75		mA
						-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(6)</sup>	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
			Min.	Typ.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3	90	125		75		MHz
		5.0	140	175		125		
t <sub>PLH</sub>	Propagation Delay, CP to Q <sub>n</sub>	3.3	3.0	8.0	13.0	1.5	14.0	ns
		5.0	2.0	6.0	9.0	1.5	10.0	
t <sub>PHL</sub>	Propagation Delay, CP to Q <sub>n</sub>	3.3	3.5	8.5	13.0	2.0	14.5	ns
		5.0	2.5	6.5	10.0	1.5	11.0	

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Typ.	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW, D <sub>n</sub> to CP	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to CP	3.3	-2.0	0	0		ns
		5.0	-1.0	1.0	1.0		
t <sub>S</sub>	Setup Time, HIGH or LOW, CE to CP	3.3	4.0	6.0	7.5		ns
		5.0	2.5	4.0	4.5		
t <sub>H</sub>	Hold Time, HIGH or LOW, CE to CP	3.3	-3.5	0	0		ns
		5.0	-2.0	1.0	1.0		
t <sub>W</sub>	CP Pulse Width, HIGH or LOW	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		

**Note:**

7. Voltage range 3.3 is 3.0V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

**AC Electrical Characteristics for ACT**

Symbol	Parameter	$V_{CC}$ (V) <sup>(8)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Clock Frequency	5.0	140	175		125		MHz
$t_{PLH}$	Propagation Delay, CP to $Q_n$	5.0	3.0	6.5	9.0	2.5	10.0	ns
$t_{PHL}$	Propagation Delay, CP to $Q_n$	5.0	3.5	7.0	10.0	2.5	11.0	ns

**Note:**8. Voltage Range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ **AC Operating Requirements for ACT**

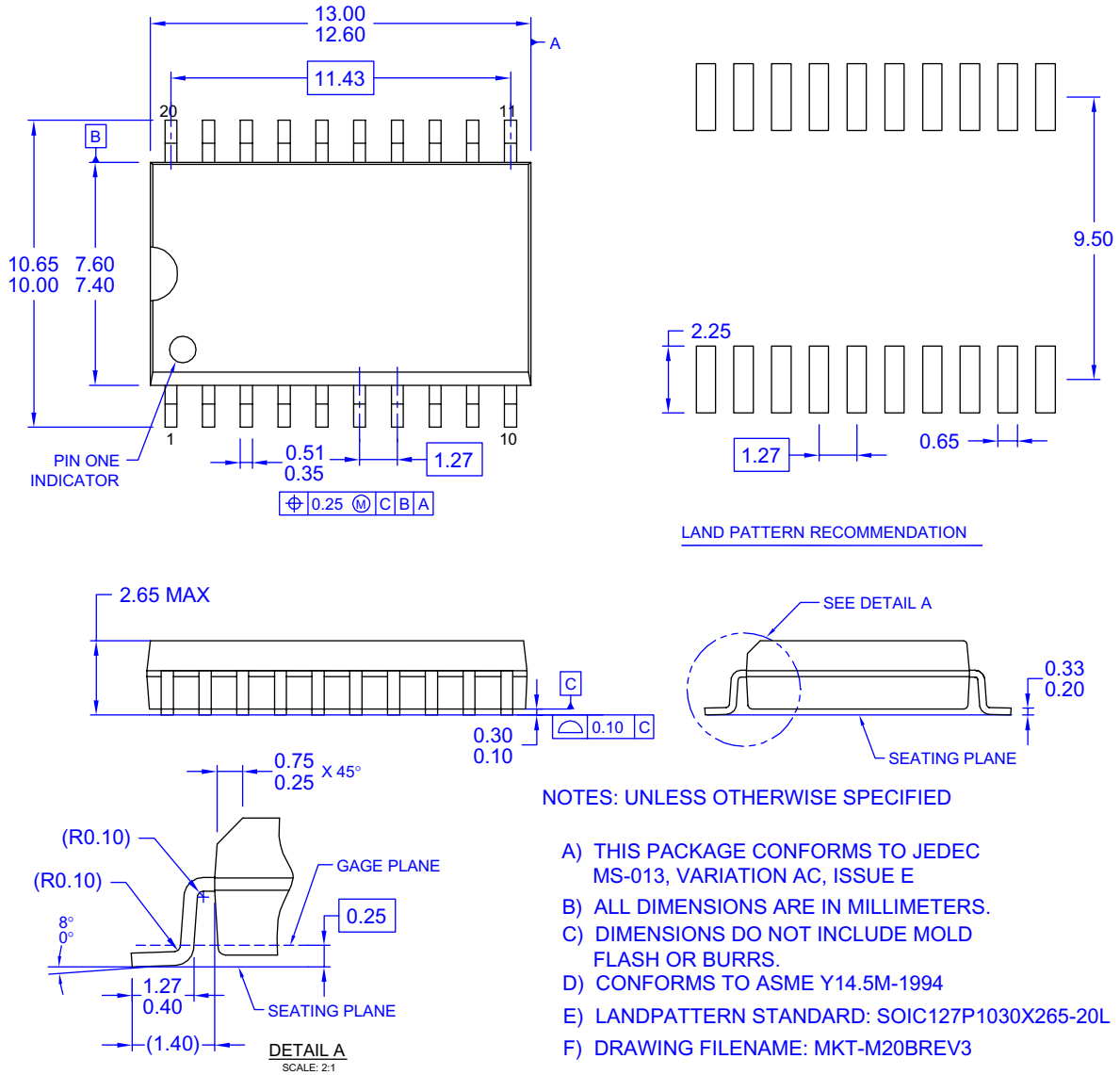
Symbol	Parameter	$V_{CC}$ (V) <sup>(9)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
$t_S$	Setup Time, HIGH or LOW, $D_n$ to CP	5.0	2.5	4.5	5.5		ns
$t_H$	Hold Time, HIGH or LOW, $D_n$ to CP	5.0	-1.0	1.0	1.0		ns
$t_S$	Setup Time, HIGH or LOW, $\overline{CE}$ to CP	5.0	2.5	4.5	5.5		ns
$t_H$	Hold Time, HIGH or LOW, $\overline{CE}$ to CP	5.0	-1.0	1.0	1.0		ns
$t_W$	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.5		ns

**Note:**9. Voltage Range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ **Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	90.0	pF



## Physical Dimensions



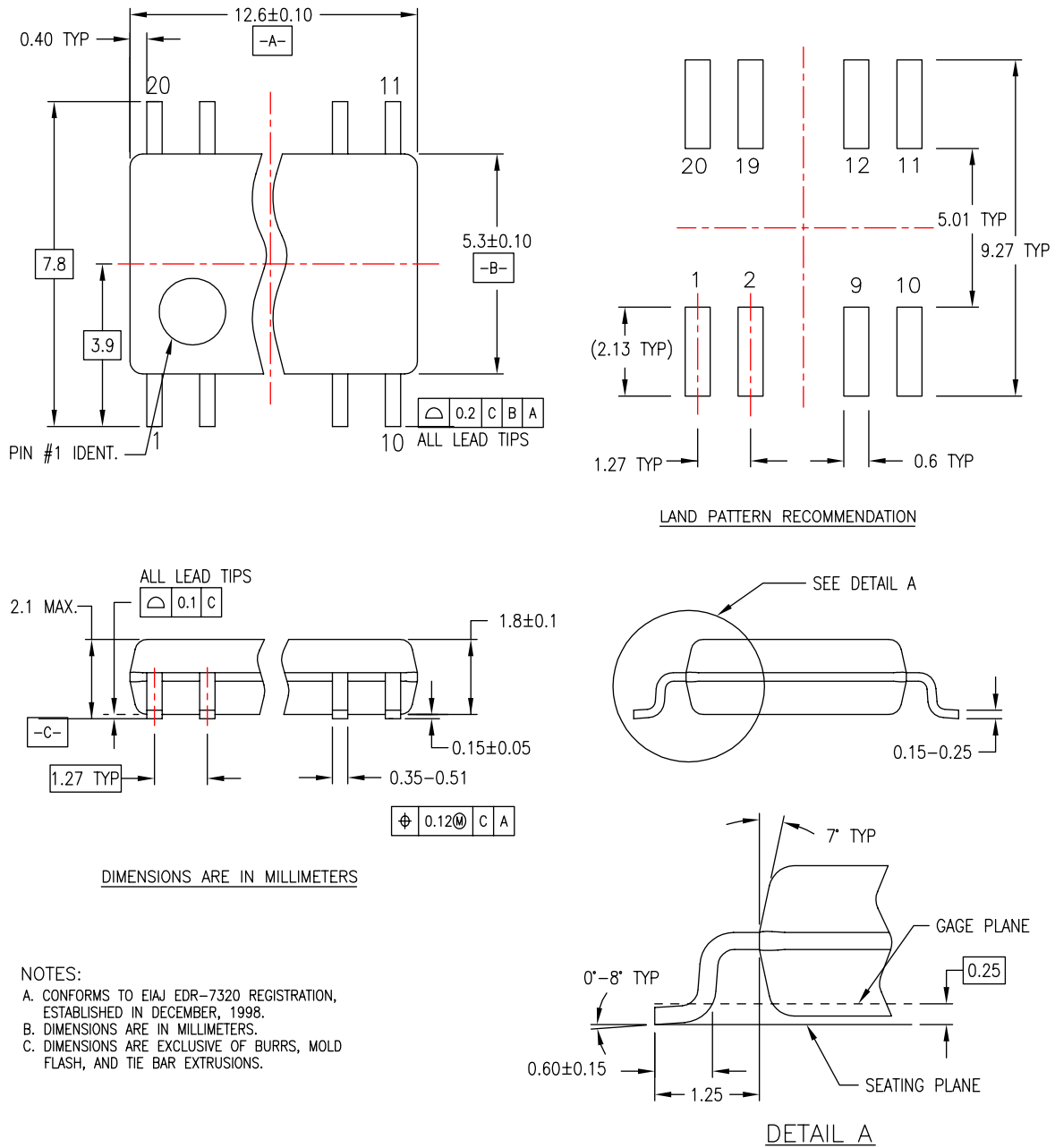
**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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**Physical Dimensions (Continued)**



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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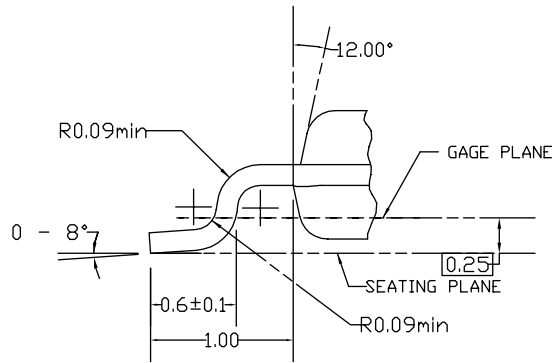
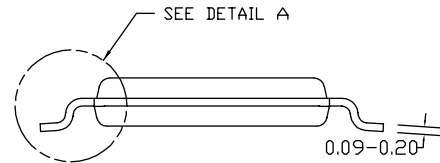
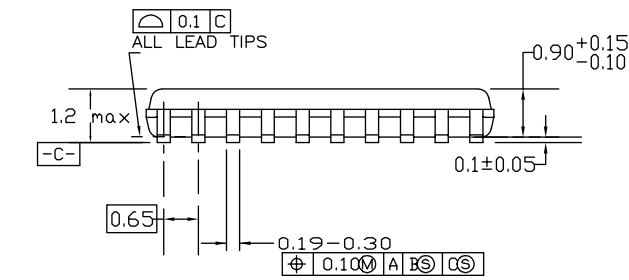
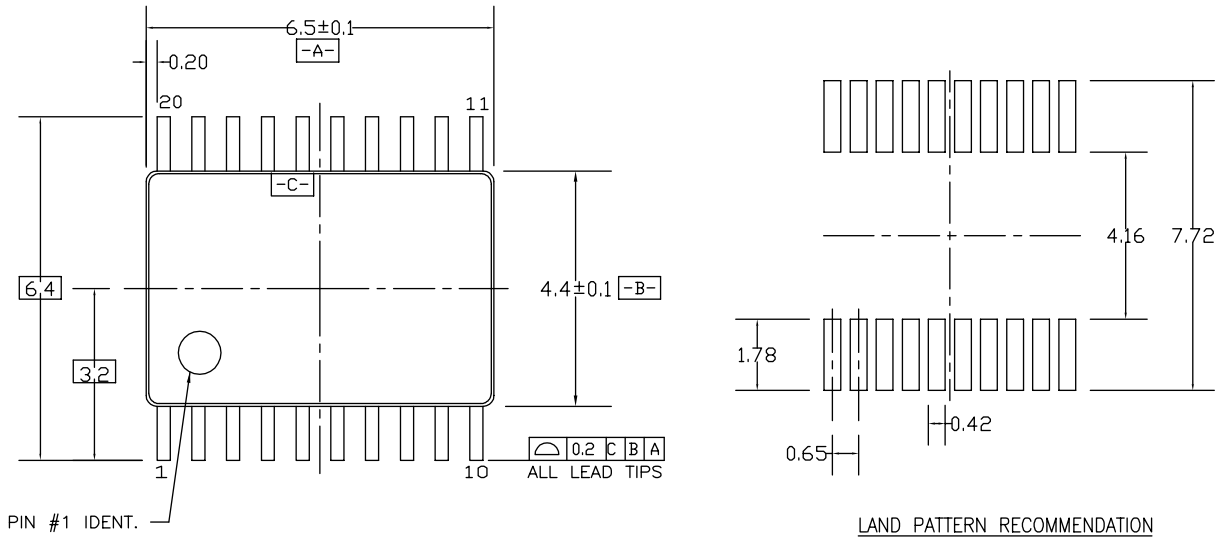
**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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**Physical Dimensions (Continued)**



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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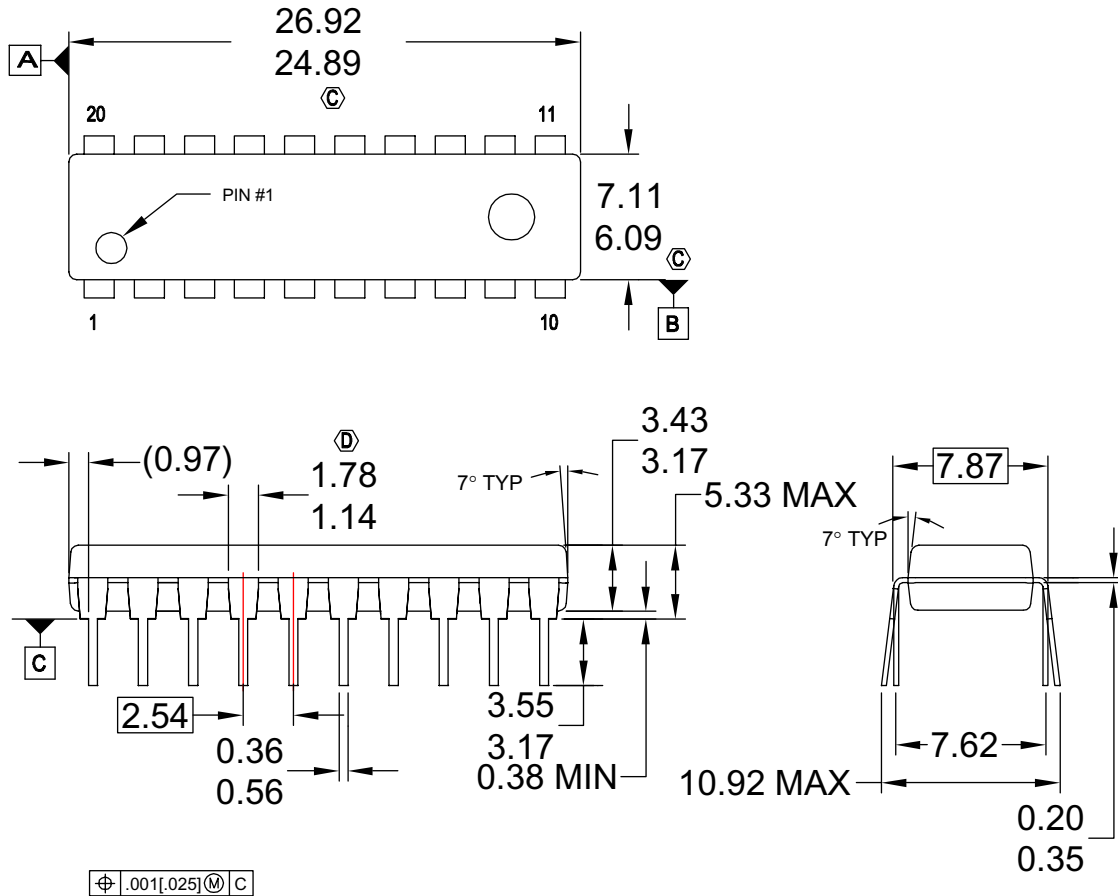
**Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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**Physical Dimensions** (Continued)



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

**Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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CorePLUS <sup>™</sup>	Global Power Resource <sup>SM</sup>	Power247 <sup>®</sup>	GENERAL <sup>®</sup>
CROSSVOLT <sup>™</sup>	Green FPS <sup>™</sup>	POWEREDGE <sup>®</sup>	The Power Franchise <sup>®</sup>
CTL <sup>™</sup>	Green FPS <sup>™</sup> e-Series <sup>™</sup>	Power-SPM <sup>™</sup>	the power <sup>™</sup>
Current Transfer Logic <sup>™</sup>	GTO <sup>™</sup>	PowerTrench <sup>®</sup>	franchise
EcoSPARK <sup>®</sup>	i-Lo <sup>™</sup>	Programmable Active Droop <sup>™</sup>	TinyBoost <sup>™</sup>
EZSWITCH <sup>™</sup> *	IntelliMAX <sup>™</sup>	QFET <sup>®</sup>	TinyBuck <sup>™</sup>
 ™	ISOPLANAR <sup>™</sup>	QS <sup>™</sup>	TinyLogic <sup>®</sup>
 ™	MegaBuck <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TINYOPTO <sup>™</sup>
Fairchild <sup>®</sup>	MICROCOUPLER <sup>™</sup>	Quiet Series <sup>™</sup>	TinyPower <sup>™</sup>
Fairchild Semiconductor <sup>®</sup>	MicroFET <sup>™</sup>	RapidConfigure <sup>™</sup>	TinyPWM <sup>™</sup>
FACT Quiet Series <sup>™</sup>	MicroPak <sup>™</sup>	SMART START <sup>™</sup>	TinyWire <sup>™</sup>
FACT <sup>®</sup>	MillerDrive <sup>™</sup>	SPM <sup>®</sup>	μSerDes <sup>™</sup>
FAST <sup>®</sup>	Motion-SPM <sup>™</sup>	STEALTH <sup>™</sup>	UHC <sup>®</sup>
FastvCore <sup>™</sup> *	OPTOLOGIC <sup>®</sup>	SuperFET <sup>™</sup>	Ultra FRFET <sup>™</sup>
FlashWriter <sup>®</sup> *	OPTOPLANAR <sup>®</sup>	SuperSOT <sup>™</sup> -3	UniFET <sup>™</sup>
		SuperSOT <sup>™</sup> -6	VCX <sup>™</sup>
		SuperSOT <sup>™</sup> -8	

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FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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