



**Pin Definition:**

1. Source 1	8. Drain 1
2. Gate 1	7. Drain 1
3. Source 2	6. Drain 2
4. Gate 2	5. Drain 2

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
30	19 @ $V_{GS} = 10V$	8.5
	28 @ $V_{GS} = 4.5V$	6

### Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

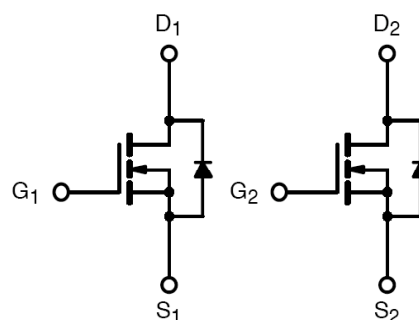
### Application

- Load Switch
- PWM Application

### Ordering Information

Part No.	Package	Packing
TSM4416DCS RL	SOP-8	2.5Kpcs / 13" Reel

### Block Diagram



Dual N-Channel MOSFET

### Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	20	V
Continuous Drain Current	$I_D$	8.5	A
Pulsed Drain Current	$I_{DM}$	40	A
Continuous Source Current (Diode Conduction) <sup>a,b</sup>	$I_S$	2.6	A
Maximum Power Dissipation	$P_D$	Ta = 25°C	2.5
		Ta = 75°C	1.6
Operating Junction Temperature	$T_J$	+150	°C
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C

### Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta_{JF}}$	25	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta_{JA}}$	50	°C/W

Notes:

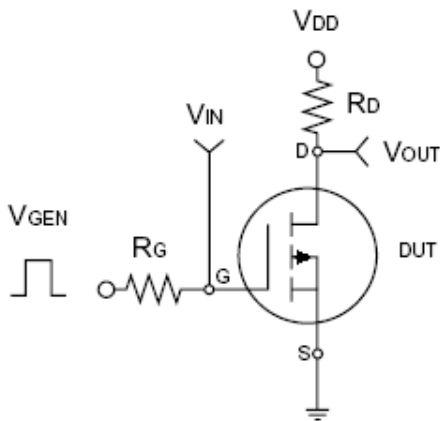
- a. Pulse width limited by the Maximum junction temperature
- b. Surface Mounted on FR4 Board, t ≤ 10 sec.

### Electrical Specifications (Ta = 25°C unless otherwise noted)

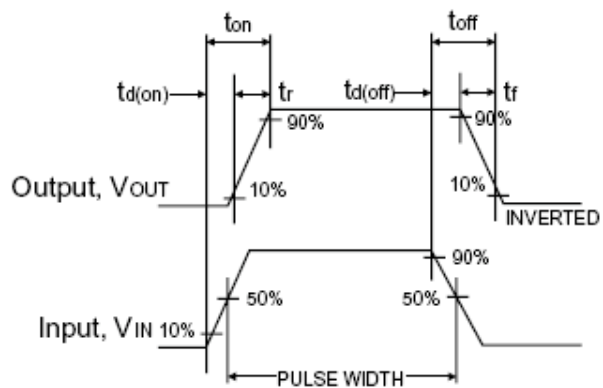
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1	1.8	3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$	$I_{DSS}$	--	--	-1.0	$\mu A$
On-State Drain Current <sup>a</sup>	$V_{DS} \geq 5V, V_{GS} = 10V$	$I_{D(ON)}$	40	--	--	A
Drain-Source On-State Resistance <sup>a</sup>	$V_{GS} = 10V, I_D = 8.5A$	$R_{DS(ON)}$	--	15.5	19	m $\Omega$
	$V_{GS} = 4.5V, I_D = 6A$		--	23	28	
Forward Transconductance <sup>a</sup>	$V_{DS} = 5V, I_D = 8.5A$	$g_{fs}$	--	23	--	S
Diode Forward Voltage	$I_S = 1A, V_{GS} = 0V$	$V_{SD}$	--	0.71	1.0	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$V_{DS} = 15V, I_D = 8.5A, V_{GS} = 5V$	$Q_g$	--	19	24	nC
Gate-Source Charge		$Q_{gs}$	--	9.36	12	
Gate-Drain Charge		$Q_{gd}$	--	4.2	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz$	$C_{iss}$	--	1040	--	pF
Output Capacitance		$C_{oss}$	--	180	--	
Reverse Transfer Capacitance		$C_{rss}$	--	110	--	
<b>Switching<sup>c</sup></b>						
Turn-On Delay Time	$V_{DD} = 15V, R_L = 1.8\Omega, I_D = 1A, V_{GEN} = 10V, R_G = 3\Omega$	$t_{d(on)}$	--	5.2	--	nS
Turn-On Rise Time		$t_r$	--	4.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17.3	--	
Turn-Off Fall Time		$t_f$	--	3.3	--	

Notes:

- a. pulse test: PW  $\leq 300\mu S$ , duty cycle  $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

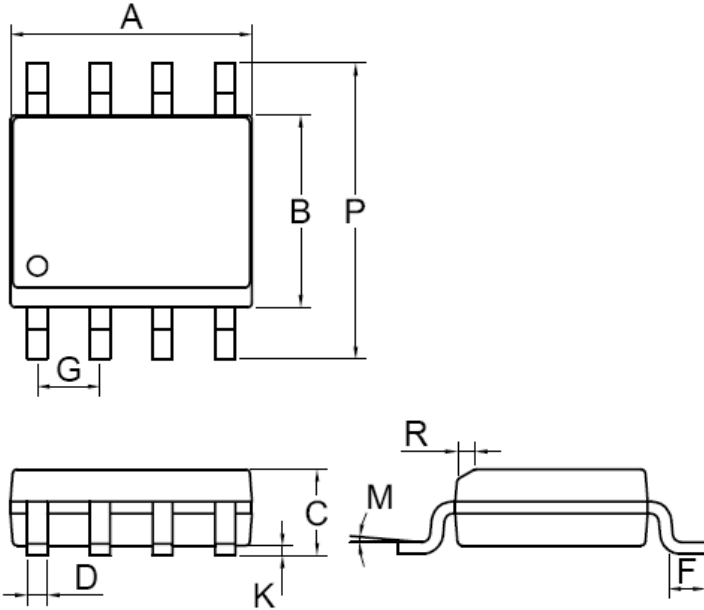


Switching Test Circuit



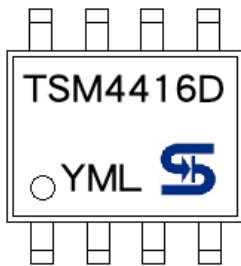
Switchin Waveforms

**SOP-8 Mechanical Drawing**



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**Marking Diagram**



- Y** = Year Code
- M** = Month Code  
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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