TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MBL3244AFK

#### Octal Bus Switch

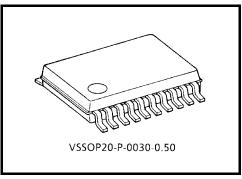
The TC7MBL3244AFK provides eight bits of low-voltage, high-speed bus switching in a standard '244 device pinout. The low ON-resistance of the switch allows connections to be made with minimal propagation delay and while maintaining CMOS low power dissipation.

The device comprises two 4-bit low-impedance switches with separate output-enable ( $\overline{\text{OE}}$ ) inputs. When  $\overline{\text{OE}}$  is low, the switch is on and data can flow from port A to port B, or vice versa. When  $\overline{\text{OE}}$  is high, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits to guard against static discharge.

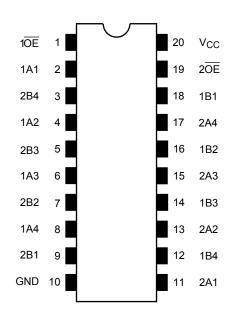


- Operating voltage:  $V_{CC} = 2.0 \sim 3.6 \text{ V}$
- High speed:  $t_{pd} = 0.31 \text{ ns (max)} @ V_{CC} = 3.0 \text{ V}$
- Low ON-resistance:  $R_{ON} = 5 \Omega$  (typ.) @  $V_{CC} = 3.0 \text{ V}$
- ESD performance: Machine model  $\geq \pm 200~V$ Human body model  $\geq \pm 2000~V$
- Power-down protection for inputs (OE input only)
- Package: VSSOP (US20)
- Pin compatible with the 74xx244 type



Weight: 0.03 g (typ.)

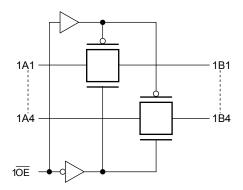
# Pin Assignment (top view)

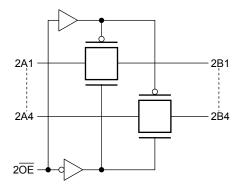


#### **Truth Table**

Inputs	Function	
ŌĒ	runction	
L	A port = B port	
Н	Disconnect	

## System Diagram





## **Absolute Maximum Ratings (Note)**

Charac	cteristic	Symbol	Rating	Unit	
Power supply range		V <sub>CC</sub>	-0.5~4.6	V	
Control pin input ve	oltage	V <sub>IN</sub> -0.5~4.6		V	
Switch terminal I/O voltage		VS	-0.5~Vcc+0.5	V	
Clump diode	Control input pin	lık	-50	mA	
current	Switch terminal	ΊΚ	±50		
Switch I/O current		IS	128	mA	
Power dissipation		PD	180	mW	
DC V <sub>CC</sub> /GND current		I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperatu	re	T <sub>stg</sub>	-65~150	°C	

Note: Exceeding any of the absolute maximum ratings, even briefly, may lead to deterioration in IC performance or even destruction

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

# **Operating Ranges (Note)**

Characteristic	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	2.0~3.6	V
Control pin input voltage	V <sub>IN</sub>	0~3.6	V
Switch I/O voltage	Vs	0~Vcc	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{\text{CC}}$  or GND.

## **Electrical Characteristics**

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## DC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteristic	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Тур.	Max	Unit
High-level control input voltage	V <sub>IH</sub>	_	2.0 to 3.6	0.7 × V <sub>CC</sub>	_		V
Low-level control input voltage	V <sub>IL</sub>	_	2.0 to 3.6	_	_	$^{0.3\times}_{\text{VCC}}$	V
Control input current	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V	2.0 to 3.6	_	_	±1.0	μΑ
Power off leakage current	loff	OE = 0 to 3.6 V	0	_	_	±1.0	μΑ
Off-stage leakage current (switch off)	I <sub>SZ</sub>	A, B = 0 to $V_{CC}$ , $\overline{OE} = V_{CC}$	2.0 to 3.6	_	_	±1.0	μΑ
		$V_{IS} = 0 \text{ V}, I_{IS} = 30 \text{ mA}$ (Note 1)	3.0	_	2	7	
		$V_{IS} = 3.0 \text{ V}, I_{IS} = 30 \text{ mA}$ (Note 1)	3.0	_	3	9	
Switch ON-resistance (Note 2)	R <sub>ON</sub>	$V_{IS} = 2.4 \text{ V}, I_{IS} = 15 \text{ mA}$ (Note 1)	3.0	_	5	20	Ω
,		$V_{IS} = 0 \text{ V}, I_{IS} = 24 \text{ mA}$ (Note 1)	2.3	_	3	10	
		$V_{IS} = 2.3 \text{ V}, I_{IS} = 24 \text{ mA}$ (Note 1)	2.3	_	4	15	
Quiescent supply current	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	3.6	_	_	10	μΑ

Note 1: All typical values are at  $Ta = 25^{\circ}C$ .

Note 2: Measured by voltage drop between A and B pins at indicated current through the switch. ON-resistance is determined by the lower of the voltages on the two pins (A or B).

## AC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteristic	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay (bus to bus)	t <sub>pLH</sub>	Figure 1, Figure 2 (Note)	$3.3 \pm 0.3$	_	0.31	ns
Tropagation delay (bus to bus)	t <sub>pHL</sub>	(Note)	$2.5 \pm 0.2$		0.52	2
Output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	$3.3 \pm 0.3$		6	ns
Output enable time	t <sub>pZH</sub>	rigure 1, rigure 3	$2.5 \pm 0.2$		7.5	20
Output disable time	$t_{pLZ}$	tpLZ Figure 1, Figure 3	$3.3 \pm 0.3$		6	ne
Output disable time tpLZ tpHZ		i igure 1, i igure 3	$2.5 \pm 0.2$	_	7.5	ns

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON-resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage from the source (zero output impedance).

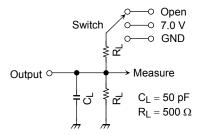
## Capacitance (Ta = 25°C)

Characteristic	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Control input capacitance	C <sub>IN</sub>	(Note)	3.0	3	pF
Switch terminal capacitance	C <sub>I/O</sub>	$\overline{OE} = V_{CC}$ (Note)	3.0	17	pF

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Note: This parameter is guaranteed by design.

## **AC Test Circuit**



Parameter	Switch		
t <sub>pLH</sub> , t <sub>pHL</sub>	Open		
$t_{pLZ}, t_{pZL}$	2 × V <sub>CC</sub>		
t <sub>pHZ</sub> , t <sub>pZH</sub>	GND		

Figure 1

## **AC Waveforms**

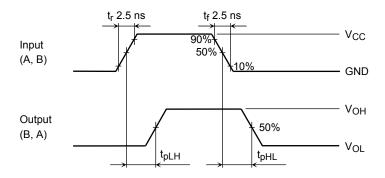


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>

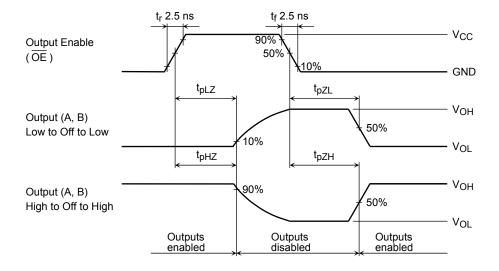
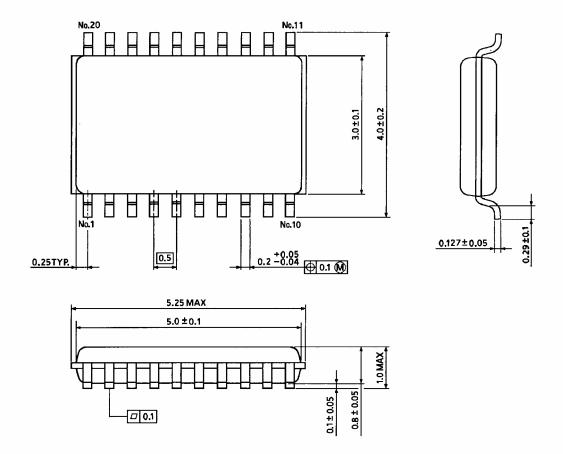


Figure 3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$ 



# **Package Dimensions**



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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