9-IN 3-OUT STEREO AUDIO SELECTOR

■ GENERAL DESCRIPTION

The **NJW1111** is a 9-input 3-output stereo audio selector. It includes three independent 9input-1output stereo audio selectors and adjustable gain buffers.

The **NJW1111** performs superior audio characteristics such as low distortion, low output noise and low crosstalk.

All of internal status and variables are controlled by three-wired serial bus. Selectable two Chip address is available for using two chips on same serial bus line. It is suitable for AV amplifier and receiver system and others.

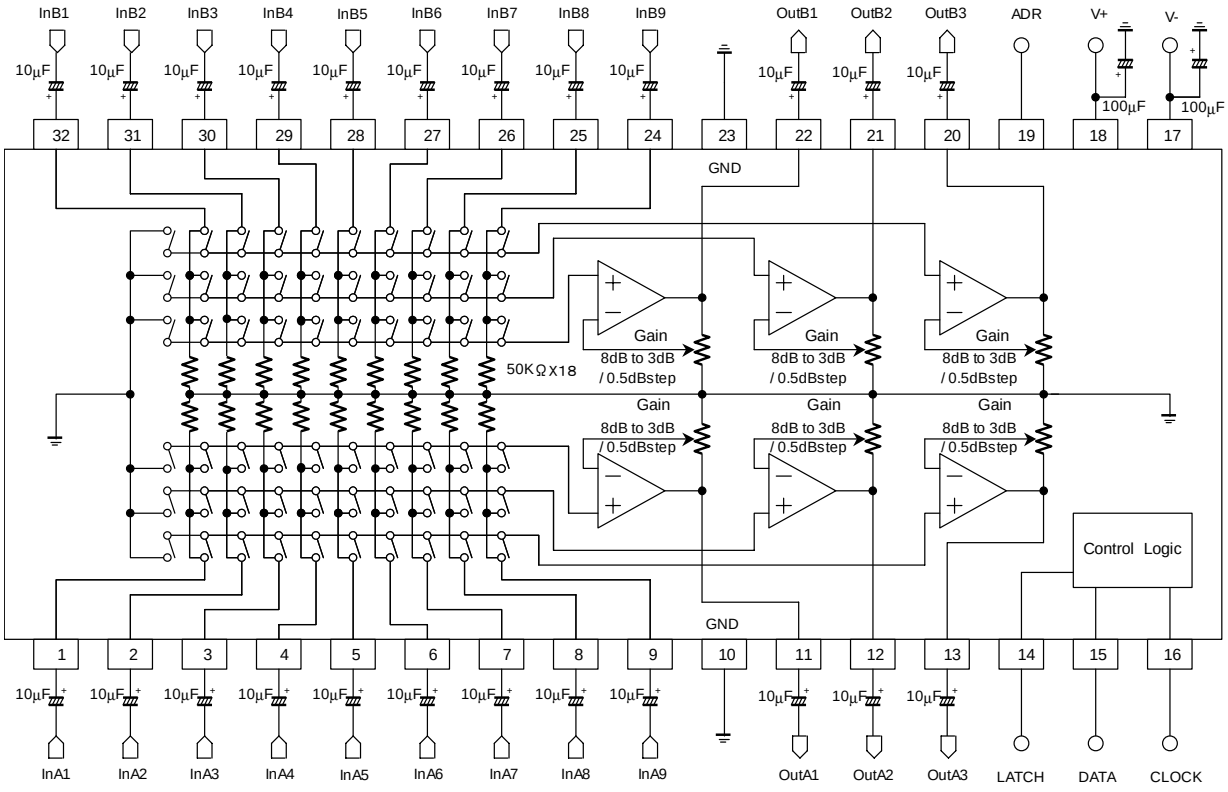
■ PACKAGE OUTLINE

NJW1111V

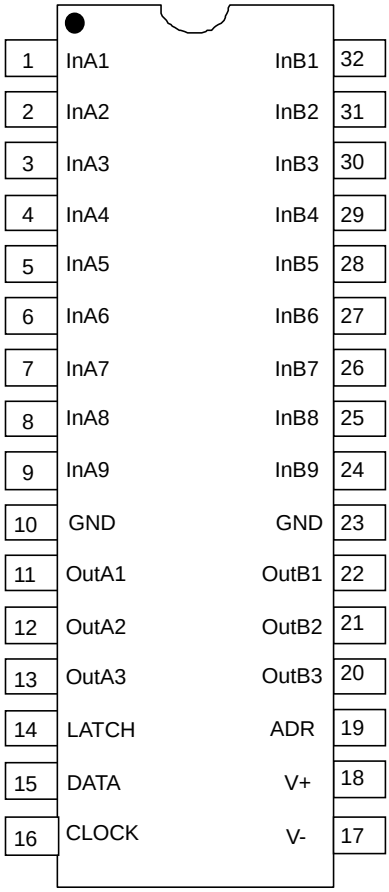
■ FEATURES

• Operating Voltage	±4.5 to ±7.5V
• 9-Input, 3-Output Stereo Audio Selector	
• Operating Current	8mA typ.
• Low Distortion	0.0007% typ.
• Low Output Noise	-116dBV typ.
• Low Crosstalk	110dB typ.
• Channel Separation	110dB typ.
• Variable Gain Buffer	0, 3 to 8dB/0.5dB step
• 3-Wired Serial Control	
• Bi-CMOS Technology	
• Package Outline	SSOP32

■ BLOCK DIAGRAM



■PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	InA1	Ach Input 1	17	V-	V- Power Supply Terminal
2	InA2	Ach Input 2	18	V+	V+ Power Supply Terminal
3	InA3	Ach Input 3	19	ADR	Chip address setting terminal
4	InA4	Ach Input 4	20	OutB3	Bch Output 3
5	InA5	Ach Input 5	21	OutB2	Bch Output 2
6	InA6	Ach Input 6	22	OutB1	Bch Output 1
7	InA7	Ach Input 7	23	GND	Ground Terminal
8	InA8	Ach Input 8	24	InB9	Bch Input 9
9	InA9	Ach Input 9	25	InB8	Bch Input 8
10	GND	Ground Terminal	26	InB7	Bch Input 7
11	OutA1	Ach Output 1	27	InB6	Bch Input 6
12	OutA2	Ach Output 2	28	InB5	Bch Input 5
13	OutA3	Ach Output 3	29	InB4	Bch Input 4
14	LATCH	LATCH	30	InB3	Bch Input 3
15	DATA	DATA	31	InB2	Bch Input 2
16	CLOCK	CLOCK	32	InB1	Bch Input 1

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V^+	+8/-8	V
Maximum Input Voltage	V_{IM}	V^+/V^-	V
Power Dissipation	P_D	800 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+/V^-	-	±4.5	±7.0	±7.5	V

■ ELECTRICAL CHARACTERISTICS

♦Power Supply (Ta=25°C, V^+/V^-=±7V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I_{CC}	V^+, No Signal	4.0	8.0	12.0	MA
Supply Current 2	I_{EE}	V^-No Signal	4.0	8.0	12.0	MA

♦AC CHARACTERISTICS (Ta=25°C, V^+/V^-=±7V, V_{IN}=1Vrms,f=1kHz,R_L=47kΩ)

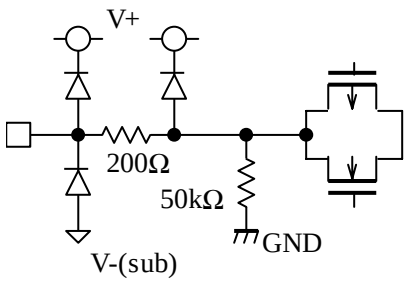
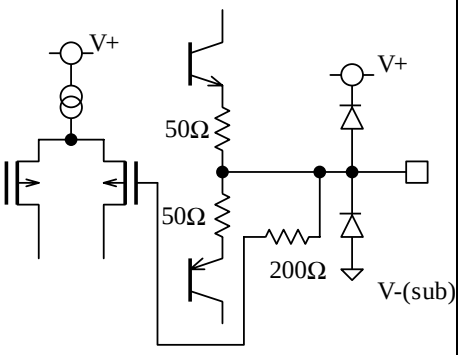
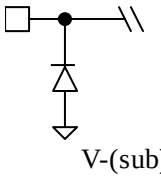
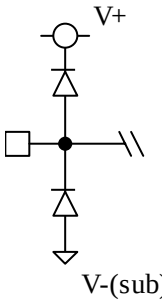
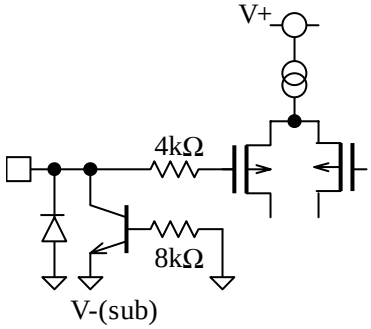
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Output Voltage	V_{OM}	THD=1%	10.6 (3.4)	12.9 (4.4)	-	dBV (Vrms)
Voltage Gain 1	G_{V1}	-	-0.5	0	0.5	dB
Voltage Gain 2	G_{V2}	V_{IN}=200mVrms, Gain=6dB	5.0	6.0	7.0	
Total Harmonic Distortion 1	THD1	BW=400Hz-30kHz	-	0.0007	0.02	%
Total Harmonic Distortion 2	THD2	Vin=2Vrms, BW=400Hz-30kHz	-	0.001	-	
Total Harmonic Distortion 3	THD3	f=10kHz, BW=400Hz-30kHz	-	0.001	-	
Mute Level	A_{TT}	Selector=Mute, A-weighted	-	-110	-	dB
Output Noise	V_{NO}	Rg=0Ω, A-Weighted	-	-116 (1.6)	-106 (5.0)	dBV (μVrms)
Cross Talk 1	CT1	Rg=0Ω, A-Weighted	-	-110	-	dB
Cross Talk 2	CT2	Rg=0Ω, f=20kHz	-	-96	-	
Channel Separation 1	CS1	Rg=0Ω, A-Weighted	-	-110	-90	dB
Channel Separation 2	CS2	Rg=0Ω, f=20kHz	-	-96	-	

BW: Band Width

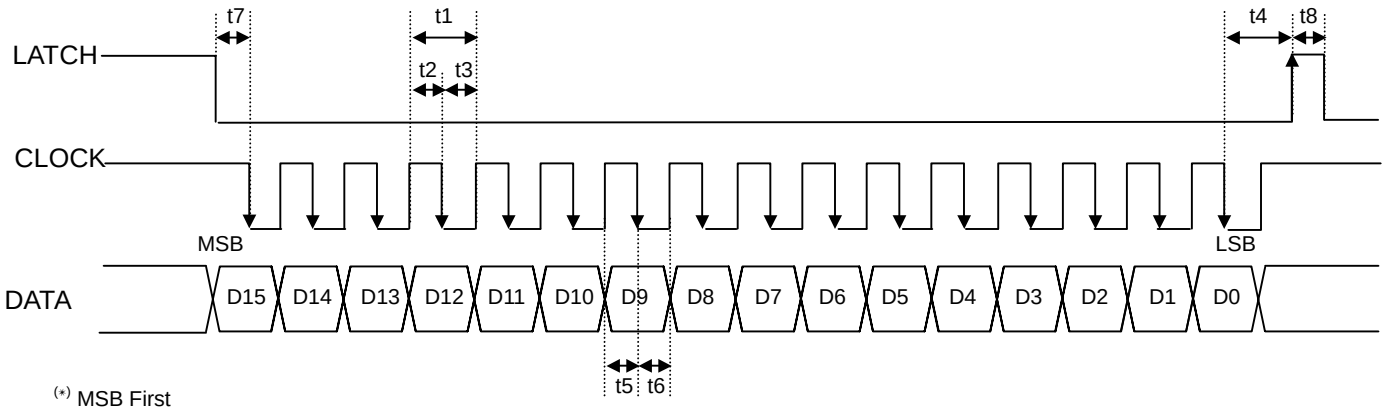
♦Logic Control Characteristics (Ta=25°C, V^+/V^-=±7V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V_{ADRH}	ADR Terminal	2.5	-	V^+	V
Low Level Input Voltage	V_{ADRL}	ADR Terminal	0	-	1.5	

■ **TERMINAL DESCRIPTION**

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
1 to 9 32 to 24	InA1 to 9 InB1 to 9	Ach Input 1 to 9 Bch Input 1 to 9		0V
11 to 13 22 to 20	OutA1 to 3 OutB1 to 3	Ach Output 1 to 3 Bch Output 1 to 3		0V
18	V^+	V+ Power Supply Terminal		V+
10 23	GND	Ground Terminal		0V
14 15 16 19	LATCH DATA CLOCK ADR	LATCH DATA CLOCK Chip address setting terminal		0V

■ **CONTROL DATA FORMAT**



(*) MSB First

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t1	CLOCK Clock Width	4	-	-	µsec
t2	CLOCK Pulse Width (High)	2	-	-	µsec
t3	CLOCK Pulse Width (Low)	2	-	-	µsec
t4	LATCH Rise Hold Time	4	-	-	µsec
t5	DATA Setup Time	1.6	-	-	µsec
t6	DATA Hold Time	1.6	-	-	µsec
t7	CLOCK Setup Time	1.6	-	-	µsec
t8	LATCH High Pulse Width	1.6	-	-	µsec

■ CONTROL DATA

NJW1111 control data is constructed with 16bits.

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Setting DATA								Select Address				Chip Address			

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Gain1				Selector1				0	0	0	0	*	*	*	*
Gain2				Selector2				0	0	0	1	*	*	*	*
Gain3				Selector3				0	0	1	0	*	*	*	*

* Chip address is set by chip address select terminal (ADR) status.

Chip address select terminal	Chip Address			
	D3	D2	D1	D0
Low	1	0	1	0
High	1	0	1	1

■INITIAL CONDITION

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
0	0	0	0	0	0	0	0	0	0	0	1	*	*	*	*
0	0	0	0	0	0	0	0	0	0	1	0	*	*	*	*

* Chip address is set by chip address select terminal (ADR) status.

■ CONTROL DATA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Gain1				Selector1				0	0	0	0	*	*	*	*
Gain2				Selector2				0	0	0	1	*	*	*	*
Gain3				Selector3				0	0	1	0	*	*	*	*

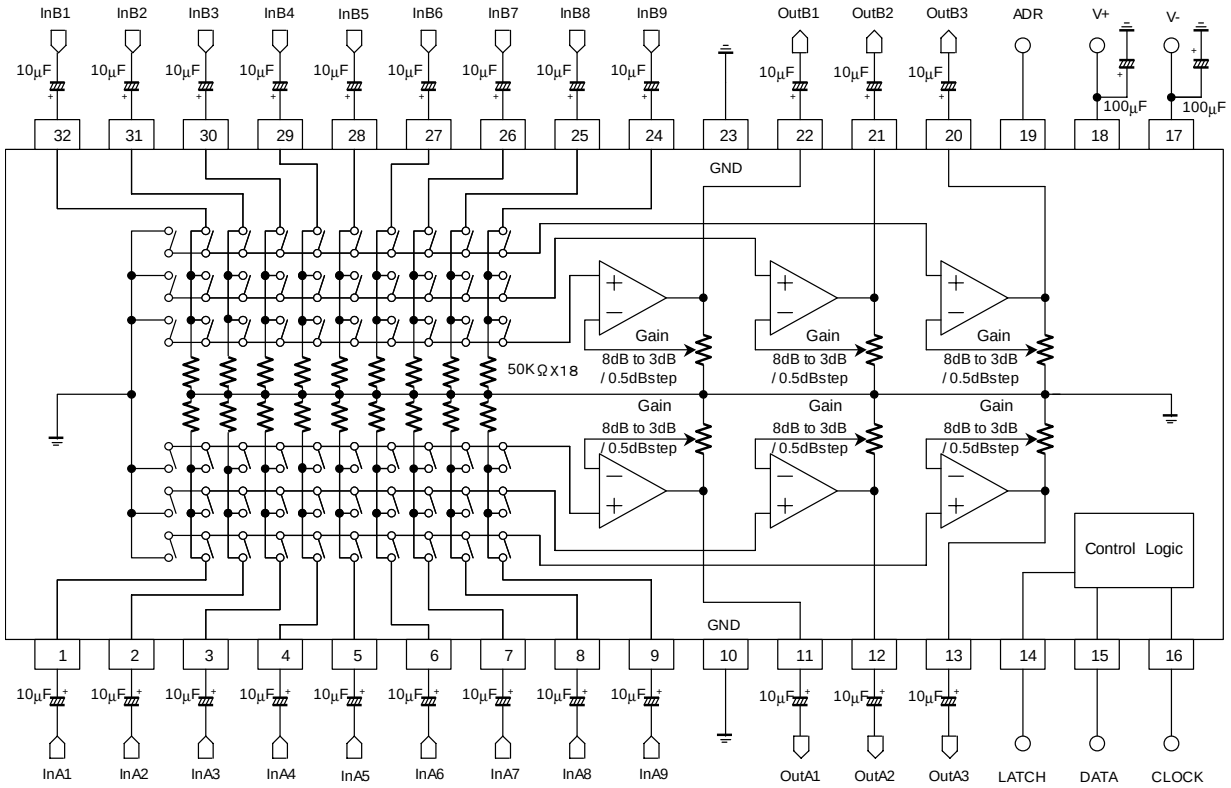
a)Gain

DATA				Setting
D15	D14	D13	D2	
0	0	0	0	0dB
0	0	0	1	+3.0 dB
0	0	1	0	+3.5 dB
0	0	1	1	+4.0 dB
0	1	0	0	+4.5 dB
0	1	0	1	+5.0 dB
0	1	1	0	+5.5 dB
0	1	1	1	+6.0 dB
1	0	0	0	+6.5 dB
1	0	0	1	+7.0 dB
1	0	1	0	+7.5 dB
1	0	1	1	+8.0 dB

b)Input Selector

DATA				Setting
D11	D10	D9	D8	
0	0	0	0	Mute(*)
0	0	0	1	InA1/B1
0	0	1	0	InA2/B2
0	0	1	1	InA3/B3
0	1	0	0	InA4/B4
0	1	0	1	InA5/B5
0	1	1	0	InA6/B6
0	1	1	1	InA7/B7
1	0	0	0	InA8/B8
1	0	0	1	InA9/B9

■ APPLICATION CIRCUIT



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