FAIRCHILD
SEMICONDUCTOR®

April 2007

FXLH1T45
Low Voltage 1-Bit Bi-directional Level Translator with Configurable Voltage Supplies and Bushold Data Inputs

Features

- Bi-directional interface between any 2 levels from 1.1V to 3.6V
- Fully configurable: Inputs track V_{CC} level
- Non-preferential power-up sequencing; either V_{CC} may be powered-up first
- Outputs remain in 3-STATE until active V_{CC} level is reached
- Outputs switch to 3-STATE if either V_{CC} is at GND
- Power off protection
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- Control input (T/$\overline{R}$) levels are referenced to V_{CCA} voltage
- Packaged in the MicroPak 6 (1.0mm x 1.45mm)
- ESD protections exceeds:
  - 4kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM ESD (per ESD STM 5.3)
  - 200V MM ESD (per JESD22-A115 & ESD STM5.2)

General Description

The FXLH1T45 is a single bit configurable dual-voltage supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in 3-STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-STATE if either V_{CC} is removed.

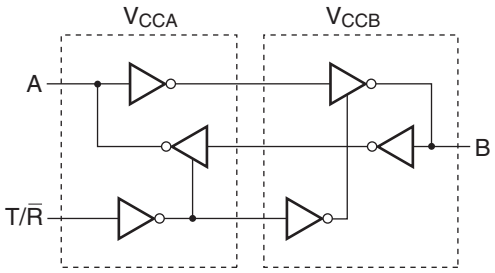
The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the device. The FXLH1T45 is designed so that the control pin (T/$\overline{R}$) is supplied by V_{CCA}.

Ordering Information

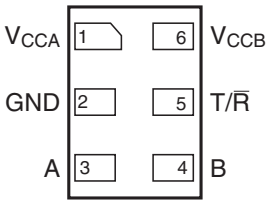
Order Number	Package Number	Pb-Free	Package Description	Supplied As
FXLH1T45L6X	MAC06A	Yes	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Functional Diagram



Connection Diagram



(Top Through View)

Pin Assignment

Pin Number	Terminal Name
1	V_{CCA}
2	GND
3	A
4	B
5	$\overline{T/R}$
6	V_{CCB}

Pin Descriptions

Pin Names	Description
$\overline{T/R}$	Transmit/Receive Input
A	Side A Input or Output
B	Side B Input or Output
V_{CCA}	Side A Power Supply
V_{CCB}	Side B Power Supply

Function Table

Inputs ($\overline{T/R}$)	Outputs
L	Bus B Data to Bus A
H	Bus A Data to Bus B

H = HIGH Logic Level
L = LOW Logic Level

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0V, outputs are in a HIGH-Impedance state. To ensure that bus contention, excessive currents, or oscillations do not occur, a proper power-up sequence is recommended.

The recommended power-up sequence is the following:

1. Apply power to either V_{CC}.
2. Apply power to the $\overline{T/R}$ input (Logic HIGH for A-to-B operation; Logic LOW for B-to-A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1.
3. Apply power to other V_{CC}.

The recommended power-down sequence is the following:

1. Remove power from either V_{CC}.
2. Remove power from other V_{CC}.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	–0.5V to +4.6V
	I/O Port B	–0.5V to +4.6V
	Control Input (T/$\overline{R}$)	–0.5V to +4.6V
V_O	Output Voltage(1)	
	Outputs 3-STATE	–0.5V to +4.6V
	Outputs Active (A_n)	–0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n)	–0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current @ V_I < 0V	–50mA
I_{OK}	DC Output Diode Current @	
	V_O < 0V	–50mA
	V_O > V_{CC}	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	–50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
	Input Voltage	
	Port A	0.0V to 3.6V
	Port B	0.0V to 3.6V
	Control Input (T/$\overline{R}$)	0.0V to V_{CCA}
	Output Current in I_{OH}/I_{OL} with V_{CC} @	
	3.0V to 3.6V	±24mA
	2.3V to 2.7V	±18mA
	1.65V to 1.95V	±6mA
	1.4V to 1.65V	±2mA
	1.1V to 1.4V	±0.5mA
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta t/\Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Notes:

1. I_O Absolute Maximum Rating must be observed.
2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0	–	–	V
			2.3–2.7		1.6	–	–	
			1.65–2.3		0.65 x V_{CCI}	–	–	
			1.4–1.65		0.65 x V_{CCI}	–	–	
			1.1–1.4		0.9 x V_{CCI}	–	–	
		Control Pin T/$\overline{R}$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	2.0	–	–	
			2.3–2.7		1.6	–	–	
			1.65–2.3		0.65 x V_{CCA}	–	–	
			1.4–1.65		0.65 x V_{CCA}	–	–	
			1.1–1.4		0.9 x V_{CCA}	–	–	
V_{IL}	Low Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	–	–	0.8	V
			2.3–2.7		–	–	0.7	
			1.65–2.3		–	–	0.35 x V_{CCI}	
			1.4–1.65		–	–	0.35 x V_{CCI}	
			1.1–1.4		–	–	0.1 x V_{CCI}	
		Control Pin T/$\overline{R}$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	–	–	0.8	
			2.3–2.7		–	–	0.7	
			1.65–2.3		–	–	0.35 x V_{CCA}	
			1.4–1.65		–	–	0.35 x V_{CCA}	
			1.1–1.4		–	–	0.1 x V_{CCA}	
V_{OH}	High Level Output Voltage[4]	I_{OH} = –100µA	1.1–3.6	1.1–3.6	V_{CC0}–0.2	–	–	V
		I_{OH} = –12mA	2.7	2.7	2.2	–	–	
		I_{OH} = –18mA	3.0	3.0	2.4	–	–	
		I_{OH} = –24mA	3.0	3.0	2.2	–	–	
		I_{OH} = –6mA	2.3	2.3	2.0	–	–	
		I_{OH} = –12mA	2.3	2.3	1.8	–	–	
		I_{OH} = –18mA	2.3	2.3	1.7	–	–	
		I_{OH} = –6mA	1.65	1.65	1.25	–	–	
		I_{OH} = –2mA	1.4	1.4	1.05	–	–	
		I_{OH} = –0.5mA	1.1	1.1	0.75 x V_{CC0}	–	–	
V_{OL}	Low Level Output Voltage[4]	I_{OL} = 100µA	1.1–3.6	1.1–3.6	–	–	0.2	V
		I_{OL} = 12mA	2.7	2.7	–	–	0.4	
		I_{OL} = 18mA	3.0	3.0	–	–	0.4	
		I_{OL} = 24mA	3.0	3.0	–	–	0.55	
		I_{OL} =12mA	2.3	2.3	–	–	0.4	
		I_{OL} = 18mA	2.3	2.3	–	–	0.6	
		I_{OL} = 6mA	1.65	1.65	–	–	0.3	
		I_{OL} = 2mA	1.4	1.4	–	–	0.35	
		I_{OL} = 0.5mA	1.1	1.1	–	–	0.3 x V_{CC0}	
I_I	Input Leakage Current Control Pins	V_I = V_{CCA} or GND	1.1–3.6	3.6	–	–	±1.0	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Typ.	Max.	Units
$I_{I(HOLD)}$	Bushold Input Minimum Drive Current	V_{IN} = 0.8	3.0	3.0	75.0	–	–	µA
		V_{IN} = 2.0	3.0	3.0	-75.0	–	–	
		V_{IN} = 0.7	2.3	2.3	45.0	–	–	
		V_{IN} = 1.6	2.3	2.3	-45.0	–	–	
		V_{IN} = 0.57	1.65	1.65	25.0	–	–	
		V_{IN} = 1.07	1.65	1.65	-25.0	–	–	
		V_{IN} = 0.49	1.4	1.4	11.0	–	–	
		V_{IN} = 0.91	1.4	1.4	-11.0	–	–	
		V_{IN} = 0.11	1.1	1.1	–	4.0	–	
		V_{IN} = 0.99	1.1	1.1	–	-4.0	–	
$I_{I(OD)}$	Bushold Input Over-Drive Current-to-Change State	(5)	3.6	3.6	450	–	–	µA
		(6)	3.6	3.6	-450	–	–	
		(5)	2.7	2.7	300	–	–	
		(6)	2.7	2.7	-300	–	–	
		(5)	1.95	1.95	200	–	–	
		(6)	1.95	1.95	-200	–	–	
		(5)	1.6	1.6	120	–	–	
		(6)	1.6	1.6	-120	–	–	
		(5)	1.4	1.4	80.0	–	–	
		(6)	1.4	1.4	-80.0	–	–	
I_{OFF}	Power Off Leakage Current	A_n, V_{CCA} = V_{CCI}, V_I = 0V to 3.6V	0	3.6	–	–	±10.0	µA
		B_n, V_{CCB} = V_{CCI}, V_I = 0V to 3.6V	0	3.6	–	–	±10.0	
I_{OZ}	3-STATE Output Leakage	A_n, V_{CCA} = V_{CCO}, V_O = 0V or 3.6V	0	3.6	–	–	±10.0	µA
		B_n, V_{CCB} = V_{CCO}, V_O = 0V or 3.6V	0	3.6	–	–	±10.0	
$I_{CCA/B}$	Quiescent Supply Current(7)	V_I = V_{CCI} or GND; I_O = 0	1.1–3.6	1.1–3.6	–	–	20.0	µA
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0	1.1–3.6	–	–	–10.0	µA
		V_I = V_{CCA} or GND; I_O = 0	1.1–3.6	0	–	–	10.0	µA
I_{CCB}	Quiescent Supply Current	V_I = V_{CCB} or GND; I_O = 0	1.1–3.6	0	–	–	–10.0	µA
		V_I = V_{CCB} or GND; I_O = 0	0	1.1–3.6	–	–	10.0	µA
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0	3.6	3.6	–	–	500	µA

Notes:

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. An external driver must source at least the specified current to switch LOW-to-HIGH.
6. An external driver must source at least the specified current to switch HIGH-to-LOW.
7. Reflects current per supply, V_{CCA} or V_{CCB}.

AC Electrical Characteristics

V_{CCA} = 3.0V to 3.6V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL} (8)	Output Enable $\overline{T}/R$ to B	0.4	7.2	0.5	7.6	0.7	9.1	0.8	10.5	1.6	25.7	ns
	Output Enable $\overline{T}/\overline{R}$ to A	0.4	7.3	0.4	7.8	1.0	8.8	2.0	10.5	2.8	30.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{T}/\overline{R}$ to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable $\overline{T}/\overline{R}$ to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	

V_{CCA} = 2.3V to 2.7V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL} (8)	Output Enable $\overline{T}/R$ to B	0.4	7.8	0.6	8.2	0.7	9.6	1.0	10.9	1.6	26.0	ns
	Output Enable $\overline{T}/\overline{R}$ to A	0.5	8.0	0.6	8.5	1.2	9.3	2.0	11.5	3.0	24.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{T}/\overline{R}$ to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable $\overline{T}/\overline{R}$ to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	

V_{CCA} = 1.65V to 1.95V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL} (8)	Output Enable $\overline{T}/R$ to B	0.8	9.0	1.0	9.5	1.3	10.7	1.4	12.1	2.0	27.0	ns
	Output Enable $\overline{T}/\overline{R}$ to A	0.7	10.5	0.7	10.8	1.6	10.9	2.5	13.0	3.2	25.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{T}/\overline{R}$ to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable $\overline{T}/\overline{R}$ to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	

AC Electrical Characteristics (Continued)

V_{CCA} = 1.4V to 1.6V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL}[8]	Output Enable $\overline{T}/R$ to B	1.5	10.3	1.5	10.8	2.0	12.0	2.0	13.3	2.5	28.0	ns
	Output Enable $\overline{T}/R$ to A	1.0	12.9	1.2	13.1	1.8	13.3	2.5	14.8	3.3	27.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{T}/R$ to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable $\overline{T}/R$ to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	

V_{CCA} = 1.1V to 1.3V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL}[8]	Output Enable $\overline{T}/R$ to B	2.8	28.0	3.0	19.0	3.2	20.0	3.3	21.5	4.0	36.0	ns
	Output Enable $\overline{T}/R$ to A	2.4	37.0	2.1	29.0	2.5	30.0	3.5	32.0	4.0	44.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{T}/R$ to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable $\overline{T}/R$ to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

Note:

8. The enable time, t_{PZH} or t_{PZL}, is the time for the FXLH1T45 to return to active operation after a direction change. The enable time specifies the worst-case delay from the time the $T/\overline{R}$ pin is switched until a valid output signal is expected. For example, to change direction to B-to-A operation, the $T/\overline{R}$ pin is switched from HIGH-to-LOW. The enable time for this case is found by adding the disable time for $T/\overline{R}$ to B to the propagation delay for B to A. The formulas for calculating enable times are the following:

   t_{PZH} ($T/\overline{R}$ to A) = t_{PLZ} ($T/\overline{R}$ to B) + t_{PLH} (B to A)

   t_{PZL} ($T/\overline{R}$ to A) = t_{PHZ} ($T/\overline{R}$ to B) + t_{PHL} (B to A)

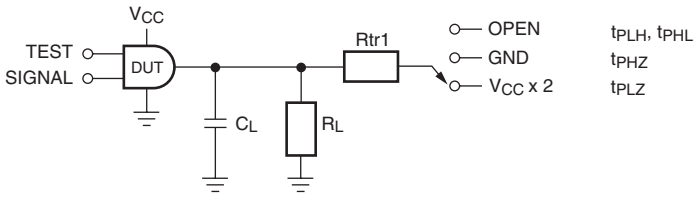
   t_{PZH} ($T/\overline{R}$ to B) = t_{PLZ} ($T/\overline{R}$ to A) + t_{PLH} (A to B)

   t_{PZL} ($T/\overline{R}$ to B) = t_{PHZ} ($T/\overline{R}$ to A) + t_{PHL} (A to B)

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
			Typical	
C_{IN}	Input Capacitance Control Pin ($T/\overline{R}$)	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	4.0	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10MHz	20.0	pF

AC Loading and Waveforms

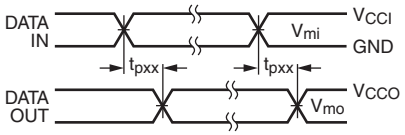


Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}	V_{CCO} x 2 at V_{CCO} = 3.3 ± 0.3V, 2.5V ± 0.2V, 1.8V ± 0.15V, 1.5V ± 0.1V, 1.2V ± 0.1V
t_{PHZ}	GND

Figure 1. AC Test Circuit

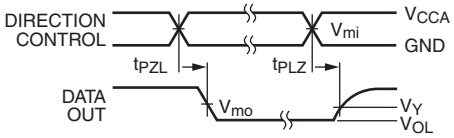
AC Load Table

V_{CCO}	C_L	R_L	Rtr1
1.2V ± 0.1V	15pF	2kΩ	2kΩ
1.5V ± 0.1V	15pF	2kΩ	2kΩ
1.8V ± 0.15V	15pF	2kΩ	2kΩ
2.5V ± 0.2V	15pF	2kΩ	2kΩ
3.3V ± 0.3V	15pF	2kΩ	2kΩ



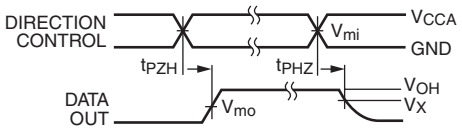
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 2. Waveform for Inverting and Non-Inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}				
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.1V	1.2V ± 0.1V
V_{mi}	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$
V_{mo}	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$
V_X	$V_{OH}-0.3V$	$V_{OH}-0.15V$	$V_{OH}-0.15V$	$V_{OH}-0.1V$	$V_{OH}-0.1V$
V_Y	$V_{OL}+0.3V$	$V_{OL}+0.15V$	$V_{OL}+0.15V$	$V_{OL}+0.1V$	$V_{OL}+0.1V$

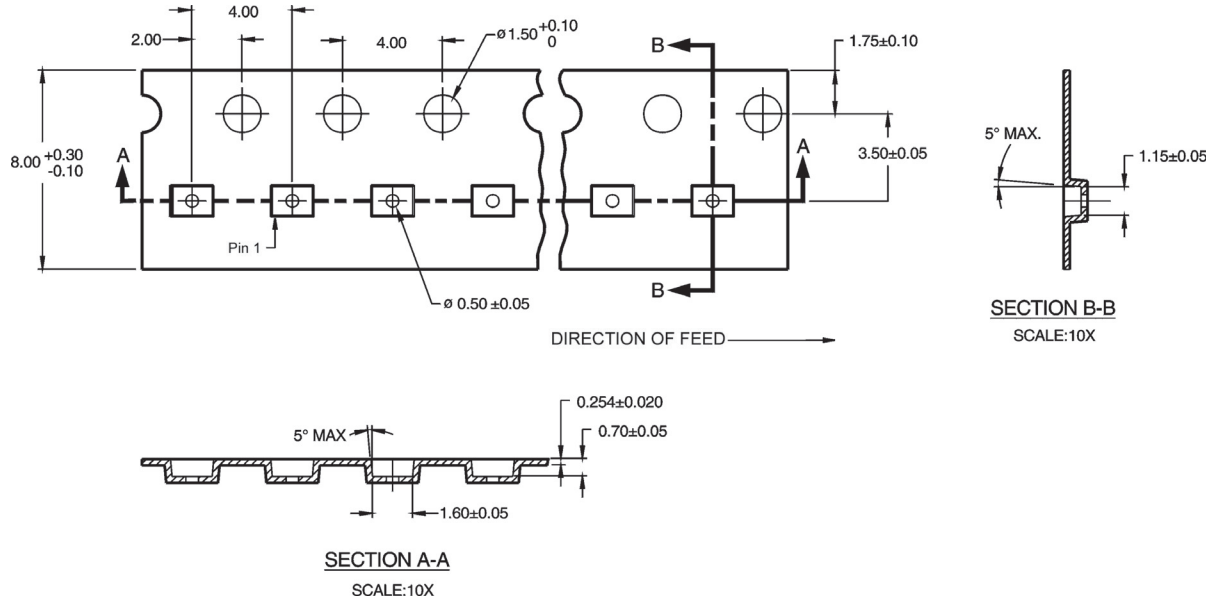
For V_{mi}: $V_{CCI} = V_{CCA}$ for Control Pin T/$\overline{R}$ or $V_{CCA}/2$

Tape and Reel Specification

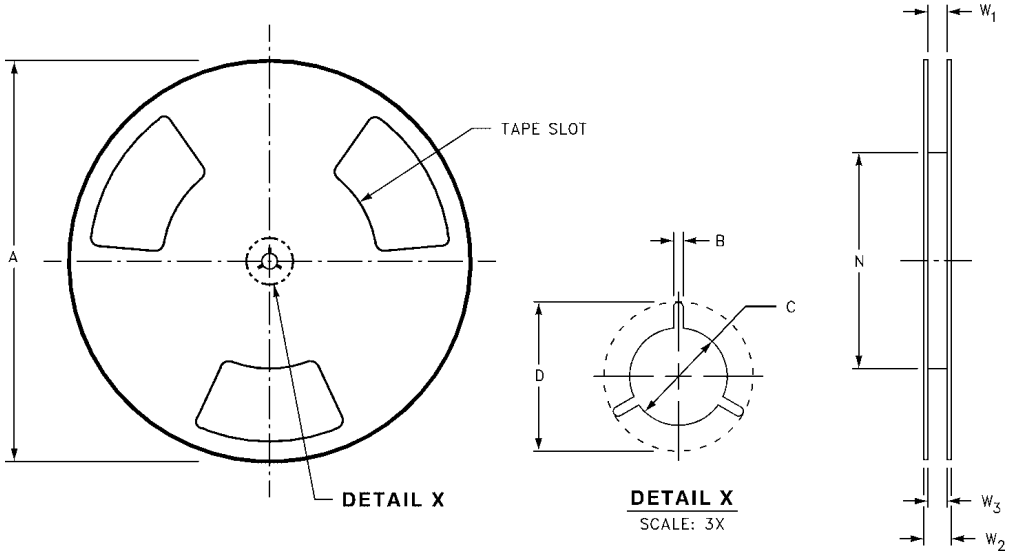
Tape Format for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions millimeters

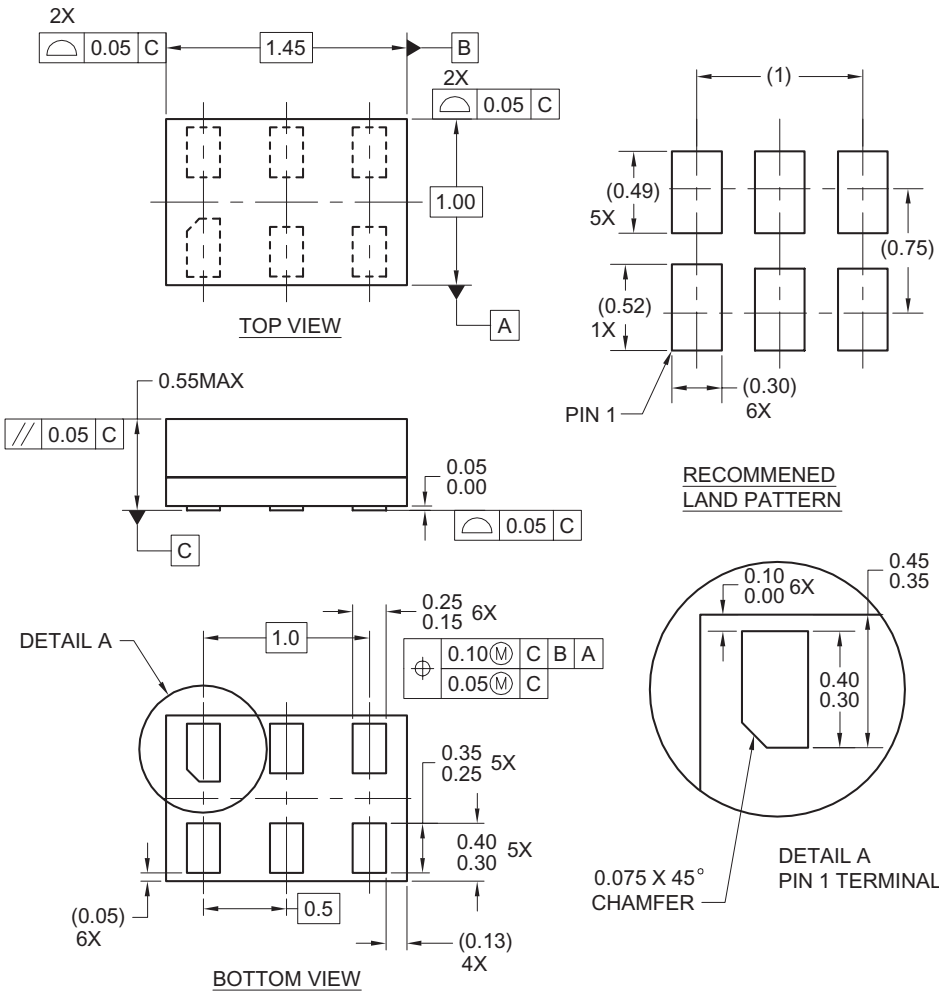


Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/-0.000 (8.40 +1.50/-0.00)	0.567 (14.40)	W1 +0.078/-0.039 (W1 +2.00/-1.00)

Physical Dimensions millimeters unless otherwise noted



Notes:

1. Conforms to JEDEC standard M0-252 variation UAAD.
2. Dimensions are in millimeters.
3. Drawing conforms to ASME Y14.5M-1994.

MAC06AREVC

6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Across the board. Around the world.™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
CTL™
Current Transfer Logic™
DOME™
E²CMOS™
EcoSPARK®
EnSigna™
FACT Quiet Series™
FACT®
FAST®
FASTr™
FPS™
FRFET®
GlobalOptoisolator™
GTO™
HiSeC™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
MICROCOUPLER™
MicroPak™
MICROWIRE™
Motion-SPM™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR®
PACMAN™
PDP-SPM™
POP™
Power220®
Power247®
PowerEdge™
PowerSaver™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
The Power Franchise®
™
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyWire™
TruTranslation™
µSerDes™
UHC®
UniFET™
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I26