CY24272

Rambus® XDR™ Clock Generator with Zero SDA Hold Time

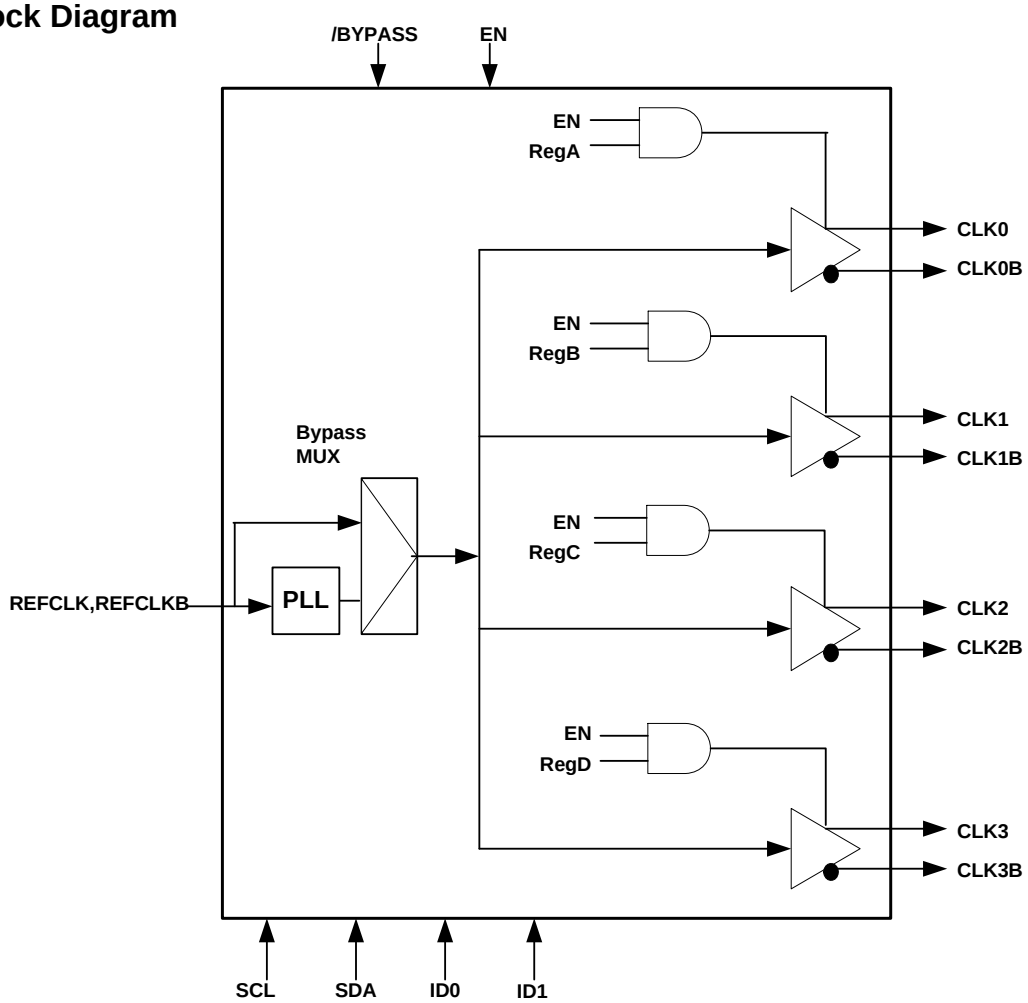
Features

- Meets Rambus® Extended Data Rate (XDR™) clocking requirements
- 25 ps typical cycle-to-cycle jitter
  - –135 dBc/Hz typical phase noise at 20 MHz offset
- 100 or 133 MHz differential clock input
- 300–667 MHz high speed clock support
- Quad (open drain) differential output drivers
- Supports frequency multipliers: 3, 4, 5, 6, 9/2 and 15/4
- Spread Aware™
- 2.5V operation
- 28-pin TSSOP package

Table 1. Device Comparison

CY24271	CY24272
SDA hold time = 300 ns (SMBus compliant)	SDA hold time = 0 ns (I^2C compliant)
R_{RC} = 200Ω typical (Rambus standard drive)	R_{RC} = 295Ω minimum (Reduced output drive)

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 28 Pin TSSOP

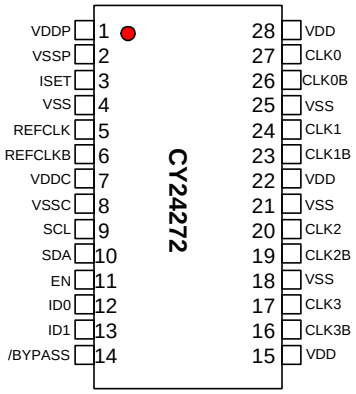


Table 2. Pin Definition - 28 Pin TSSOP

Pin No.	Name	IO	Description
1	VDDP	PWR	2.5V power supply for phased lock loop (PLL)
2	VSSP	GND	Ground
3	ISET	I	Set clock driver current (external resistor)
4	VSS	GND	Ground
5	REFCLK	I	Reference clock input (connect to clock source)
6	REFCLKB	I	Complement of reference clock (connect to clock source)
7	VDDC	PWR	2.5V power supply for core
8	VSSC	GND	Ground
9	SCL	I	SMBus clock (connect to SMBus)
10	SDA	I	SMBus data (connect to SMBus)
11	EN	I	Output Enable (CMOS signal)
12	ID0	I	Device ID (CMOS signal)
13	ID1	I	Device ID (CMOS signal)
14	/BYPASS	I	REFCLK bypassing PLL (CMOS signal)
15	VDD	PWR	Power supply for outputs
16	CLK3B	O	Complement clock output
17	CLK3	O	Clock output
18	VSS	GND	Ground
19	CLK2B	O	Complement clock output
20	CLK2	O	Clock output
21	VSS	GND	Ground
22	VDD	PWR	Power supply for outputs
23	CLK1B	O	Complement clock output
24	CLK1	O	Clock output
25	VSS	GND	Ground
26	CLK0B	O	Complement clock output
27	CLK0	O	Clock output
28	VDD	PWR	Power supply for outputs

PLL Multiplier

Table 3 shows the frequency multipliers in the PLL, selectable by programming the SMBus registers MULT0, MULT1, and MULT2. Default multiplier at power up is 4.

Table 3. PLL Multiplier Selection

Register			Frequency Multiplier	Output Frequency (MHz)	
MULT2	MULT1	MULT0		REFCLK = 100 MHz[1], REFSEL = 0	REFCLK = 133 MHz[1], REFSEL = 1
0	0	0	3	300	400
0	0	1	4	400[2]	–
0	1	0	5	500	667
0	1	1	6	600	–
1	0	0	Reserved	–	–
1	0	1	9/2	450	600
1	1	0	Reserved	–	–
1	1	1	15/4	375	500

Input Clock Signal

The XCG receives either a differential (REFCLK/REFCLKB) or a single-ended reference clocking input (REFCLK).

When the reference input clock is from a different clock source, it must meet the voltage levels and timing requirements listed in DC Operating Conditions on page 7 and AC Operating Conditions on page 8.

For a single-ended clock input, an external voltage divider and a supply voltage, as shown in Figure 2 on page 6, provide a reference voltage V_{TH} at the REFCLKB pin. This determines the proper trip point of REFCLK. For the range of V_{TH} specified in DC Operating Conditions on page 7, the outputs also meet the DC and AC Operating Conditions tables.

Modes of Operation

The modes of operation are determined by the logic signals applied to the EN and /BYPASS pins and the values in the five SMBus Registers: RegTest, RegA, RegB, RegC, and RegD. Table 5 on page 4 shows selection from one to all four of the outputs, the Outputs Disabled Mode (EN = low), and Bypass Mode (EN = high, /BYPASS = low). There is an option reserved for vendor test. Disabled outputs are set to High Z.

At power up, the SMBus registers default to the last entry in Table 6 on page 5. The value at RegTest is 0. The values at RegA, RegB, RegC, and RegD are all ‘1’. Thus, all outputs are controlled by the logic applied to EN and /BYPASS.

Table 4. SMBus Device Addresses for CY24272

XCG		Hex Address	8-bit SMBus Device Address Including Operation							
Device	Operation		Five Most Significant Bits					ID1	ID0	WR# / RD
0	Write	D8	1	1	0	1	1	0	0	0
	Read	D9								1
1	Write	DA						0	1	0
	Read	DB								1
2	Write	DC						1	0	0
	Read	DD								1
3	Write	DE						1	1	0
	Read	DF								1

Notes
1. Output frequencies shown in Table 3 are based on nominal input frequencies of 100 MHz and 133.3 MHz. The PLL multipliers are applicable to spread spectrum modulated input clock with maximum and minimum input cycle time. The REFSEL bit in SMBus 81h is set correctly as shown.
2. Default PLL multiplier at power up.

Table 5. Modes of Operation for CY24272

EN	/BYPASS	RegTest	RegA	RegB	RegC	RegD	CLK0/CLK0B	CLK1/CLK1B	CLK2/CLK2B	CLK3/CLK3B
L	X	X	X	X	X	X	High Z	High Z	High Z	High Z
H	X	1	X	X	X	X	Reserved for Vendor Test			
H	L	0	X	X	X	X	REFCLK/ REFCLKB[3]	REFCLK/ REFCLKB	REFCLK/ REFCLKB	REFCLK/ REFCLKB
H	H	0	0	0	0	0	High Z	High Z	High Z	High Z
H	H	0	0	0	0	1	High Z	High Z	High Z	CLK/CLKB
H	H	0	0	0	1	0	High Z	High Z	CLK/CLKB	High Z
H	H	0	0	0	1	1	High Z	High Z	CLK/CLKB	CLK/CLKB
H	H	0	0	1	0	0	High Z	CLK/CLKB	High Z	High Z
H	H	0	0	1	0	1	High Z	CLK/CLKB	High Z	CLK/CLKB
H	H	0	0	1	1	0	High Z	CLK/CLKB	CLK/CLKB	High Z
H	H	0	0	1	1	1	High Z	CLK/CLKB	CLK/CLKB	CLK/CLKB
H	H	0	1	0	0	0	CLK/CLKB	High Z	High Z	High Z
H	H	0	1	0	0	1	CLK/CLKB	High Z	High Z	CLK/CLKB
H	H	0	1	0	1	0	CLK/CLKB	High Z	CLK/CLKB	High Z
H	H	0	1	0	1	1	CLK/CLKB	High Z	CLK/CLKB	CLK/CLKB
H	H	0	1	1	0	0	CLK/CLKB	CLK/CLKB	High Z	High Z
H	H	0	1	1	0	1	CLK/CLKB	CLK/CLKB	High Z	CLK/CLKB
H	H	0	1	1	1	0	CLK/CLKB	CLK/CLKB	CLK/CLKB	High Z
H	H	0[4]	1[4]	1[4]	1[4]	1[4]	CLK/CLKB	CLK/CLKB	CLK/CLKB	CLK/CLKB

Device ID and SMBus Device Address

The device ID (ID0 and ID1) is a part of the SMBus device 8-bit address. The least significant bit of the address designates a write or read operation. Table 4 on page 3 shows the addresses for four CY24272 devices on the same SMBus.

SMBus Protocol

The CY24272 is a slave receiver supporting operations in the word and byte modes described in sections 5.5.4 and 5.5.5 of the SMBus Specification 2.0.

DC specifications are modified to Rambus standard to support 1.8, 2.5, and 3.3 volt devices. Time out detection and packet error protocol SMBus features are not supported.

Hold time for SDA is reduced relative to the CY24271, so that it is compatible with I^2C.

SMBus Data Byte Definitions

Three data bytes are defined for the CY24272. Byte 0 is for programming the PLL multiplier registers and clock output registers.

The definition of Byte 2 is shown in Table 6, Table 7, and Table 8 on page 5. The upper five bits are the revision numbers of the device and the lower three bits are the ID numbers assigned to the vendor by Rambus.

Notes
3. Bypass Mode: REFCLK bypasses the PLL to the output drivers.
4. Default mode of operation is at power up.

Table 6. Command Code 80h[5]

Bit	Register	POD	Type	Description
7	Reserved	0	RW	Reserved (no internal function)
6	MULT2	0	RW	PLL Multiplier Select (reference Table 3 on page 3)
5	MULT1	0	RW	
4	MULT0	1	RW	
3	RegA	1	RW	Clock 0 Output Select
2	RegB	1	RW	Clock 1 Output Select
1	RegC	1	RW	Clock 2 Output Select
0	RegD	1	RW	Clock 3 Output Select

Table 7. Command Code 81h[5]

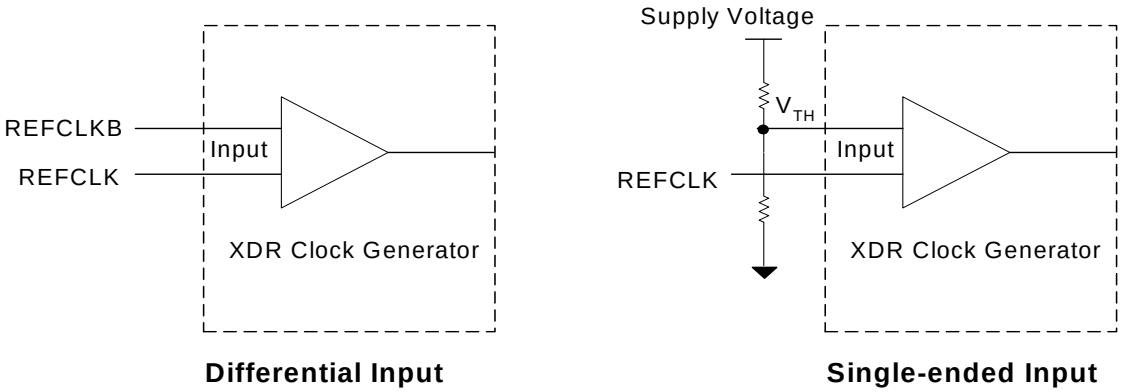
Bit	Register	POD	Type	Description
7	Reserved	0	RW	Reserved (no internal function)
6	Reserved	0	RW	
5	Reserved	0	RW	
4	Reserved	0	RW	
3	Reserved	1	RW	Reserved (must be set to ‘1’ for proper operation)
2	REFSEL	0	RW	Reference Frequency Select (reference Table 3 on page 3)
1	Reserved	0	RW	Reserved (must be set to ‘0’ for proper operation)
0	RegTest	0	RW	Reserved (must be set to ‘0’ for proper operation)

Table 8. Command Code 82h[5]

Bit	Register	POD	Type	Description
7	Device Revision Number	?	RO	Contact factory for Device Revision Number information.
6		?	RO	
5		?	RO	
4		?	RO	
3		?	RO	
2	Vendor ID	0	RO	Rambus assigned Vendor ID Code
1		1	RO	
0		0	RO	

Note
5. RW = Read and Write, RO = Read Only, POD = Power on default. See Table 3 on page 3 for PLL multipliers and Table 5 on page 4 for clock output selections.

Figure 2. Differential and Single-Ended Clock Inputs



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Clock Buffer Supply Voltage		–0.5	4.6	V
V_{DDC}	Core Supply Voltage		–0.5	4.6	V
V_{DDP}	PLL Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage (SCL and SDA)	Relative to V_{SS}	–0.5	4.6	V
	Input Voltage (REFCLK/REFCLKB)	Relative to V_{SS}	–0.5	V_{DD} + 1.0	V
	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JA}$	Junction to Ambient thermal resistance	Zero air flow	–	100	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V

DC Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DDP}	Supply Voltage for PLL	2.5V ± 5%	2.375	2.625	V
V_{DDC}	Supply Voltage for Core	2.5V ± 5%	2.375	2.625	V
V_{DD}	Supply Voltage for Clock Buffers	2.5V ± 5%	2.375	2.625	V
V_{IHCLK}	Input High Voltage, REFCLK/REFCLKB		0.6	0.95	V
V_{ILCLK}	Input Low Voltage, REFCLK/REFCLKB		–0.15	+0.15	V
V_{IXCLK}[6]	Crossing Point Voltage, REFCLK/REFCLKB		200	550	mV
ΔV_{IXCLK}[6]	Difference in Crossing Point Voltage, REFCLK/REFCLKB		–	150	mV
V_{IH}	Input Signal High Voltage at ID0, ID1, EN, and /BYPASS		1.4	2.625	V
V_{IL}	Input Signal Low Voltage at ID0, ID1, EN, and /BYPASS		–0.15	0.8	V
$V_{IH,SM}$	Input Signal High Voltage at SCL and SDA[7]		1.4	3.465	V
$V_{IL,SM}$	Input Signal Low Voltage at SCL and SDA		–0.15	0.8	V
V_{TH}[8]	Input Threshold Voltage for single-ended REFCLK		0.35	$0.5V_{DD}$	V
$V_{IH,SE}$	Input Signal High Voltage for single-ended REFCLK		V_{TH} + 0.3	2.625	V
$V_{IL,SE}$	Input Signal Low Voltage for single-ended REFCLK		–0.15	V_{TH} – 0.3	V
T_A	Ambient Operating Temperature		0	70	°C

Notes

6. Not 100% tested except V_{IXCLK} and ΔV_{IXCLK}. Parameters guaranteed by design and characterizations, not 100% tested in production.
7. This range of SCL and SDA input high voltage enables the CY24272 for use with 3.3V, 2.5V, or 1.8V SMBus voltages.
8. Single-ended operation guaranteed only when $0.8 < (V_{IH,SE} – V_{TH})/(V_{TH} – V_{IL,SE}) < 1.2$.

AC Operating Conditions

The AC operating conditions follow.[6]

Parameter	Description	Condition	Min	Max	Unit
$t_{CYCLE,IN}$	REFCLK, REFCLKB input cycle time	REFSEL = 0, /BYPASS = High	9	11	ns
		REFSEL = 1, /BYPASS = High	7	8	ns
		/BYPASS = Low	4	–	ns
$t_{JIT,IN(cc)}$	Input Cycle to Cycle Jitter[9]		–	185	ps
t_{DCIN}[10]	Input Duty Cycle	Over 10,000 cycles	40%	60%	t_{CYCLE}
t_{RIN} / t_{FIN}	Rise and Fall Times	Measured at 20%–80% of input voltage for REFCLK and REFCLKB inputs	175	700	ps
Δt_{RIN} / t_{FIN}	Rise and Fall Times Difference		–	150	ps
p_{MIN}[11]	Modulation Index for triangular modulation		–	0.6	%
	Modulation Index for non-triangular modulation		–	0.5[12]	%
f_{MIN}[11]	Input Frequency Modulation		30	33	kHz
$t_{SR,IN}$	Input Slew Rate (measured at 20%–80% of input voltage) for REFCLK		1	4	V/ns
$C_{IN,REF}$	Capacitance at REFCLK inputs		–	7	pF
$C_{IN,CMOS}$	Capacitance at CMOS inputs		–	10	pF
f_{SCL}	SMBus clock frequency input in SCL pin		DC	100	kHz

DC Electrical Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{OX}[6]	Differential output crossing point voltage[13]	–	1.08	–	V
V_{COS}[6]	Output voltage swing (peak-to-peak single-ended)[14]	–	400	–	mV
$V_{OL,ABS}$	Absolute output low voltage at CLK[3:0], CLK[3:0]B[15]	0.85	–	–	V
V_{ISET}	Reference voltage for swing controlled current, I_{REF}	0.98	1.0	1.02	V
I_{DD}[7]	Power Supply Current at 2.625V, f_{ref} = 100 MHz, and f_{out} = 300 MHz	–	–	85	mA
I_{DD}[7]	Power Supply Current at 2.625V, f_{ref} = 133 MHz, and f_{out} = 667 MHz	–	–	125	mA
I_{OL}/I_{REF}	Ratio of output low current to reference current[16]	6.8	7.0	7.2	
$I_{OL,ABS}$	Minimum current at $V_{OL,ABS}$[17]	25	–	–	mA
$V_{OL,SDA}$	SDA output low voltage at test condition of SDA output low current = 4 mA	–	–	0.4	V
$I_{OL,SDA}$	SDA output low voltage at test condition of SDA voltage = 0.8V	6	–	–	mA
I_{OZ}	Current during High Z per pin at CLK[3:0], CLK[3:0]B	–	–	10	µA
Z_{OUT}	Output dynamic impedance when clock output signal is at V_{OL} = 0.9V[18]	1000	–	–	Ω

Notes

9. Jitter measured at crossing points and is the absolute value of the worst case deviation.
10. Measured at crossing points.
11. If input modulation is used; input modulation is allowed but not required.
12. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew that cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.
13. V_{OX} is measured on external divider network.
14. V_{COS} = (clock output high voltage – clock output low voltage), measured on the external divider network.
15. V_{OL_ABS} is measured at the clock output pins of the package.
16. I_{REF} is equal to V_{ISET}/R_{RC}.
17. Minimum $I_{OL,ABS}$ is measured at the clock output pin with R_{RC} = 266 ohms or less.
18. Z_{OUT} is defined at the output pins as (0.94V – 0.90V)/($I_{0.94}$ – $I_{0.90}$) under conditions specified for $I_{OL,\ ABS}$.

AC Electrical Specification

The AC Electrical specifications follow. [6]

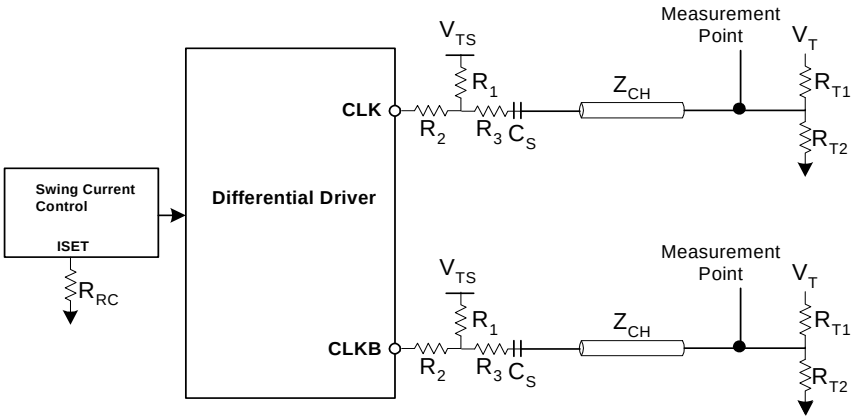
Parameter	Description	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle time[19]	1.25		3.34	ns
$t_{JIT(cc)}$	Jitter over 1-6 clock cycles at 400–635 MHz[20]	–	25	40	ps
	Jitter over 1-6 clock cycles at 638–667 MHz	–	25	30	ps
L_{20}	Phase noise SSB spectral purity L(f) at 20 MHz offset: 400–500 MHz (In addition, device must not exceed L(f) = 10log[1+(50x10^6/f)$^{2.4}$] –138 for f = 1 MHz to 100 MHz except for the region near f = REFCLK/Q where Q is the value of the internal reference divider.)	–	–135	–128	dBC/Hz
$t_{JIT(hper,cc)}$	Cycle-to-cycle duty cycle error at 400–635 MHz	–	25	40	ps
	Cycle-to-cycle duty cycle error at 636–667 MHz	–	25	30	ps
Δt_{SKEW}	Drift in t_{SKEW} when ambient temperature varies between 0°C and 70°C and supply voltage varies between 2.375V and 2.625V.[21]	–	–	15	ps
DC	Long term average output duty cycle	45%	50	55%	t_{CYCLE}
$t_{EER,SCC}$	PLL output phase error when tracking SSC	–100	–	100	ps
t_{CR},t_{CF}	Output rise and fall times at 400–667 MHz (measured at 20%–80% of output voltage)	–	150	–	ps
$t_{CR,CF}$	Difference between output rise and fall times on the same pin of the single device (20%–80%) of 400–667 MHz[22]	–	–	100	ps

Table 9. SMBus Timing Specification

Parameter	Description	Min	Max	Units
FSMB	SMBus Operating Frequency	10	100	kHz
TBUF	Bus free time between Stop and Start Condition	4.7		µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	4.0		µs
TSU:STA	Repeated Start Condition setup time	4.7		µs
TSU:STO	Stop Condition setup time	4.0		µs
THD:DAT	Data Hold time	0		ns
TSU:DAT	Data Setup time	250		ns
TTIMEOUT	Detect clock low timeout			Not supported
TLOW	Clock low period	4.7		µs
THIGH	Clock high period	4.0	50	µs
TLOW:SEXT	Cumulative clock low extend time (slave device)		25	ms CY24272 doesn't extend
TLOW:MEXT	Cumulative clock low extend time (master device)		10	ms
TF	Clock/Data Fall Time		300	ns
TR	Clock/Data Rise Time		1000	ns
TPOR	Time in which a device must be operational after power on reset		500	ms

Test and Measurement Setup

Figure 3. Clock Outputs



Example External Resistor Values and Termination Voltages for a 50Ω Channel

Parameter	Value	Unit
R_1	33.0	Ω
R_2	18.0	Ω
R_3	17.0	Ω
R_{T1}	60.4	Ω
R_{T2}	301	Ω
C_S	2700	pF
R_{RC}	432	Ω
V_{TS}	2.5V	V
V_T	1.2V	V

Signal Waveforms

A physical signal that appears at the pins of a device is deemed valid or invalid depending on its voltage and timing relations with other signals. Input and output voltage waveforms are defined as shown in Figure 4 on page 11. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as V_H–V_L.

Figure 5 on page 11 shows the definition of the output crossing point. The nominal crossing point between the complementary outputs is defined as the 50% point of the DC voltage levels. There are two crossing points defined: Vx+ at the rising edge of CLK and Vx– at the falling edge of CLK. For some waveforms, both Vx+ and Vx– are below Vx,nom (for example, if t_{CR} is larger than t_{CF}).

Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 6 on page 11 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles. Equal requirements apply rising edges of the CLK signal. Figure 7 on page 11 shows the definition of cycle-to-cycle duty cycle error ($t_{DC,ERR}$). Cycle-to-cycle duty cycle is defined as the difference between t_{PW+} (high times) of adjacent differential clock cycles. Equal requirements apply to t_{PW-}, low times of the differential click cycles.

Notes

19. Max and min output clock cycle times are based on nominal outputs frequency of 300 and 667 MHz, respectively. For spread spectrum modulated differential or single-ended REFCLK, the output clock tracks the modulation of the input.
20. Output short term jitter spec is the absolute value of the worst case deviation.
21. t_{SKEW} is the timing difference between any two of the four differential clocks and is measured at common mode voltage. Δt_{SKEW} is the change in t_{SKEW} when the operating temperature and supply voltage change.
22. $t_{CR,CF}$ applies only when appropriate R_{RC} and output resistor network resistor values are selected to match pull up and pull down currents.

Figure 4. Input and Output Waveforms

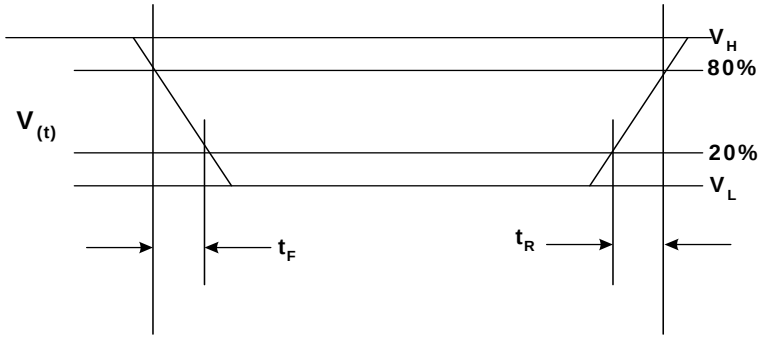


Figure 5. Crossing Point Voltage

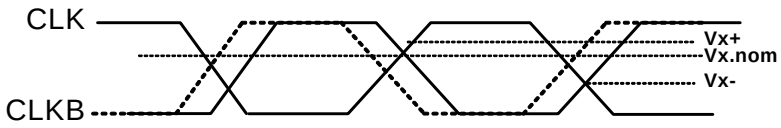
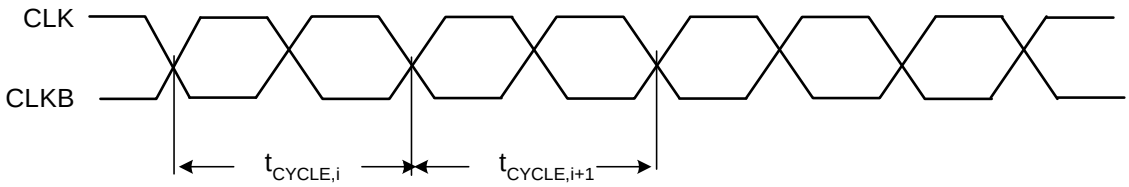
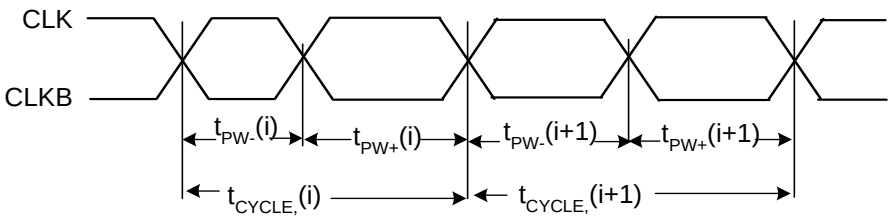


Figure 6. Cycle-to-cycle Jitter



$t_J = t_{CYCLE,i} - t_{CYCLE,i+1}$ over 10,000 consecutive cycles

Figure 7. Cycle-to-cycle Duty-cycle Error



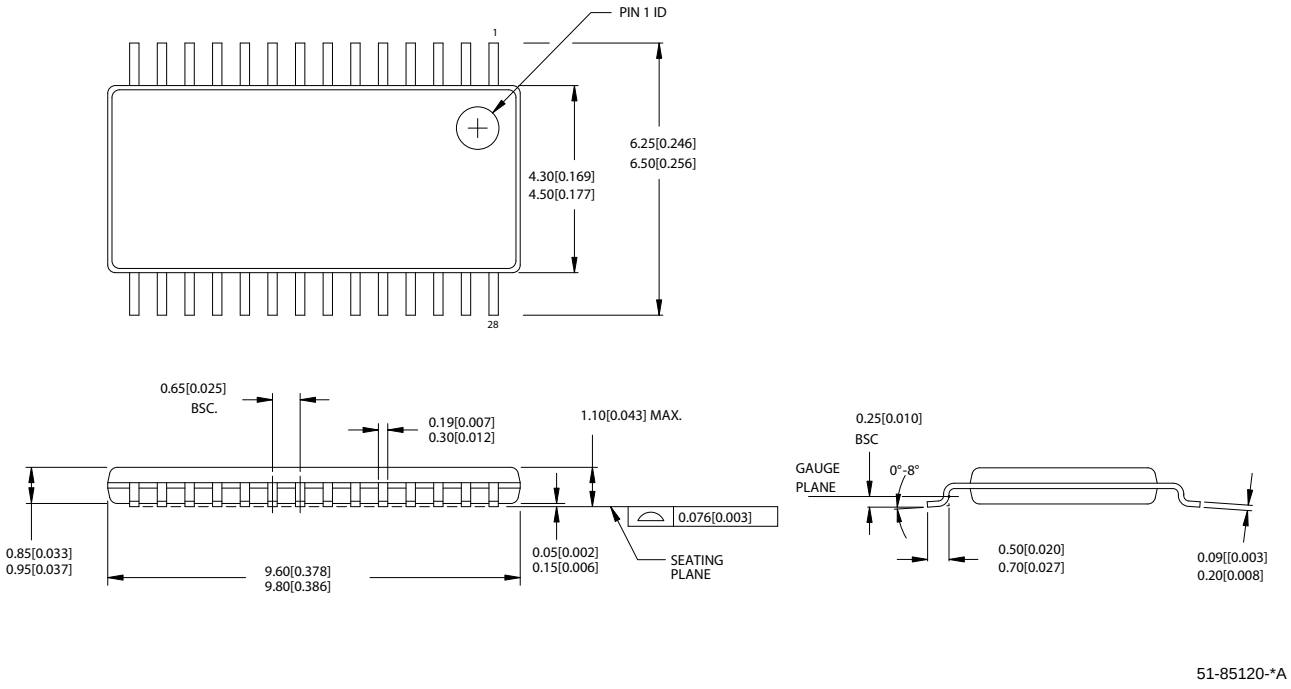
$t_{DC,ERR} = t_{PW-}(i) - t_{PW-}(i+1)$ and $t_{PW-}(i+1) - t_{PW+}(i+1)$

Ordering Information

Part Number	Package Type	Product Flow
Pb-Free		
CY24272ZXC	28-pin TSSOP	Commercial, 0°C to 70°C
CY24272ZXCT	28-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C

Package Drawing and Dimension

Figure 8. 28-Pin Thin Shrunk Small Outline Package (4.40-mm Body) ZZ28



Document History Page

Document Title: CY24272 Rambus® XDR™ Clock Generator with Zero SDA Hold Time Document Number: 001-42414				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1749003	See ECN	KVM/AESA	New data sheet No 8 or 15/2 multipliers or 133MHz * 4 option Max frequency is 667MHz