



## 74LCX162541

Low voltage CMOS 16-bit bus buffer (3-state)  
with 5V tolerant inputs and outputs

### Features

- 5V tolerant inputs and outputs
- High speed:
  - $t_{PD} = 4.4\text{ns}$  (Max) at  $V_{CC} = 3\text{V}$
- Power down protection on inputs and outputs
- Symmetrical output impedance:
  - $|I_{OH}| = I_{OL} = 12\text{mA}$  (Min) at  $V_{CC} = 3\text{V}$
- PCI bus levels guaranteed at 12mA
- Balanced propagation delays:
  - $t_{PLH} \cong t_{PHL}$
- $26\Omega$  serie resistor in outputs
- Operating voltage range:
  - $V_{CC}$  (Opr) = 2.0V to 3.6V
- Pin and function compatible with 74 series 162541
- Latch-up performance exceeds 500mA (JESD 17)
- ESD performance:
  - HBM > 2000V (MIL STD 883 method 3015); MM > 200V



### Description

The 74LCX162541 is a low voltage CMOS 16 bit bus buffer (non-inverted) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

This is composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffers section, the 3 state control gate operates as a two input AND such that if either  $n\overline{G}1$  and  $n\overline{G}2$  are high, all outputs are in the high impedance state.

This device is designed to be used with 3 state memory address drivers, etc.

The device circuits is including  $26\Omega$  series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### Order codes

Part number	Package	Packaging
74LCX162541TTR	TSSOP48	Tape and reel

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# 1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

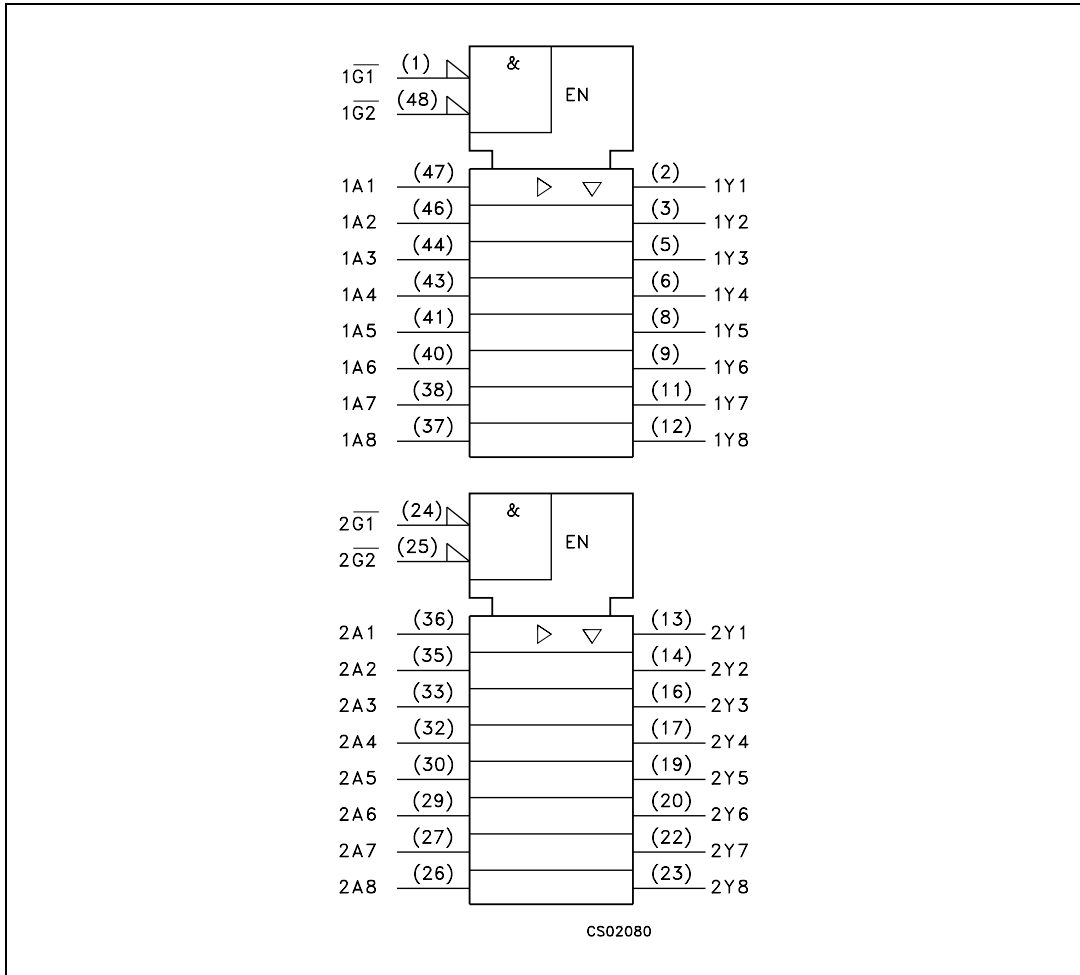
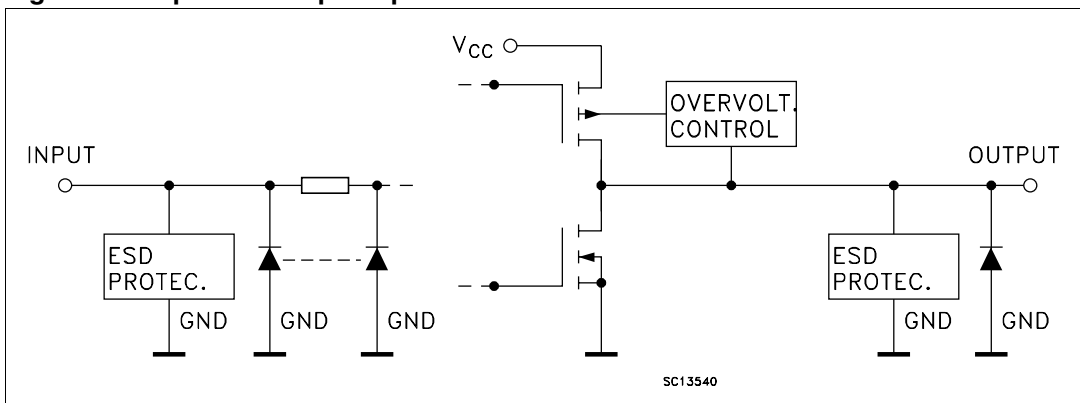


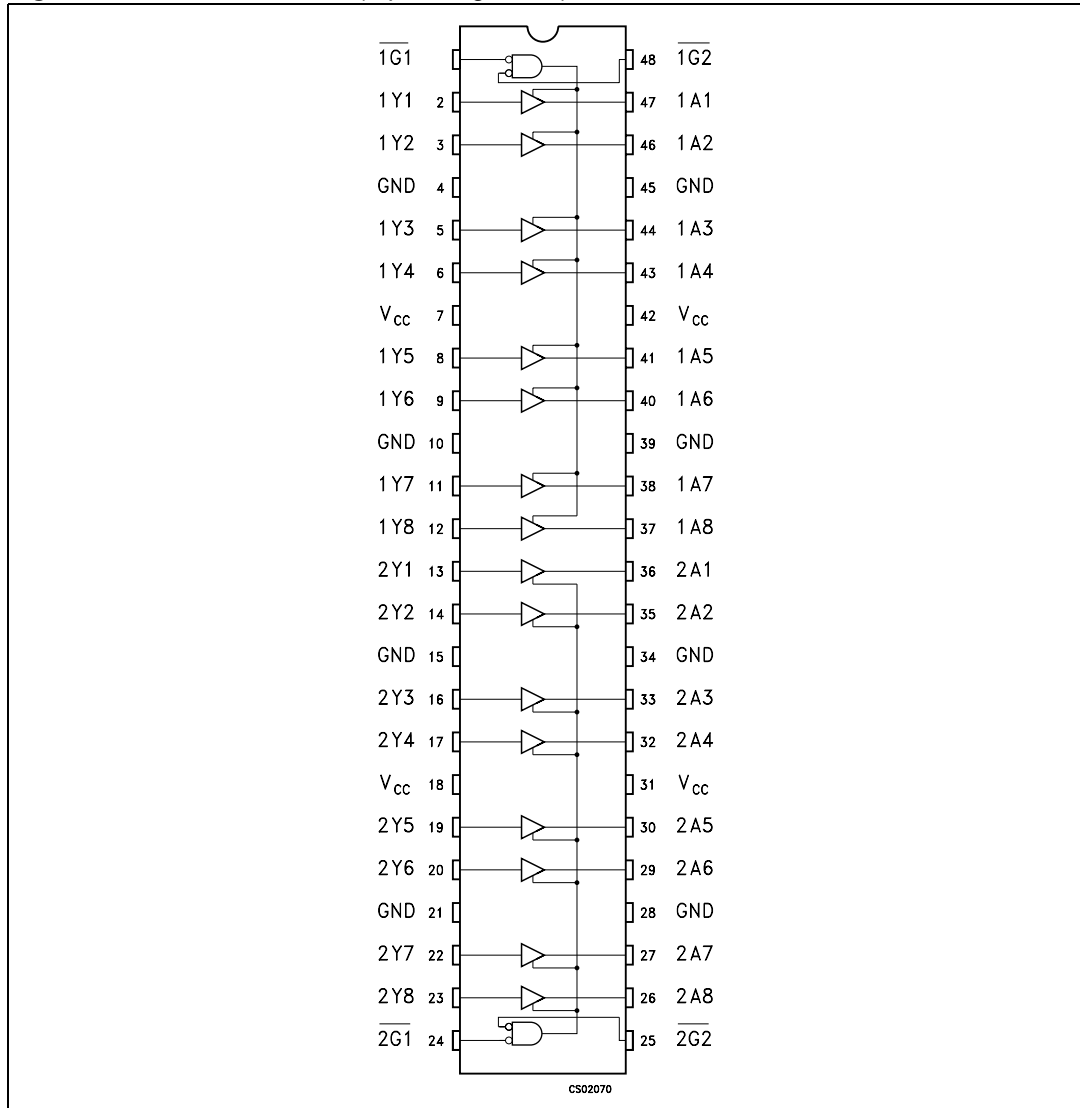
Figure 2. Input and output equivalent circuit



## 2 Pin settings

### 2.1 Pin connection

Figure 3. Pin connection (top through view)



## 2.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1, 48	$\overline{1G1}, \overline{1G2}$	Output enable inputs
2, 3, 5, 6, 8, 9, 11, 12	1Y1 to 1Y8	Data outputs
13, 14, 16, 17, 19, 20, 22, 23	2Y1 to 2Y8	Data outputs
24, 25	$\overline{2G1}, \overline{2G2}$	Output enable inputs
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data outputs
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

## 3 Logic states

### 3.1 Truth table

Table 2. Truth table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	An	Yn
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

Note: X : Do not care  
Z : High impedance

## 4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_I$	DC input voltage	-0.5 to +7.0	V
$V_O$	DC output voltage (OFF state)	-0.5 to +7.0	V
$V_O$	DC output voltage (high or low state) <sup>(1)</sup>	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC input diode current	-50	mA
$I_{OK}$	DC output diode current <sup>(2)</sup>	-50	mA
$I_O$	DC output current	$\pm 50$	mA
$I_{CC}$	DC supply current per supply pin	$\pm 100$	mA
$I_{GND}$	DC ground current per supply pin	$\pm 100$	mA
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_L$	Lead temperature (10 sec)	300	°C

1.  $I_O$  absolute maximum rating must be observed
2.  $V_O < GND$

### 4.1 Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	2.0 to 3.6	V
$V_I$	Input voltage	0 to 5.5	V
$V_O$	Output voltage (OFF state)	0 to 5.5	V
$V_O$	Output voltage (high or low state)	0 to $V_{CC}$	V
$I_{OH}, I_{OL}$	High or low level output current ( $V_{CC} = 3.0$ to $3.6V$ )	$\pm 12$	mA
$I_{OH}, I_{OL}$	High or low level output current ( $V_{CC} = 2.7V$ )	$\pm 8$	mA
$T_{op}$	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time <sup>(2)</sup>	0 to 10	ns/V

1. Truth table guaranteed: 1.5V to 3.6V
2.  $V_{IN}$  from 0.8V to 2V at  $V_{CC} = 3.0V$

## 5 Electrical characteristics

**Table 5. DC specification**

Symbol	Parameter	Test condition		Value		Unit
		V <sub>CC</sub> (V)		-40 to 85 °C		
				Min	Max	
V <sub>IH</sub>	High level input voltage	2.7 to 3.6		2.0		V
V <sub>IL</sub>	Low level input voltage					0.8
V <sub>OH</sub>	High level output voltage	2.7 to 3.6	I <sub>O</sub> = -100 μA	V <sub>CC</sub> -0.2		V
		2.7	I <sub>O</sub> = -8 mA	2.0		
		3.0	I <sub>O</sub> = -6 mA	2.4		
			I <sub>O</sub> = -12 mA	2.0		
V <sub>OL</sub>	Low level output voltage	2.7 to 3.6	I <sub>O</sub> = 100 μA		0.2	V
		2.7	I <sub>O</sub> = 8 mA		0.6	
		3.0	I <sub>O</sub> = 6 mA		0.55	
			I <sub>O</sub> = 12 mA		0.8	
I <sub>I</sub>	Input leakage current	2.7 to 3.6	V <sub>I</sub> = 0 to 5.5V		± 5	μA
I <sub>off</sub>	Power OFF leakage current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>OZ</sub>	High impedance output leakage current	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to V <sub>CC</sub>		± 5	μA
I <sub>CC</sub>	Quiescent supply current	2.7 to 3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		20	μA
			V <sub>I</sub> or V <sub>O</sub> = 3.6 to 5.5V		± 20	
ΔI <sub>CC</sub>	I <sub>CC</sub> incr. per Input	2.7 to 3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

**Table 6. Dynamic switching characteristics**

Symbol	Parameter	Test condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min	Typ	Max	
V <sub>OLP</sub>	Dynamic low level quiet output <sup>(1)</sup>	3.3	C <sub>L</sub> = 50pF V <sub>IL</sub> = 0V, V <sub>IH</sub> = 3.3V		0.8		V
V <sub>OLV</sub>					-0.8		

1. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

**Table 7. AC electrical characteristics**

Symbol	Parameter	Test Condition				Value		Unit
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	R <sub>L</sub> (Ω)	t <sub>s</sub> = t <sub>r</sub> (ns)	-40 to 85 °C		
						Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	2.7	50	500	2.5	1.5	5.6	ns
		3.0 to 3.6				1.5	4.4	
t <sub>PZL</sub> t <sub>PZH</sub>	Output enable time	2.7	50	500	2.5	1.5	6.3	ns
		3.0 to 3.6				1.5	5.9	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output disable time	2.7	50	500	2.5	1.5	6.3	ns
		3.0 to 3.6				1.5	5.9	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to output skew time <sup>(1)</sup> <sup>(2)</sup>	3.0 to 3.6	50	500	2.5		1.0	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|)
2. Parameter guaranteed by design

**Table 8. Capacitive characteristics**

Symbol	Parameter	Test Condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min	Typ	Max	
C <sub>IN</sub>	Input capacitance				4		pF
C <sub>OUT</sub>	Output capacitance				10		pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1)</sup>	3.3	f <sub>IN</sub> = 10MHz V <sub>IN</sub> = 0 or V <sub>CC</sub>		50		pF

1. C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/16 (per circuit)



## 6 Test circuit

Figure 4. Test circuit

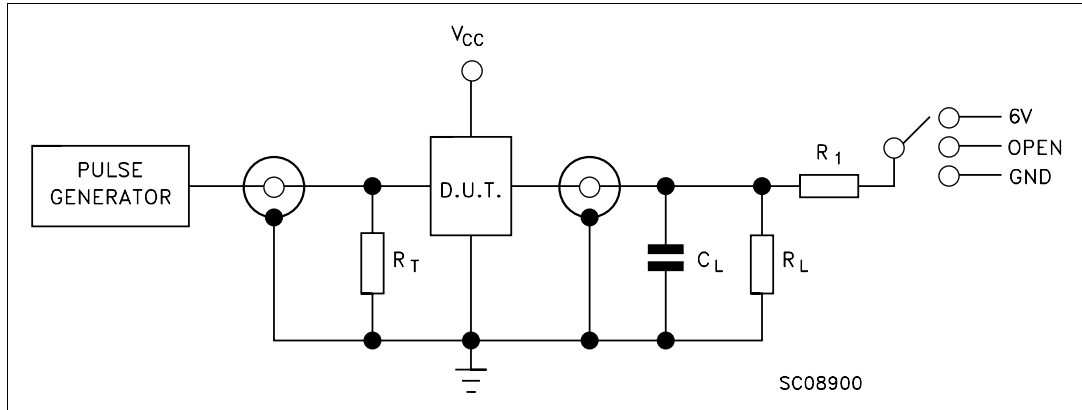


Figure 5. Test circuit

Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

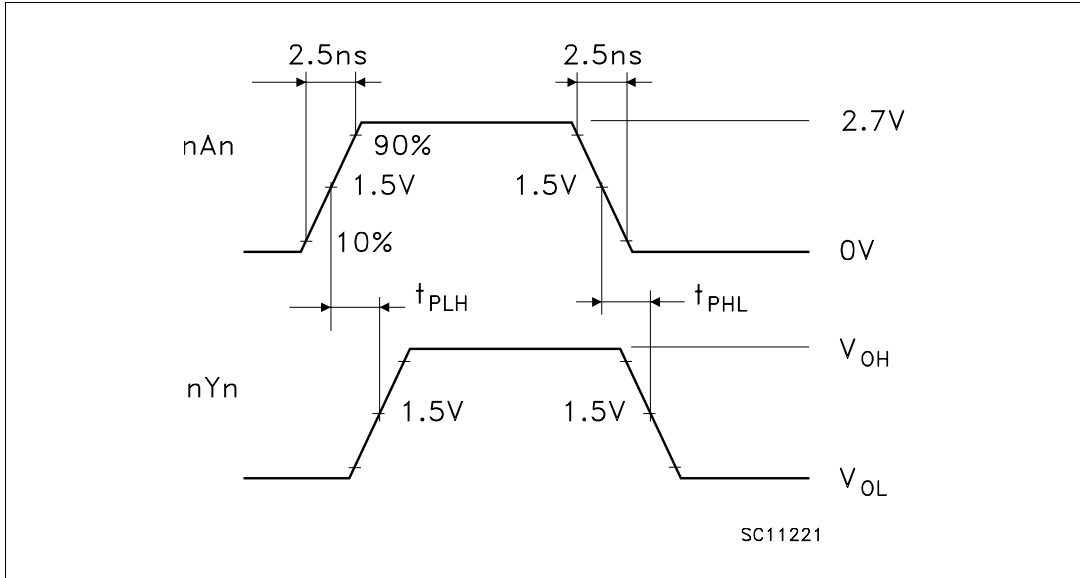
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$  or equivalent

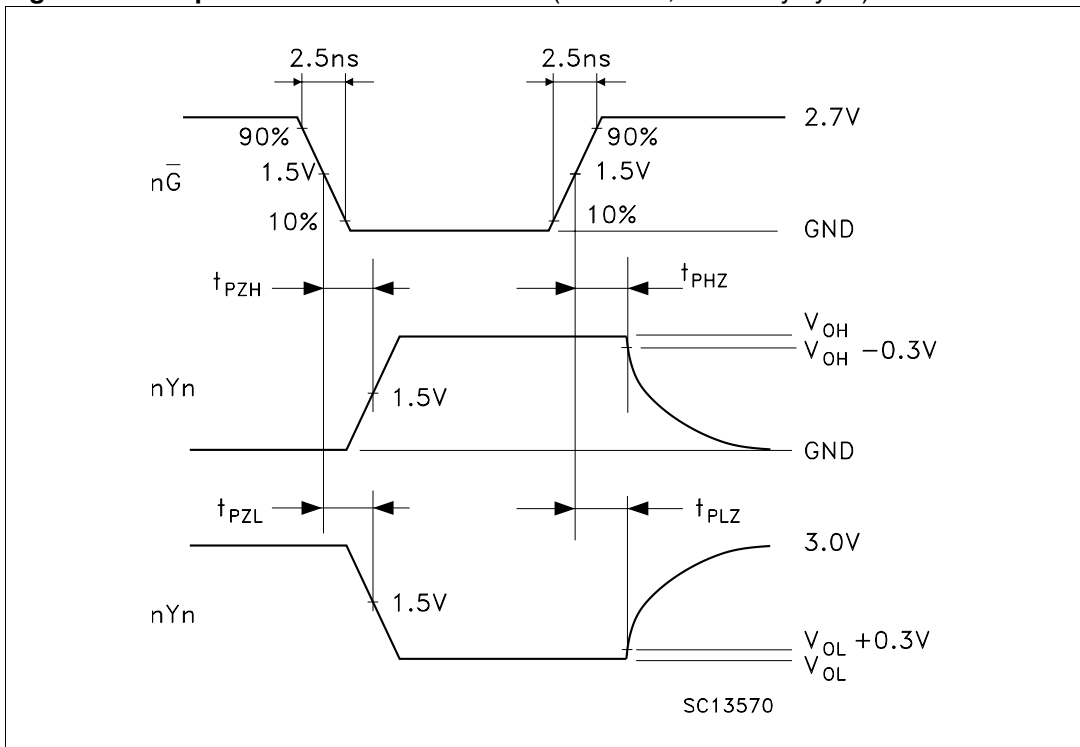
$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

# 7 Waveforms

**Figure 6. Propagation delays (f = 1MHz; 50% duty cycle)**



**Figure 7. Output enable and disable time (f = 1MHz; 50% duty cycle)**

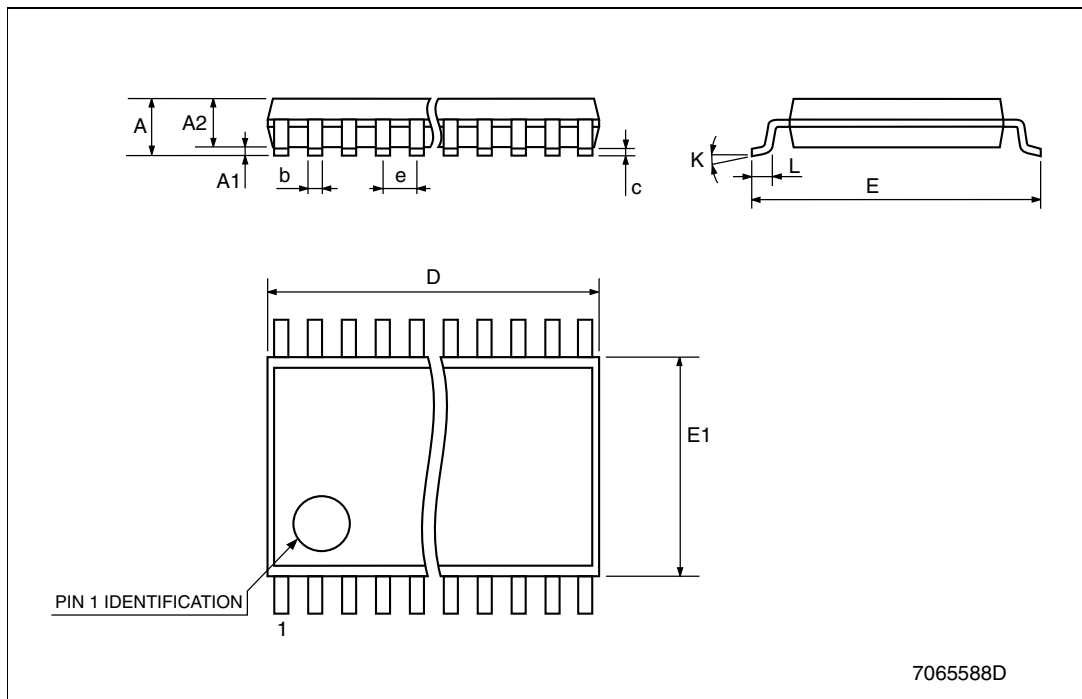


## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

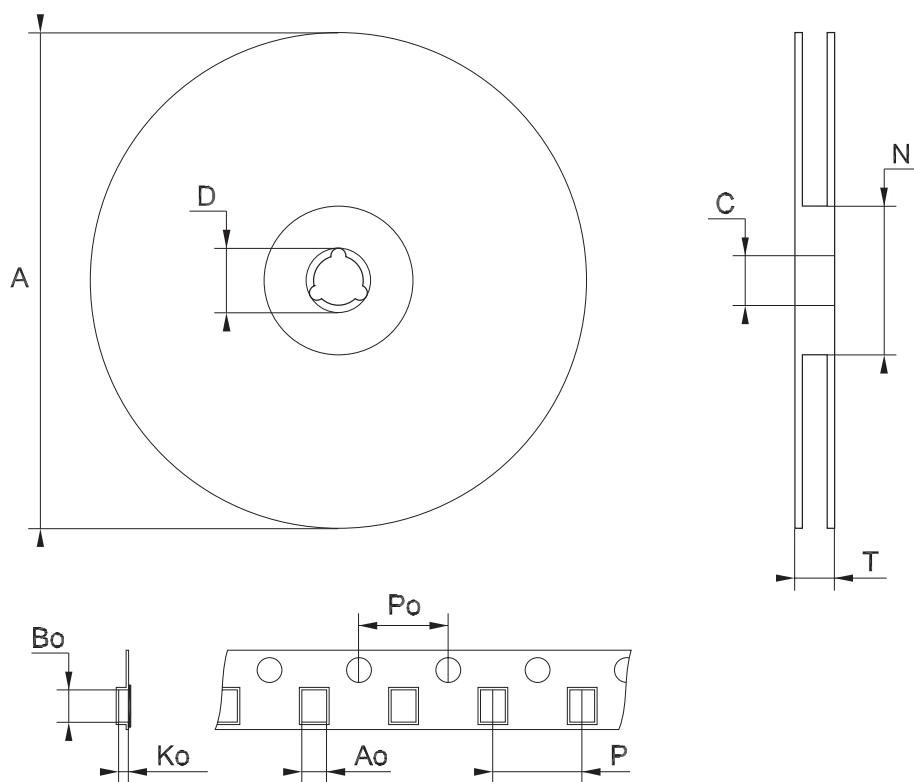
**TSSOP48 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.45		0.75	0.018		0.030



**Tape & Reel TSSOP48 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

## 9 Revision history

**Table 9. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
15-Sep-2004	2	Ordering Codes Revision - pag. 1.
06-Feb-2007	3	Document reformatted, temperature ranges updated

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