Description

YB7002 charge high voltage photoflash capacitors quickly and efficiently. Designed for use in digital and film cameras, these devices use flyback topology to achieve efficiencies up to four times better than competing flash modules. A unique peak inductor current control mechanism maintains current-limited mode transformer operation throughout the entire charge cycle, eliminating the high inrush current often found in modules.

YB7002 output voltage sensing scheme monitors the flyback voltage to directly regulate the output voltage. This feature allows the capacitor to be held at a fully charged state without excessive power consumption. Adjustable refresh time is fully controllable by the user with a resistor. The DONE pin signals that the capacitor is full charged.

Features

- Charge Any Size Photoflash Capacitor
- Support Operation from Two AA Cells or Any Supply from 1.8V to 16V
- Use Standard transformers
- No High Voltage Zener Diode Required
- Built in 40V output switch
- Adjustable Output Voltage
- Adjustable Peak Switch Current
- Automatic Refresh with adjustable timer
- Charge Complete Indicator
- Small 10-Lead MSOP Packages

Applications

- Digital Camera Flash unit
- Film Camera Flash Unit
- High Voltage Power Supplies

Typical Application Circuit

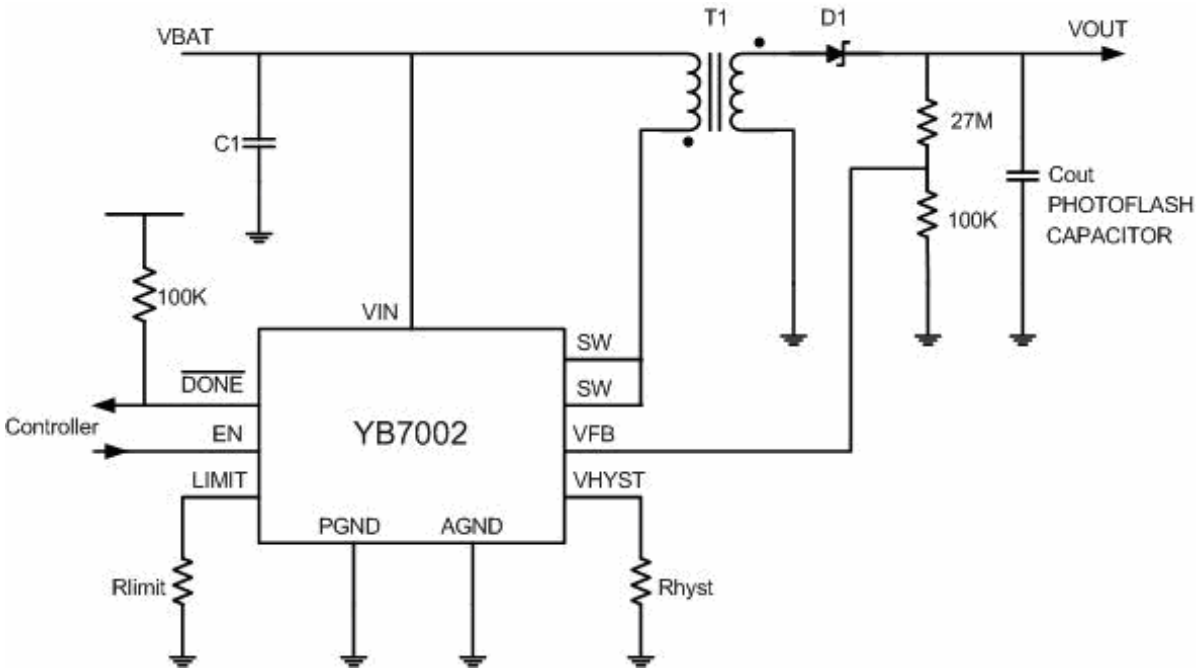


Figure1：Typical Application Circuit

Pin Description

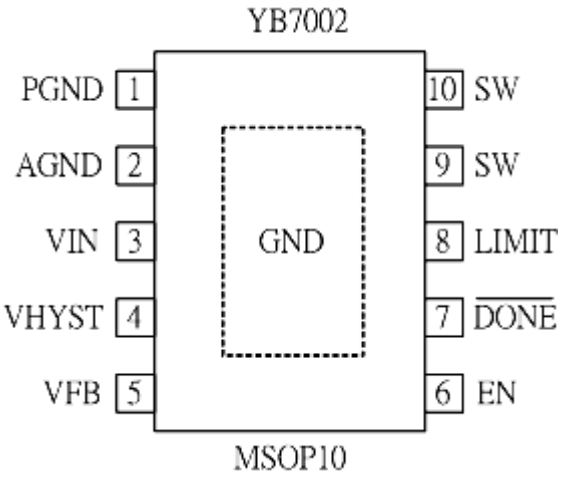


Figure2：YB7002 MSOP10

Pin Designator

Table1：

Pin	NAME	Description
1	PGND	Power ground, tie solidly to system ground of the board.
2	AGND	Analog ground, tie solidly to system ground of the board.
3	V_{IN}	Input supply pin. Must be locally bypassed capacitor to eliminate noise.
4	V_{HYST}	Connecting a resistor RHYST from VHYST to ground will set the refresh time. A 13.5K resistor and RHYST form a divider circuit to restart the charging cycle once VFB is dropping below Vhyst.
5	V_{FB}	A resistor divider from VOUT to ground enables the system to sense VOUT voltage and determine the charging and recharging cycles.
6	EN	Device enable, a1.8V or above will turn on the IC. Below 0.4V will put the chip in shut down mode.
7	DONE	Once VOUT voltage reaches above the designated value, DONE pin will be pulled low to indicate charging is completed.
8	LIMIT	Tie a resistor Rlimit from Limit to ground will adjust the value of the peak Switch pin current. A 11uA current going through Rlimit sets up the peak voltage the sense node can reach (see the block diagram).
9	SW	They connect to the collector of the power NPN device.
10		

Ordering Information

Table2：

Order Number	Package Type	Supplied as	Package Marking
YB7002	MSOP10	2500 units Tape & Reel	YB7002

Package Information

Absolute Maximum Retings

Vin	16V
SW voltage	40V
DONE	16V
Current into DONE pin	1mA
Maximum Junction Temp, Tj (note 2)	125°C
Storage Temperature Range	-65°Cto 50°C
Lead Temperature (Soldering 10 sec)	300°C

Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Recommended Operating Conditions

Operating Temperature	-40℃ ~ +85°C
Supply Voltage	2 V ~ 16V
Maximum SW Voltage	40V

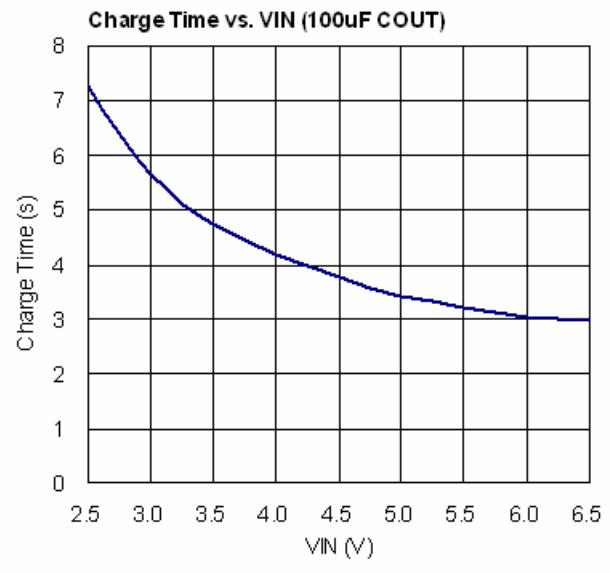
Electricity Characteristics

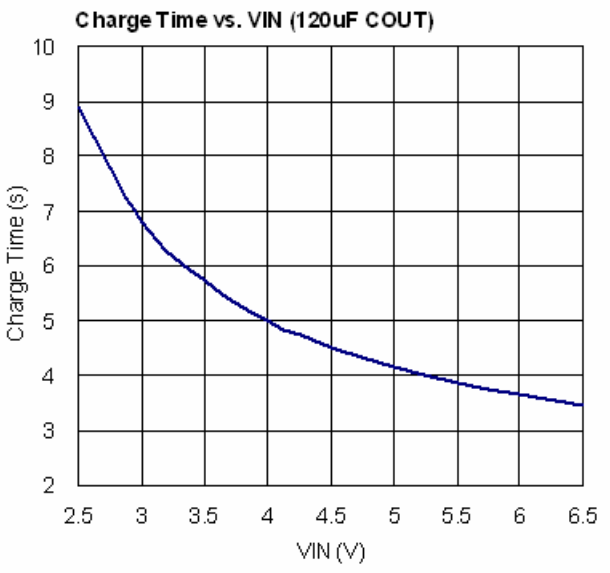
Table3：(T_A=25°C, Vin=3.3V unless otherwise noted)

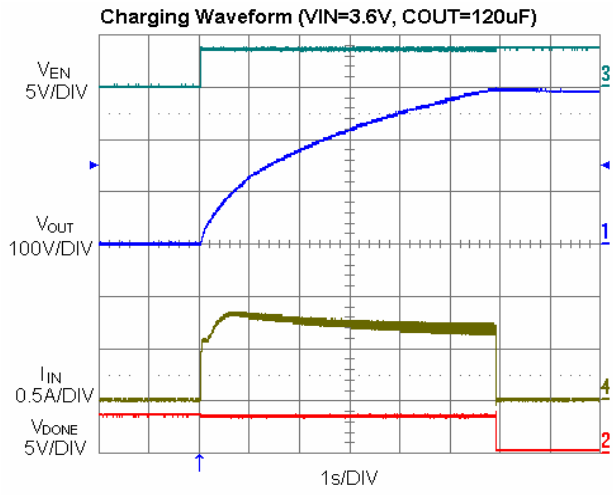
Symbol	Function Parameter	Test Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2		16	V
I_Q (Quiescent Current)	Not Switching	V_{FB} = 1.5V			400	uA
	Shutdown	EN =0V			10	
V_{FB}	FB threshold voltage		1.21	1.23	1.25	V
I_{FB}	FB pin bias current	V_{FB}=1.23V			250	nA
$I_{PEAK,PRI}$	Primary site peak current limit	R_{LIMIT}=26K	1.4	1.5	1.6	A
I_{LKG}	SW Leakage Current	V_{SW}=40V, V_{FB}=1.5V		1	10	uA
T_{OFF}	Switch Off Time			1000		ns
$V_{CE,SAT}$	Switch saturation voltage	I_{SW}=300mA		220	340	mV
On/Off Hystersis	SW On/Off hystersis ratio	R_{HYST}=150KΩ, Note 1		8		%
V_{IH}	EN pin input voltage high		1.8			V
V_{IL}	EN pin input voltage low				0.4	V
I_{EN}	EN pin bias current	V_{EN}=3V		4.5	15	uA
	EN pin bias current	V_{EN}=0V		0.01	1	
V_{OH}	DONE pin output signal high	100KΩ at VIN to DONE		3.3		V
V_{OL}	DONE pin output signal low	33uA into DONE pin		100	200	mV

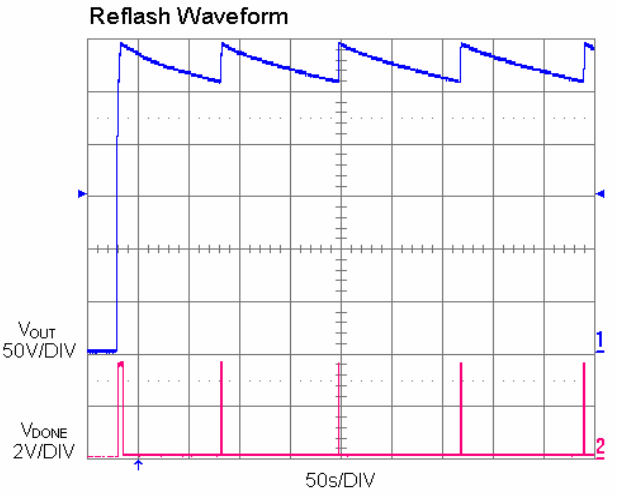
Note：

Typical Performance Characteristics









Functional Block

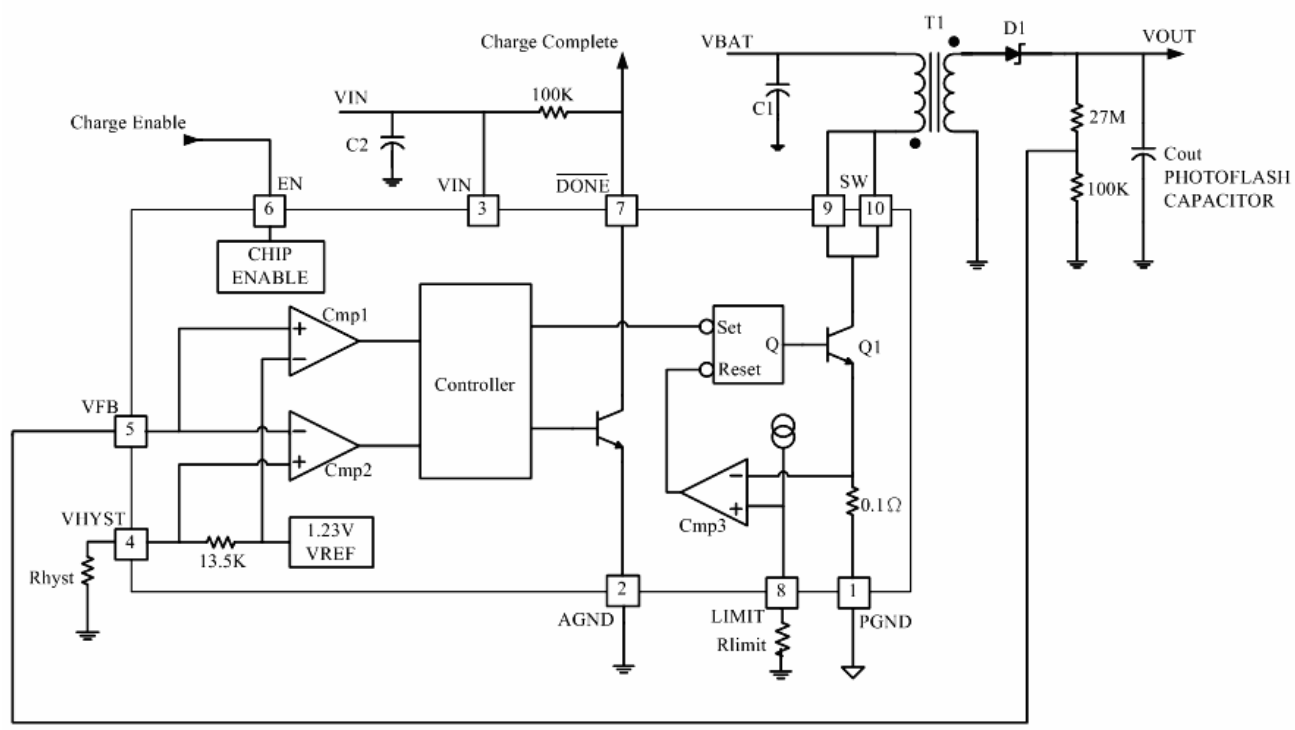


Figure3：Functional Block

Functional Description

YB7002 employs the peak-current-limit scheme to control the charging of the inductor current. Once the inductor reaches the preset value determined by the Limit Pin, output power NPN is shut off and the primary side energy is delivered to the secondary side capacitor. The discharging time is set to be about 1us. Once the discharge cycle is completed, the power NPN is on again. If the secondary side output voltage has not yet reached the designated value, the inductor current will be charged up to the preset value again. This charging and discharging sequence will repeat itself until the output capacitor voltage gets to the designated value and triggers the on-off latch to hold off the power NPN regardless the inductor current value.
As the power switch is off, output capacitor starts to drop slowly due to its own leakage and the resistor divider. When VFB voltage is below VHYST, on-off latch turns on the power NPN again and the charging cycle is enabled.
User is able to use resistors to set Limit Pin value and V voltage. A 11uA current source is coming out of the IC and going through the limit resistor R to ground. Limit pin voltage determines the peak inductor current. The higher the Limit pin voltage,
the larger the peak inductor current would be. **USER MUST BE CAREFUL WITH THE THERMAL EFFECT GENERATED DURING THE CAPACITOR CHARGING CYCLE.** To reduce the thermal temperature, user can lower the resistor R value to reduce the peak inductor current.

Application Information

Hysteresis voltage is setup by connecting a resistor Rhyst from VHYST to ground. A resistor divider of 13.5k (internal resistor) and Rhyst from bandgap voltage will determine heysteresis voltage. Once VFB drops below VHYST voltage, charging cycle is activated again. To calculate the refresh time, consider the followings:

$$C_{OUT} \cdot \frac{\partial_{VOUT}}{\partial t} + \frac{V_{OUT}}{R1+R2} + I_{COUT,LEAKAGE} = 0$$

As the capacitor leakage current is a function of output voltage, it can be considered to be constant within the tiny range of voltage from Vout to $VHYST \cdot \frac{R1+R2}{R2}$, where R1 and R2 are the resistor divider at the secondary side output.

By solving the above equation, we can find the time it takes for capacitor voltage to drop from Vout to $VHYST \cdot \frac{R1+R2}{R2}$

For the convenience of the user, two tables have been setup for reference. Table 1 is for Limit Pin while Table 2 is for VHYST. Please check the tables to pick the resistor values for peak primary inductor current and recharge voltage.

Table4

RLIMIT	10 KΩ	15 KΩ	20 KΩ	25 KΩ
Peak Current	0.8A	1A	1.2A	1.3A

Table5 (V_{OUT}=300V)

RHYST	Hysteresis ratio	Recharge Voltage
436.5 KΩ	3%	291V
211.5 KΩ	6%	282V
136.5 KΩ	9%	273V
99 KΩ	12%	264V

Once capacitor reaches the designated voltage, DONE pin will be pulled low to indicate the completion of charging process.When output, voltage drops below secondary capacitance and series resistance will improve system efficiency and performance.

Primary side inductance will affect the charging time. Higher primary side inductance will raise the average discharging current into the output capacitance, resulting a smaller charging time. Yet, thermal effect will become adversely affecting the system. So always pay attention to the amount of dissipated $VHYST \cdot \frac{R1+R2}{R2}$, DONE is released to signal the re-start of charging process.

User always has the freedom to shut off the operation of the chip by pulling the ENABLE pin lower than 0.4V. Also to activate the IC, ENABLE pin NEED needs to be above 1.8V. In shutdown mode, the chip is only drawing about 2uA current.

Component Selection:

The rectifying diode must be of low capacitance type while being able to withstand peak reverse voltage and heavy forward current.

The peak reverse voltage is:

$$V_{R,PEAK} = V_{OUT} - (-N \cdot V_{BAT}) = V_{OUT} + N \cdot V_{BAT}$$

$$I_{SEC,MAX} = \frac{I_{PRI,MAX}}{N}$$

As $I_{PRI,\ MAX}$ is being set by RLIMIT, its value can reach as high as 1.5A.

Since the switching voltage across the rectifying diode is very large, any parasitic capacitance across the diode will translate to huge loss for the system. Moreover, it will slow down the transition of the Switch pin, inducing further loss of efficiency.

Input Capacitor:

Even though the chip is not drawing much current, still a good decoupling capacitor is needed for VIN pin.

It is very important to have a solid VBAT voltage. A low ESR ceramic capacitor is recommended.

Transformer:

A number of issues must be considered before selecting a transformer.

Turn ratio N, primary inductance, primary side series resistance, transformer leakage inductance, secondary capacitance and series resistance, transformer efficiency are the main considerations when choosing a transformer.

$$V_{SWITCH} = V_{BAT} + \frac{V_{OUT} + V_D}{N}$$

Care must be exercised so that V_{SWITCH} will not exceed the maximum voltage breakdown voltage of 40V. Minimizing primary side series resistance, transformer leakage inductance, secondary capacitance and series resistance will improve system efficiency and performance.
Primary side inductance will affect the charging time. Higher primary side inductance will raise the average discharging current into the output capacitance, resulting a smaller charging time. Yet, thermal effect will become adversely affecting the system. So always pay attention to the amount of dissipated power.

Thermal Consideration:

When YB7002 is set to handle high switch current will result in internal power dissipation generating heat. For thermal improvement can be made by use of vias to connects the part and dissipate heat to an internal ground plane.

Placing vias under the exposed thermal pad of package can be lowered significant. Using larger traces and more copper on the top site of board can also further help. With careful PCB layout it is possible to reduce the thermal effect.
Always beware the amount of power dissipated during the charging process.
Too high the temperature built up inside the IC will slow the charging cycle and lengthen the charging time, further worsen the thermal condition of the IC. To resolve the thermal built up issue, reduce RLIMIT which lower the peak switch current.

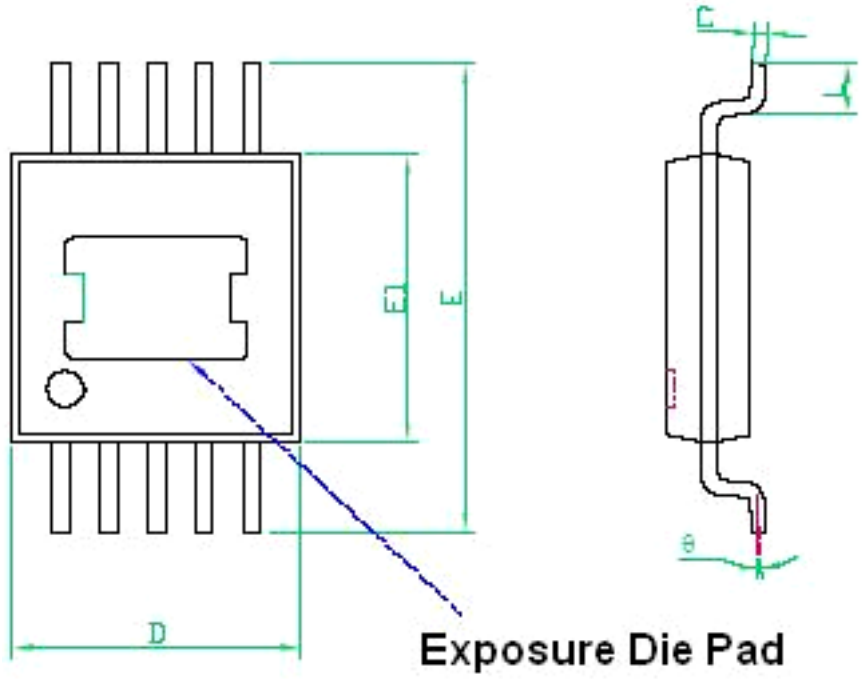
Layout consideration

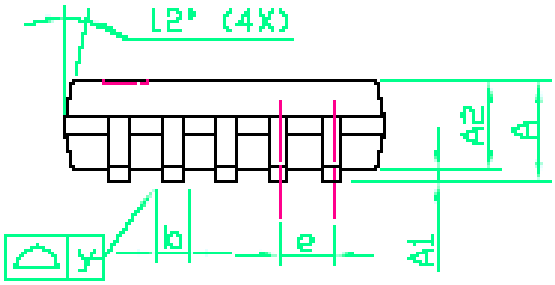
The input bypass capacitor C2must be placed close to the IC. This will reduce copper trace resistance which effect input voltage ripple of the IC.

The capacitor, C1, should also be placed close to the transformer T1. The copper trace connections for the C1, T1, and the YB7002 should be kept short as possible to eliminate over-voltage condition on SW pin due to leakage inductance of T1.

For improved thermal performance can increase the top side copper to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane located underneath the package will help.

Package Information





SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.76	0.86	1.07	0.030	0.034	0.042
A1	0.000	——	0.100	0.000	——	0.004
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	——	0.50	——	——	0.0197	——
L	0.40	0.53	0.66	0.016	0.021	0.026
y	——	——	0.10	——	——	0.004
θ	0°	——	6°	0°	——	6°
L1	0.85	0.95	1.05	0.033	0.037	0.041

Figure4：MSOP10