OVERVIEW

The SM6801A is an analog-input, class-D mono amplifier. Class-D operation provides high efficiency and low power consumption. The device also incorporates an original real-time operation dynamic range compression function that effectively suppresses the distortion in the saturation level region output by soft-clipping, boosting the average sound pressure from the speaker during playback. It also incorporates an input equalizer pin for output speaker frequency characteristics adjustment. These features make the device ideal for use in mobile telephones and speaker applications requiring miniaturization and high-efficiency. The output stage has a BTL output configuration where the output waveform inverts only the modulation components, enabling direct drive connection, without using an LC filter, to a dynamic speaker. The device is available in miniature 16-pin QFN packages, and requires only a peripheral chip capacitor to form a miniature amplifier circuit.

FEATURES

- Operating supply voltage
  - V_{DDS} = 2.0 to 3.6V (input, logic)
  - V_{DDP} = 2.0 to 5.5V (output)
- Low current consumption: 4.2mA (V_{DD} = 3.6V)
  1.6mA (V_{DD} = 2.4V)
- Output power: 0.7W (V_{DD} = 3.6V, 8Ω load)
  0.28W (V_{DD} = 2.4V, 8Ω load)
- Output fundamental frequency: 125kHz
- Gain
  - 6dB (Normal)
  - 15dB to 6dB automatic adjustment in response to the input level
    (Dynamic range compression mode)
- Silicon-gate CMOS process
- Package: 16-pin QFN

APPLICATIONS

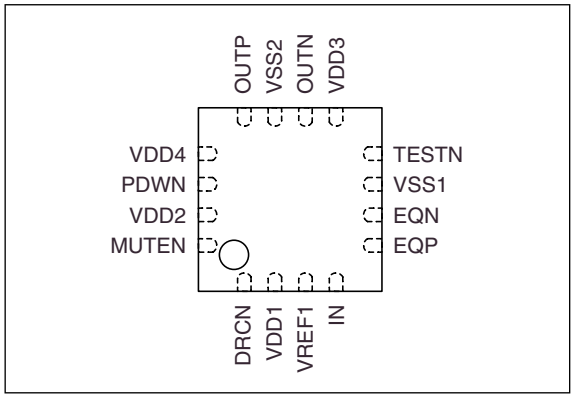
- Cellular phone
- PDA
- Digital still camera

ORDERING INFORMATION

Device	Package
SM6801AB	16-pin QFN

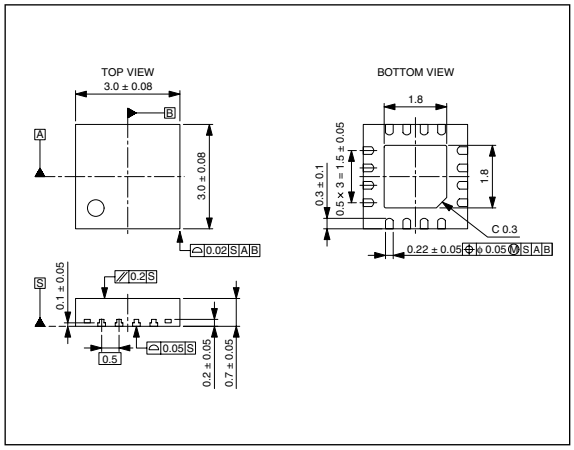
PINOUT

(Top view)

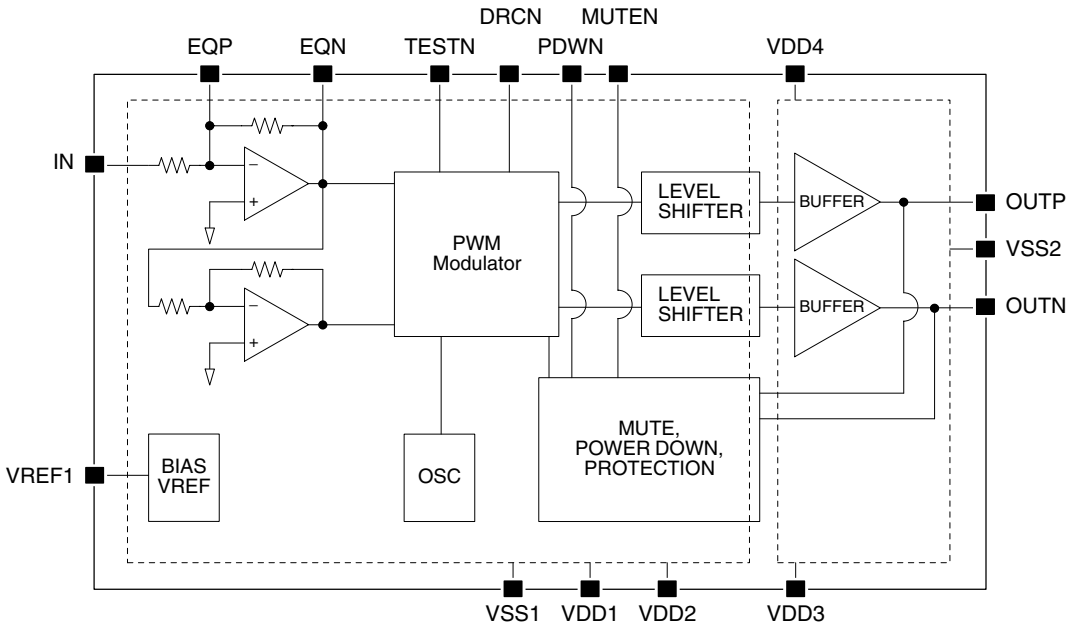


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name*1	I/O*2	Function
1	DRCN	I	Dynamic range compression mode setting (HIGH: normal operation, LOW: DRC mode)
2	VDD1	–	Supply (input system)
3	VREF1	–	Reference voltage 1 (bias voltage)
4	IN	I	Signal input
5	EQP	I	Equalizer network connection
6	EQN	I	Equalizer network connection
7	VSS1	–	Ground (input system)
8	TESTN	Ip	Test pin (HIGH: normal operation, LOW: test mode)
9	VDD3	I	Supply (OUTN stage)
10	OUTN	O	Speaker minus (–) output
11	VSS2	–	Ground (output stage)
12	OUTP	O	Speaker plus (+) output
13	VDD4	–	Supply (OUTP stage)
14	PDWN	I	Power-down control (active LOW)
15	VDD2	–	Supply (logic system)
16	MUTEN	I	Mute control (active LOW)

*1. V_{DDS} = VDD1, VDD2, V_{DDP} = VDD3, VDD4, V_{SS} = VSS1, VSS2
*2. Ip = input pin with built-in pull-up resistor

SPECIFICATIONS

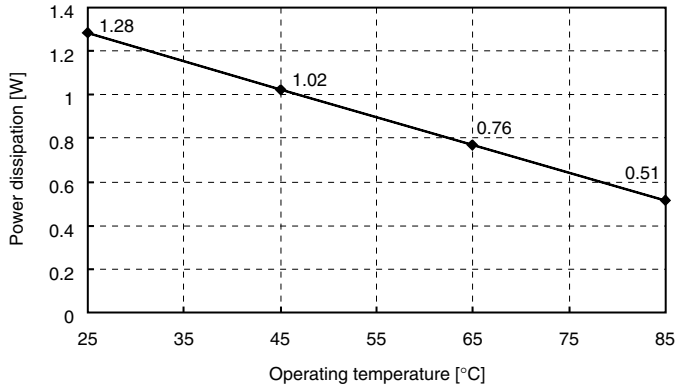
Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DDS}	–0.3 to 4.6	V
	V_{DDP}	–0.3 to 7.0	V
	V_{SS}	0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DDS} + 0.3	V
Storage temperature range	T_{STG}	–55 to 125	°C
Output current	I_O	300	mA
Power dissipation	P_D	1280 (Ta = 25°C)*1	mW

*1. When mounted on a 3.5cm × 3.5cm board, the power dissipation is related to the operating temperature by the following equation.

- Maximum junction temperature: T_{MAX} = 125°C
- Operating ambient temperature: Ta = [°C]
- Thermal resistance: θ_J = 78.0°C/W

$$P_D = \frac{(T_{MAX} - Ta)}{\theta_J}$$



Recommended Operating Conditions

V_{SS} = VSS1 = VSS2 = 0V, V_{DDS} = VDD1 = VDD2, V_{DDP} = VDD3 = VDD4 unless otherwise noted.

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DDS}	2.0 to 3.6	V
Supply voltage 2	V_{DDP}	2.0 to 5.5	V
Supply voltage difference	$V_{DD3} - V_{DD4}$	± 0.1	V
Operating ambient temperature	Ta	–40 to 85	°C

Note. $V_{DDP} \geq V_{DDS}$
V_{DDS} and V_{DDP} should be applied simultaneously.

Electrical Characteristics

DC Characteristics

Standard voltage

VSS1 = VSS2 = 0V, VDD1 = VDD2 = 2.7 to 3.6V, VDD3 = VDD4 = 2.7 to 5.5V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Pin	Symbol	Conditions		Rating min	Rating typ	Rating max	Unit
Current consumption	VDD1	I_{DD1A}	(Note 1)		–	3.8	6.0	mA
		I_{DD1S}	(Note 2)		–	0.1	0.5	µA
	VDD2	I_{DDAA}	(Note 1)	VDD3 = VDD4 = 3.6V	–	0.3	1.5	mA
				VDD3 = VDD4 = 5V	–	1.0	6.0	mA
		I_{DDAS}	(Note 2)	VDD3 = VDD4 = 3.6V	–	0.1	0.3	µA
				VDD3 = VDD4 = 5V	–	0.1	0.3	µA
Input voltage 1	TESTN, DRCN	V_{IH1}	HIGH level		$0.7V_{DD1}$	–	–	V
		V_{IL1}	LOW level		–	–	$0.3V_{DD1}$	V
Input voltage 2	MUTEN, PDWN	V_{IH2}	HIGH level		1.6	–	–	V
		V_{IL2}	LOW level		–	–	0.4	V
Input current 1	TESTN, DRCN, MUTEN, PDWN	I_{IL1}	$V_{IN} = V_{SS}$		–	–	90	µA
Input current 2		I_{LH1}	$V_{IN} = V_{DDS}$		–	–	1.0	µA

Note 1. MUTEN = HIGH, PDWN = HIGH, input and VREF1 connected by 600Ω, DRCN = HIGH, no-load output
Note 2. MUTEN = LOW, PDWN = LOW, input and VREF1 connected by 600Ω, DRCN = HIGH, no-load output

Low voltage

VSS1 = VSS2 = 0V, VDD1 = VDD2 = VDD3 = VDD4 = 2.0 to 3.2V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Pin	Symbol	Conditions	Rating min	Rating typ	Rating max	Unit
Current consumption	VDD1	I_{DD1A}	(Note 1)	–	1.6	6.0	mA
		I_{DD1S}	(Note 2)	–	0.1	0.5	µA
	VDD2	I_{DDAA}	(Note 1)	–	0.2	1.5	mA
		I_{DDAS}	(Note 2)	–	0.1	0.3	µA
Input voltage 1	TESTN, DRCN	V_{IH1}	HIGH level	$0.7V_{DD1}$	–	–	V
		V_{IL1}	LOW level	–	–	$0.3V_{DD1}$	V
Input voltage 2	MUTEN, PDWN	V_{IH2}	HIGH level	1.6	–	–	V
		V_{IL2}	LOW level	–	–	0.4	V
Input current 1	TESTN, DRCN, MUTEN, PDWN	I_{IL1}	$V_{IN} = V_{SS}$	–	–	90	µA
Input current 2		I_{LH1}	$V_{IN} = V_{DDS}$	–	–	1.0	µA

Note 1. MUTEN = HIGH, PDWN = HIGH, input and VREF1 connected by 600Ω, DRCN = HIGH, no-load output
Note 2. MUTEN = LOW, PDWN = LOW, input and VREF1 connected by 600Ω, DRCN = HIGH, no-load output

Note. The usage with direct coupling to load is recommended for operating VDD1, VDD2, VDD3 and VDD4 at ≤ 2.4V. When using LC-type LPF, the ringing phenomena due to rush current may be judged as short-circuit of the load. In this case, the normal operation will start after the mute for 5 seconds.

AC Analog Characteristics

VDD1 = VDD2 = VDD3 = VDD4 = 3.6V, VSS1 = VSS2 = 0V, 0.708Vrms analog input amplitude, 1kHz input signal frequency, Ta = 25°C, "Measurement Block Diagram", "Measurement Conditions", "Measurement Circuit", DRCN = PDWN = MUTEN = HIGH, unless otherwise noted.

Analog Input Characteristics (IN)

Standard voltage: VDD1 = VDD2 = VDD3 = VDD4 = 3.6V, VSS1 = VSS2 = 0V

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Reference input amplitude 1	V_{AI1}	P_O = 0.25W	–	0.708	–	Vrms
Reference input amplitude 2	V_{AI2}	P_O = 0.05W	–	0.178	–	Vrms
Input resistance	R_{IN}		40	60	80	kΩ
Input clipping voltage	V_{CLP}	P_O = 0.5W	0.7	1	1.3	Vrms

Low voltage: VDD1 = VDD2 = VDD3 = VDD4 = 2.4V, VSS1 = VSS2 = 0V

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Reference input amplitude 1	V_{AI1}	P_O = 42mW	–	0.316	–	Vrms
Reference input amplitude 2	V_{AI2}	P_O = 8mW	–	0.045	–	Vrms
Input resistance	R_{IN}		40	60	80	kΩ
Input clipping voltage	V_{CLP}	P_O = 100mW	0.38	0.48	0.58	Vrms

Analog Output Characteristics (OUTP, OUTN)

Standard voltage: VDD1 = VDD2 = VDD3 = VDD4 = 3.6V, VSS1 = VSS2 = 0V

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Voltage gain 1	A_1	DRCN = HIGH, input amplitude = 0.1Vrms	4.0	6.0	8.0	dB
Voltage gain 2	A_2	DRCN = LOW, input amplitude = 0.05Vrms	13.0	15.0	17.0	dB
Residual noise voltage	V_{NS}	DRCN = HIGH, input and VREF1 connected by 600Ω	–	78	120	μVrms
Total harmonic distortion + noise	THD + N	P_O = 0.25W, reference input amplitude 1	–	0.4	1.0	%
Maximum output power	P_{OMAX}	Output power when THD = 10%	0.6	0.7	0.8	W
Mute-mode output voltage	V_{MUTE}	Output power when MUTEN = LOW	–90.0	–110	–	dBV
HIGH-level output voltage	V_{OH}		V_{DDP} – 0.2	V_{DDP} – 0.02	V_{DDP} + 0.2	V
LOW-level output voltage	V_{OL}		0	0.02	0.2	V
Efficiency	E_{EF}	Maximum output power conditions	80	83	–	%
Ripple rejection ratio 1	PSRR1	(Note 1)	–	–60	–	dB

Note 1. DRCN = HIGH, 217Hz ripple frequency, 0.2Vrms ripple amplitude on VDD1/VDD2/VDD3/VDD4, input and VREF1 connected by 600Ω.

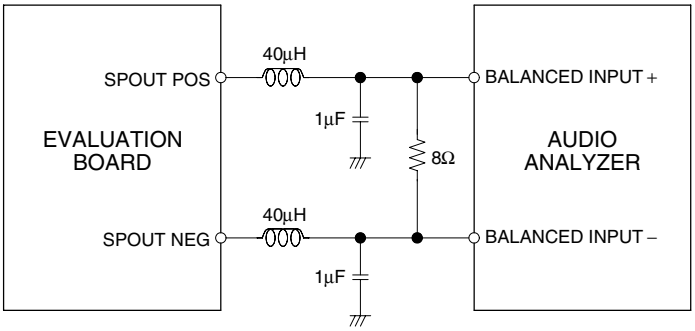
Low voltage: VDD1 = VDD2 = VDD3 = VDD4 = 2.4V, VSS1 = VSS2 = 0V

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Voltage gain 1	A_1	DRCN = HIGH, input amplitude = 0.1Vrms	–	5.6	–	dB
Voltage gain 2	A_2	DRCN = LOW, input amplitude = 0.05Vrms	–	14.5	–	dB
Residual noise voltage	V_{NS}	DRCN = HIGH, input and VREF1 connected by 600Ω	–	120	–	μVrms
Total harmonic distortion + noise	THD + N	P_O = 42mW, reference input amplitude V = 316.2mVrms	–	0.8	–	%
Maximum output power	P_{OMAX}	Output power when THD = 10%	–	0.280	–	W
Mute-mode output voltage	V_{MUTE}	Output power when MUTEN = LOW	–	–110	–	dBV
HIGH-level output voltage	V_{OH}		–	V_{DDP} – 0.02	–	V
LOW-level output voltage	V_{OL}		–	0.02	–	V

Reference Voltage Characteristics (VREF1)

Parameter	Symbol	Rating			Unit
		min	typ	max	
Reference output voltage 1	V_{REF1}	$0.45V_{DDS}$	$0.5V_{DDS}$	$0.55V_{DDS}$	V

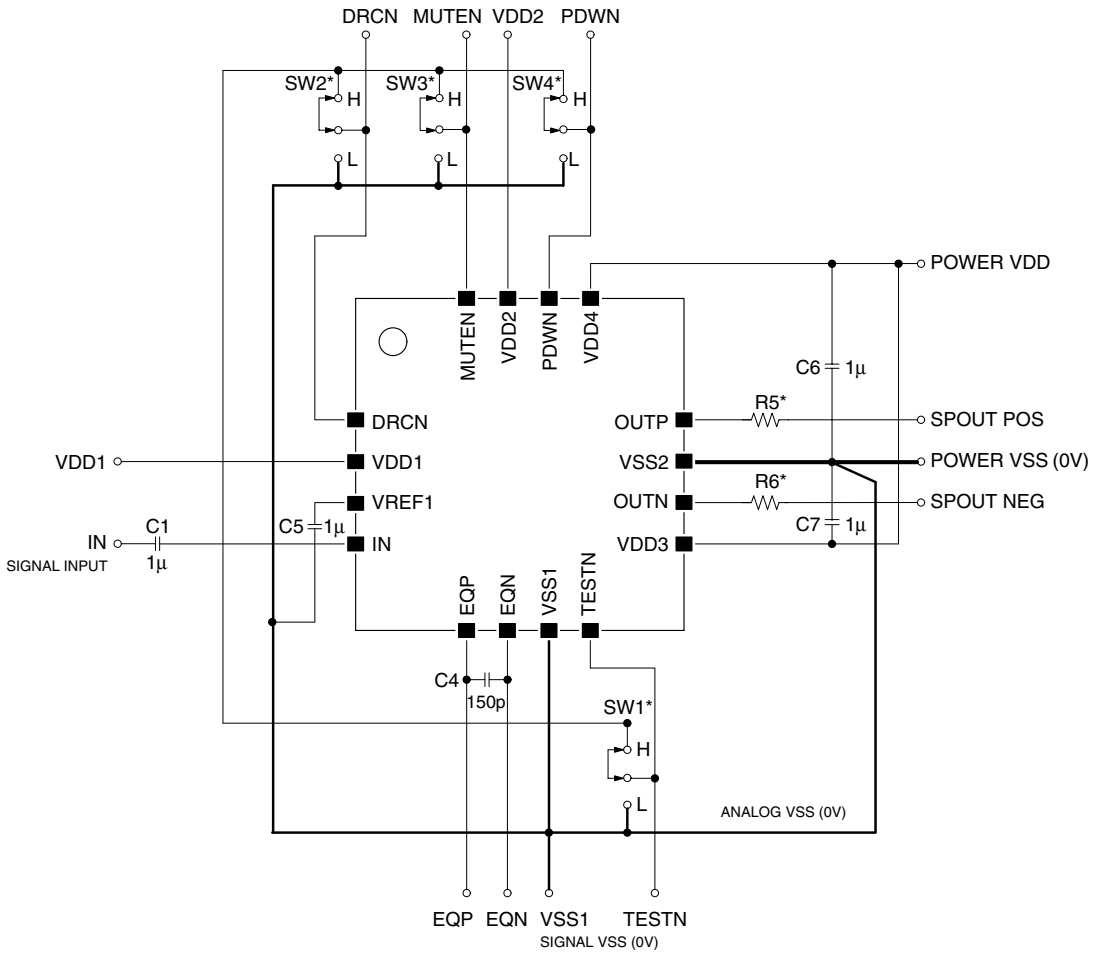
Measurement Block Diagram



Measurement Conditions

Parameter	Audio Analyzer (Audio Precision System Two Cascade) Built-in Filters
Excluding residual noise	Low-pass filter (20kHz) ON High-pass filter (22Hz) ON
Residual noise voltage	Low-pass filter (20kHz) ON High-pass filter (22Hz) ON A-weighted

Measurement Circuit



Note. *C2, C3: not inserted
*R1, R2, R3, R4: not inserted
*R5, R6: series resistors for dielectric speaker
*SW1: HIGH = Normal, LOW = Test
*SW2: LOW = DRC on, HIGH = DRC off
*SW3: LOW = Mute on, HIGH = Mute off
*SW4: LOW = Power off, HIGH = Power on

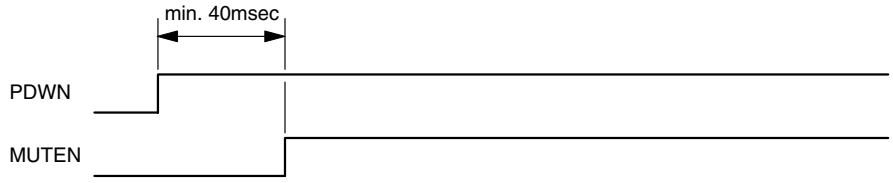
FUNCTIONAL DESCRIPTION

Power-down (PDWN)

The device enters power-down mode when PDWN goes LOW. When powered-down, the outputs become high impedance and the internal oscillation stops. In power-down mode, the MUTEN pin should be held LOW.

Mute (MUTEN)

Mute operation occurs when MUTEN goes LOW. In mute mode, the outputs become high impedance. During mute operation, the protection circuit operation is disabled, but the outputs are protected against output short circuits by their high impedance state. When power is applied, MUTEN should be held LOW for a short interval, shown in the timing diagram below, to prevent pop noise from the speaker. Also, applying and releasing mute operation after power is applied can occur at high speed without generating pop noise.



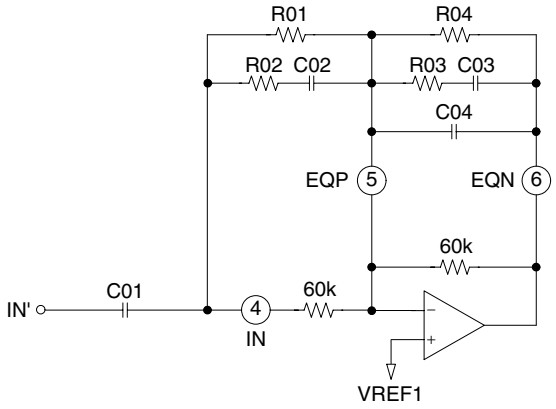
Note. VREF1 load capacitance = 1µF

Protection Circuit

The protection circuit operates if there is an output short-circuit to the supply, short-circuit to ground, or other excessive load abnormal condition lasting longer than approximately 1µs. Normal operation resumes after approximately 5 seconds. When the protection circuit becomes active, the outputs become high impedance. The usage with direct coupling to load is recommended for operating VDD1, VDD2, VDD3 and VDD4 at ≤ 2.4V. When using LC-type LPF, the ringing phenomena due to rush current may be judged as short-circuit of the load. In this case, the normal operation will start after the mute for 5 seconds.

Input Equalizer (IN, EQP, EQN)

An input equalizer network can be connected to pins IN, EQP and EQN, as shown in the input equivalent circuit and equalizer circuit below.

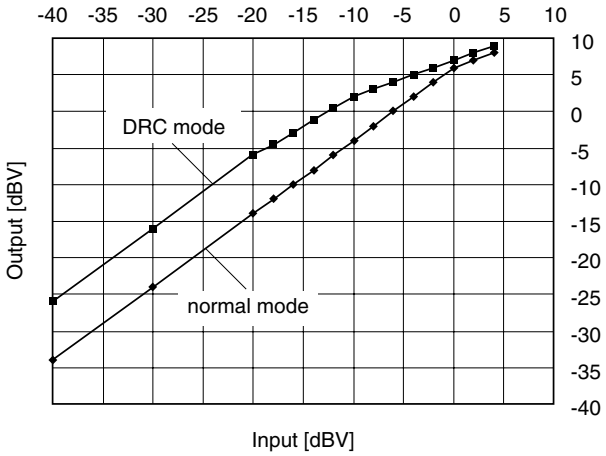


The frequency response of the equalizer circuit is given by the following equation, where f is the frequency.

$$\text{Response} = 20 \times \log_{10} \left[\frac{\dfrac{1}{\dfrac{1}{60000} + \dfrac{1}{\text{R03} + \dfrac{1}{2\pi f \text{C03}}} + \dfrac{1}{\text{R04}} + 2\pi f \text{C04}}}{\dfrac{1}{2\pi f \text{C01}} + \dfrac{1}{\dfrac{1}{60000} + \dfrac{1}{\text{R01}} + \dfrac{1}{\text{R02} + \dfrac{1}{2\pi f \text{C02}}}}} \right] \text{[dB]}$$

Dynamic Range Compression Mode (DRCN)

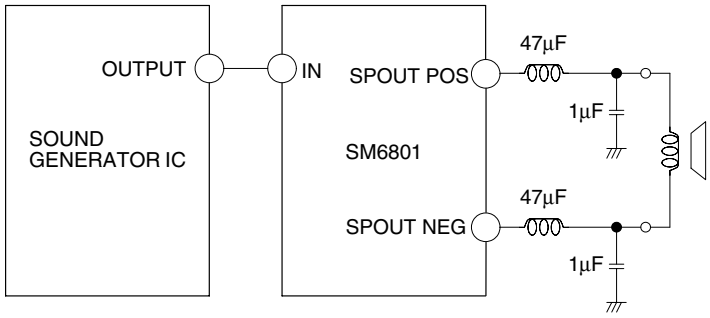
The dynamic range compression mode is set when DRCN is LOW. When a compression mode is used, the gain for small input signals is increased while large input signals are converted using a curve that performs soft-clipping. This increases the average sound pressure level emitted from the speaker during playback.



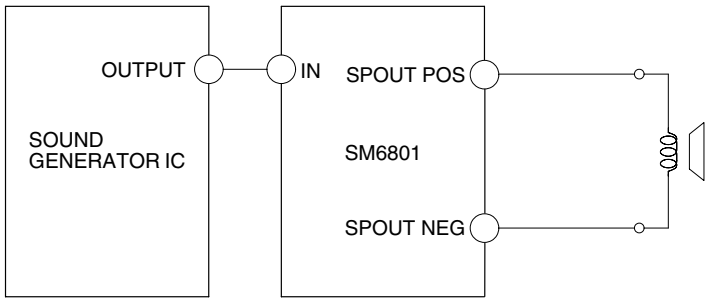
TYPICAL APPLICATION CIRCUITS

Dynamic Speaker

LC-type LPF Connection

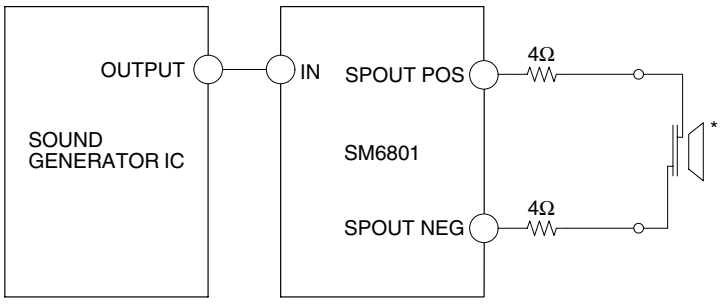


Direct Connection



Dielectric Speaker

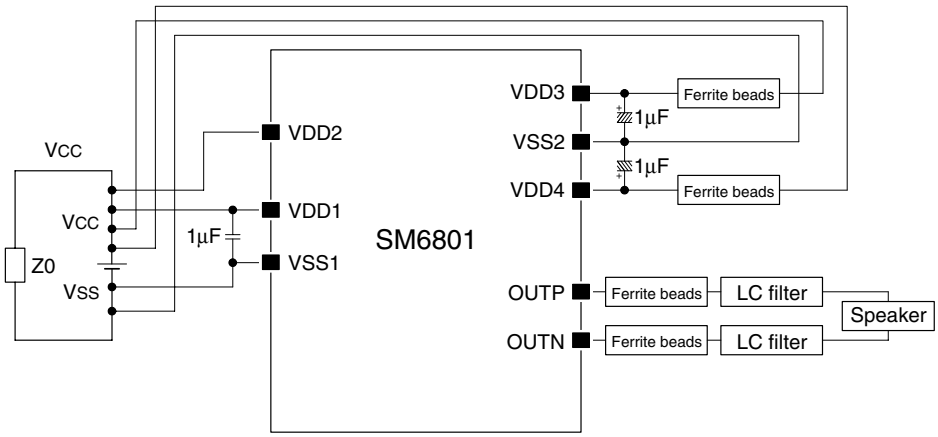
A dielectric speaker is capacitive in nature, and therefore requires output resistor connection.



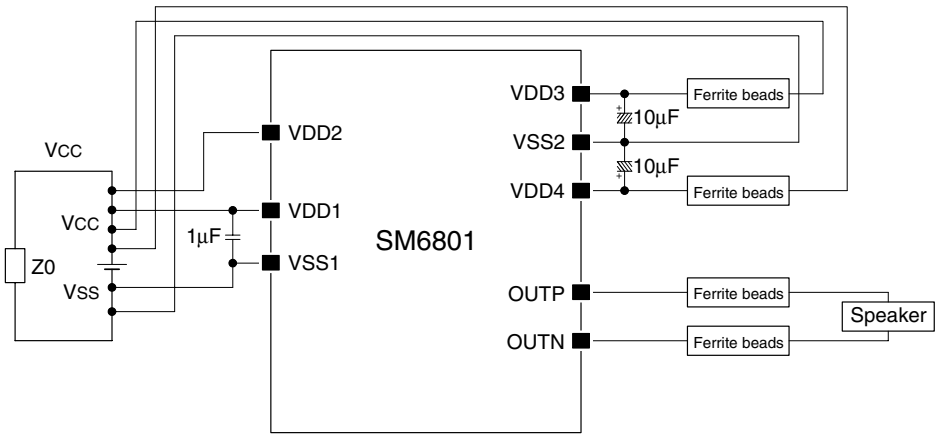
* Dielectric speaker
Taiyo Yuden MLS20070, MLS23070, MLS25070 or similar

Mounting Circuits

Connection to LC Filter



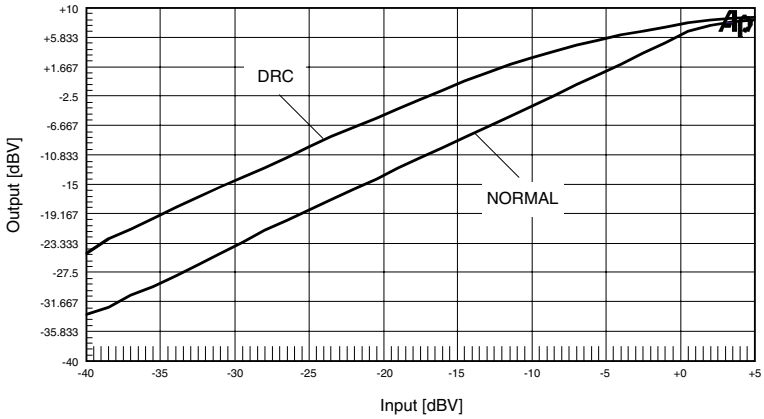
Direct Connection to Load



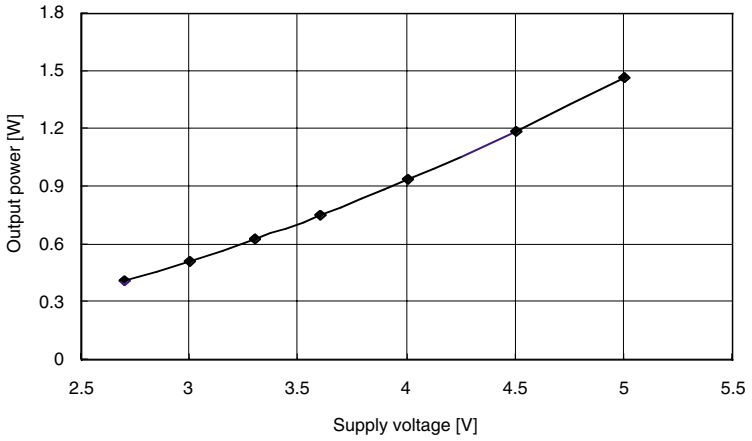
Note. As for the wiring to VDD1, VDD2, VDD3, VDD4, VSS1, and VSS2, we recommend to wire from the power supply block. The recommended value of internal impedance (Z0) is approximately less than 1/40 of load resistance.

TYPICAL CHARACTERISTICS

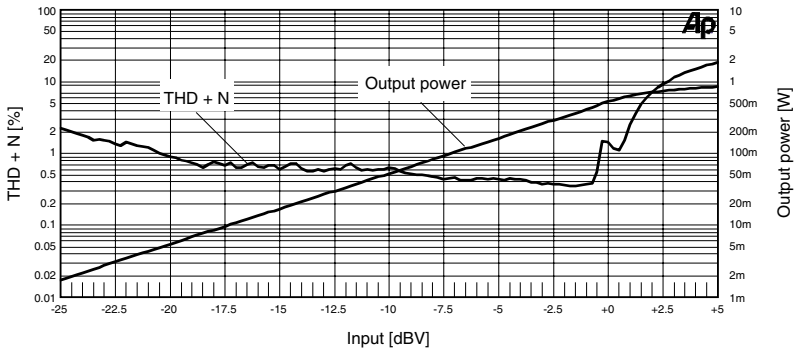
Measurement conditions: Refer to “Analog Output Characteristics”.
Measurement circuit: Refer to “Measurement Circuit”.



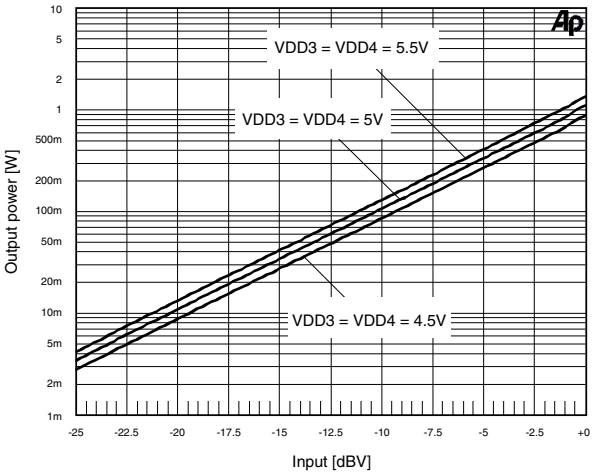
Input vs. Output



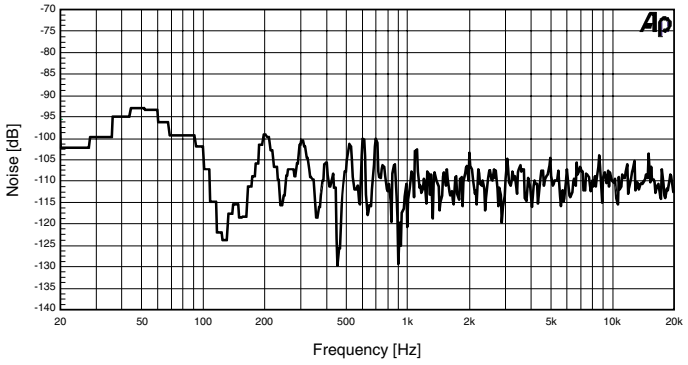
Supply voltage vs. Output power



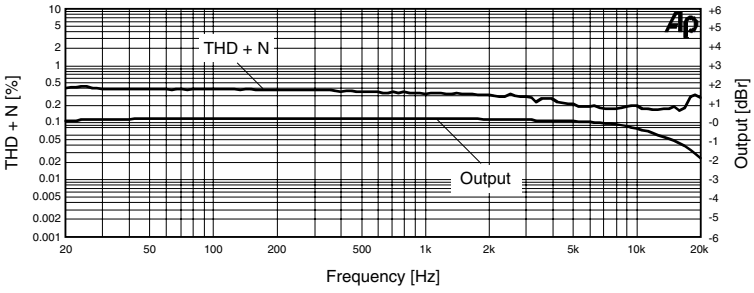
Input vs. THD + N and output power



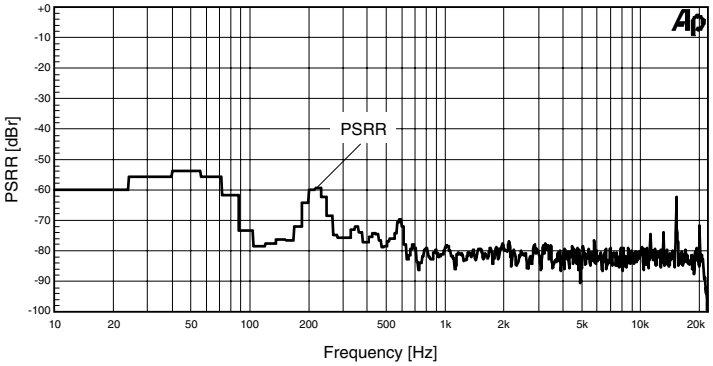
Input power vs. Output power



Residual noise vs. Frequency

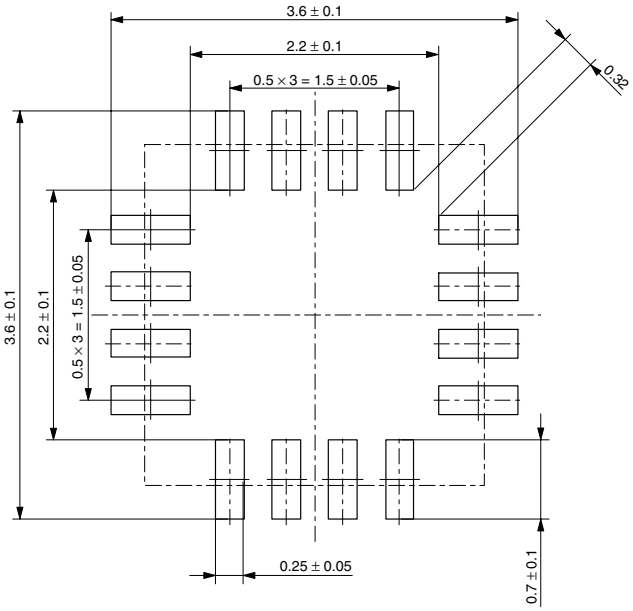


THD + N and output voltage vs. Frequency



PSRR vs. Frequency

FOOTPRINT PATTERN



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