MGCR01

Dual Mode IF Receiver for TDMA/AMPS and CDMA/AMPS

Datasheet

DS4721 ISSUE 4.4 November 2001

Ordering Information

MGCR01/KG/QP1S
MGCR01/KG/QP1T

Features

- Dual IF Inputs 50 to 250 MHz
- 90dB AGC Gain Control
- IQ demodulator
- On chip oscillator provides high accuracy quadrature LO generation
- Optional IF Output
- 3 Volt Power Supply
- 28 lead QSOP Package

Description

The MGCR01 is designed for use in dual mode mobile phones (TDMA/AMPS and CDMA/AMPS). The circuit provides IF amplification with gain control and differential I and Q baseband outputs. The MGCR01 interfaces directly with MGCM01 for TDMA/AMPS (using 60kHz low IF) and MGCM03 or MGCM04 for CDMA and AMPS applications. The on chip oscillator and prescaler are also compatible with the PLL synthesisers on these devices.

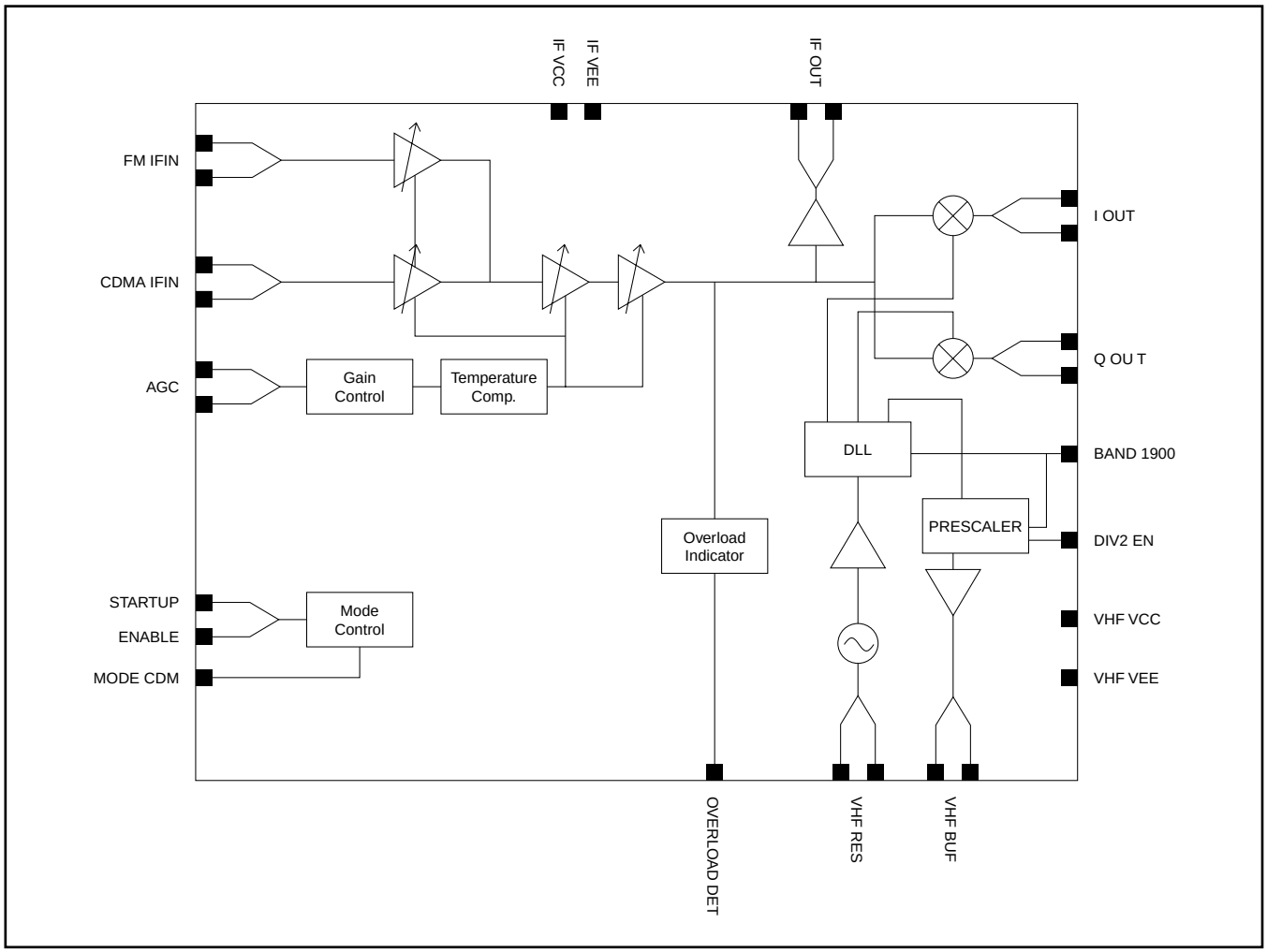


Figure 1 - Block Diagram

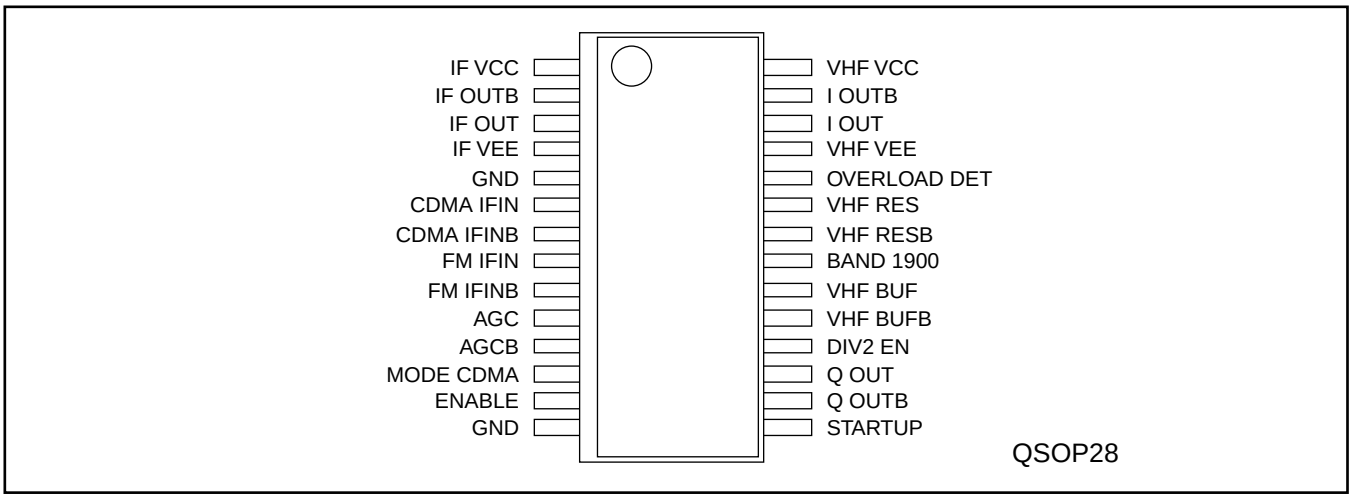


Figure 2 - Pin Connections

Pin No.	Pin Name	Description
1	IF VCC	Supply for IF inputs and AGC blocks
2	IF OUTB	IF ouput
3	IF OUT	IF output
4	IF VEE	Ground for IF inputs and AGC blocks
5	GND	Substrate ground
6	CDMA IFIN	IF input (CDMA)
7	CDMA IFINB	IF input (CDMA)
8	FM IFIIN	IF input (FM)
9	FM IFINB	IF inputs (FM) (AC ground)
10	AGC	AGC Control for IF section
11	AGCB	AGC control for IF sections (AC ground)
12	MODE CDMA	CDMA/FM input select
13	ENABLE	Power up AGC sections of device
14	GND	Substrate Ground
15	STARTUP	Power up Oscillator, DLL and Mixer
16	QOUTB	Q channel baseband output
17	QOUT	Q channel baseband output
18	GND	Ground
19	VHF BUFB	VHF oscillator buffered output for synthesiser
20	VHF BUF	VHF oscillator buffered output for synthesiser
21	BAND 1900	VHF oscillator mode (see table 1)
22	VHF RESB	VHF VCO resonator
23	VHF RES	VHF VCO resonator
24	OVERLOAD DET	Overload detector output
25	VHF VEE	Ground for VHF VCO and DLL blocks
26	I OUT	I channel baseband output
27	I OUTB	I channel baseband output
28	VHF VCC	Supply for VHF and DLL blocks

Table 1 - Pin Description

X = Don't Care

Description	ENABLE	STARTUP	MODE CDMA	BAND 1900	Conditions
Standby Mode	0	0	X	X	All circuits powered down except logic inputs
Start up Mode	0	1	X	1	For high band IF
	0	1	X	0	For low band IF
					Turns on VCO circuits, DLL quadrature generation, prescaler and IQ demodulator. All other circuits remain powered down
CDMA mode	1	1	1	1	For high band IF
	1	1	1	0	For low band IF
					All circuits operational except for IF output buffer, CDMA input stage selected.
FM Mode	1	1	0	0	All circuits operational except for IF output buffer, FM input stage selected.
Alternative FM mode	1	1	0	1	Note 4
CDMA IF AGC only mode	1	0	1	X	Demodulator and LO generation circuitry powered down. IF output buffer enabled
FM IF AGC	1	0	0	X	Demodulator and LO generation circuitry powered down. IF output buffer enabled.

Table 2 - Electrical Characteristics (Mode Control)

Notes:

1. STARTUP mode is provided to allow VCO/DLL/prescalers to stabilise before signal path is activated. This is a power-saving feature since the signal path is redundant during this period. If this feature is not required, the ENABLE and STARTUP control pins can be shorted together so that all circuitry is activated at the same time.

2. In high band mode (Band 1900 = 1) the VCO operates at twice the IF frequency. For example if IF = 210.38MHz then the oscillator operates at 420.76MHz. A delay locked loop (DLL) circuit then generates the quadrature LO signals.

3. In low band mode (Band 1900 = 0) the VCO operates at 4 times the IF frequency. for example if IF = 85.38MHz the oscillator operates at 341.52MHz. This is then divided and uses DLL circuit to provide the quadrature LO signals.

4. This mode can be used for FM. The VCO operates at twice the LO frequency. This mode is not normally used as a large tuning range is required on the VCO.

DLL and Prescaler divide ratios

The BAND 1900 and DIV2 EN inputs allow the overall divide ratio to control the total divide ratio in MGCR01 as shown in the following table.

BAND 1900	DIV2 EN	DLL Divide Ratio	Prescaler Divide Ratio	Total Divide Ratio
1	1	2	2	4
0	1	4	2	8
1	0	2	4	8
0	0	4	2	8

Table 3 - Prescaler Ratios

Notes:
if DIV2 EN is set low then the total divider ratio is always 8.

If DIV2 EN is set high then the prescaler divide ratio is always 2. For example with BAND 1900 high and if the oscillator frequency is 300MHz, then the DLL output (the mixer LO frequency) will be 150MHz and the prescaler output will be 75MHz.

Description	Min	Typ	Max	Units	Comments
Supply Voltage			4.0	Volts	
Operation temperature, Tamb	-30		+100	°C	Ambient temperature
Storage temperature, Tstg	-40		+125	°C	
Junction temperature, Tj			+150	°C	
Power dissipation			350	mW	
Maximum Pin Voltage			Vcc+0.6	Volts	All pins except Vcc and GND
Minimum Pin Voltage	-0.6			Volts	All pins except Vcc and GND
ESD voltage	1.75			kV	Human Body Metal

Table 4 - Absolute Maximum Ratings

Electrostatic handling precautions must be applied.

T_{amb}= 30°C to +70°C, V_{CC} = +2.7 to +3.6. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
General					
Supply Voltage	2.7	3.0	3.6	V	All V_{CC} Pins
Operating Temperature	-30	27	85	°C	Ambient See note 1
Current Consumption					
Standby Mode		0.03	0.1	mA	
Startup Mode		8	13	mA	
CDMA Mode		14	23	mA	
FM Mode		14	23	mA	
CDMA AGC only Mode		8	13	mA	
FM AGC only Mode		11	18	mA	
Mode Control Logic					
CMOS input logic high, VIH	V_{CC}-0.5		V_{CC}+0.1	V	All logic inputs
CMOS input high current, IIH	-10		10	µA	All logic inputs
CMOS input low current, IIL	-10		10	µA	All logic inputs
Switching time between any two modes		3		ms	
AGC Control	0.1		2.6	V	
AGC Input impedance	100	130	160	kΩ	
DC Common Mode voltages					
I OUT, I OUTB (CDMA Mode) I OUTB, QOUTB	V_{CC}-0.8	V_{CC}-0.6	V_{CC}-0.4	V	
I OUT<Q OUT (FM Mode) I OUTB, Q OUTB	V_{CC}-0.8	V_{CC}-0.6	V_{CC}-0.4	V	

Table 5 - Electrical Characteristics (DC specifications)

Notes:

1. Specifications are guaranteed over -30 to + 70°C, however operation is guaranteed over the extended range of -30 to +85°C with minimal variation in specified parameters.

T_{amb}= 30°C to +70°C, V_{CC} = +2.7 to +3.6. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Frequency = 210.38MHz

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
CDMA					
Max Voltage Gain to demodulator output	46	48		dB	AGC = 2.6v
Min Voltage Gain to demodulator output		-55	-47	dB	AGC = 0.1V
Max Voltage Gain to IF buffer output	38	41		dB	IF mode
Min Voltage Gain to IF buffer output		-51	-49	dB	IF mode
AGC control Max	2.6			V	Gain = Max
AGC control Min			0.1	V	Gain = Min
Gain slope		40		dB/V	
Gain slope linearity	6		90	dB/V	Over gain control range
Gain temperature stability	-2		2	dB	
Channel gain variation @ 210.38MHz	-0.1		0.1	dB	Within channel bandwidth (1.25MHz)
$NF_{Gainmax}$		5.5	6.5	dB	Rs (500Ω)
Input $V1dB_{Gainmin}$	104 -13	110 -7		dBµV dBm	Minimum gain Power (500Ω)
$IIP3_{Gainmax}$	69 -48			dBµV dBm	Max gain Power (500Ω)
Input impedance		500		Ω	With addition of external resistor across IF inputs
IF Frequency	50		250	MHz	
CDMA to Amps isolation	30			dB	

Table 5 - Electrical Characteristics (DC specifications) - Continued

T_{amb}= 30°C to +70°C, V_{CC} = +2.7 to +3.6. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Frequency = 85.38MHz

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
FM AGC					
Max Voltage Gain to demodulator output	50	54		dB	To demodulator outputs
Min Voltage Gain to demodulator output		-49	-42	dB	To demodulator
Max Voltage Gain to IF buffer output	49	56		dB	IF AGC only mode
Min Voltage Gain to IF buffer output		-48	-40	dB	IF AGC only mode
AGC control Max	2.6			V	Gain = Gain max
AGC control Min			0.1	V	Gain = Gain min
Gain slope		40		dB/V	
Gain slope linearity	6		80	dB/V	Over gain control range
Gain temperature stability	-2		2	dB	For any gain setting
NFGainmax			6	dB	850Ωsource
Input $V1dB_{Gainmin}$	98	105		dBµV	Minimum gain
	-17	-14		dBm	Power (850Ω)
$IIP3_{Gainmax}$	65			dBµV	Max Gain
	-54			dBm	Power (850Ω)
Input Impedance		850		Ω	With addition of external resistor across IF inputs
IF Frequency	50		250	MHz	
VHF Local Oscillator Quaderature generation					
VCO Frequency	100		500	MHz	Note 2
	100		400	MHz	Note 3
VCO Phase noise		-100	-98	dBc/Hz	@30kHz, Hiband mode Minimum tank Q=15 Note 1
VCO Noise floor			-130	dBc/Hz	@>3MHz, Note 1
VCO buffer output	350			mV	pk-pk single ended
VCO buffer output impedance			100	Ω	Differential

Table 5 - Electrical Characteristics (DC specifications) - Continued

Notes:
1. Phase noise is specified at the LO Input to the mixers.
2. Total divide ratio to prescaler output is 8.
3. Total divide ratio to prescaler ouput is 4. The prescaler output is limited to 100MHz max.

T_{amb}= 30°C to +70°C, V_{CC} = +2.7 to +3.6. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Demodulator Ouput					I OUT, I OUTB, Q OUT, Q OUTB
I/Q Gain matching		0.1	0.25	dB	
I/Q Phase matching		0.5	2	deg	
Output impedance	3	4	5	kΩ	Differential
Baseband Bandwidth		50		MHz	Defined by on-chip first order low-pass filter
Output IP3	117	119		dBµV	
Baseband differential DC offset			3.5	mV	
Overload Detect					Referred to baseband outputs
CDMA		104		dBµV	
FM Mode		106		dBµV	

Table 5 - Electrical Characteristics (DC specifications) - Continued

Additional Information

Typical Performance Characteristics

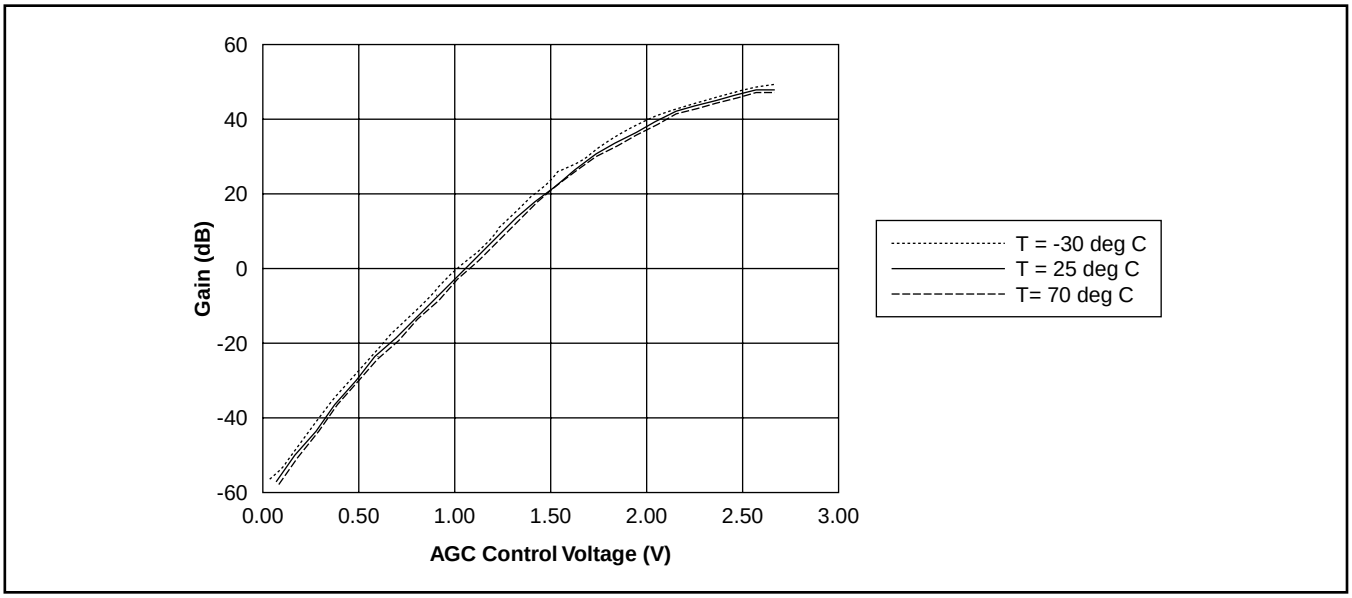


Figure 3 - CDMA Gain v AGC Voltage

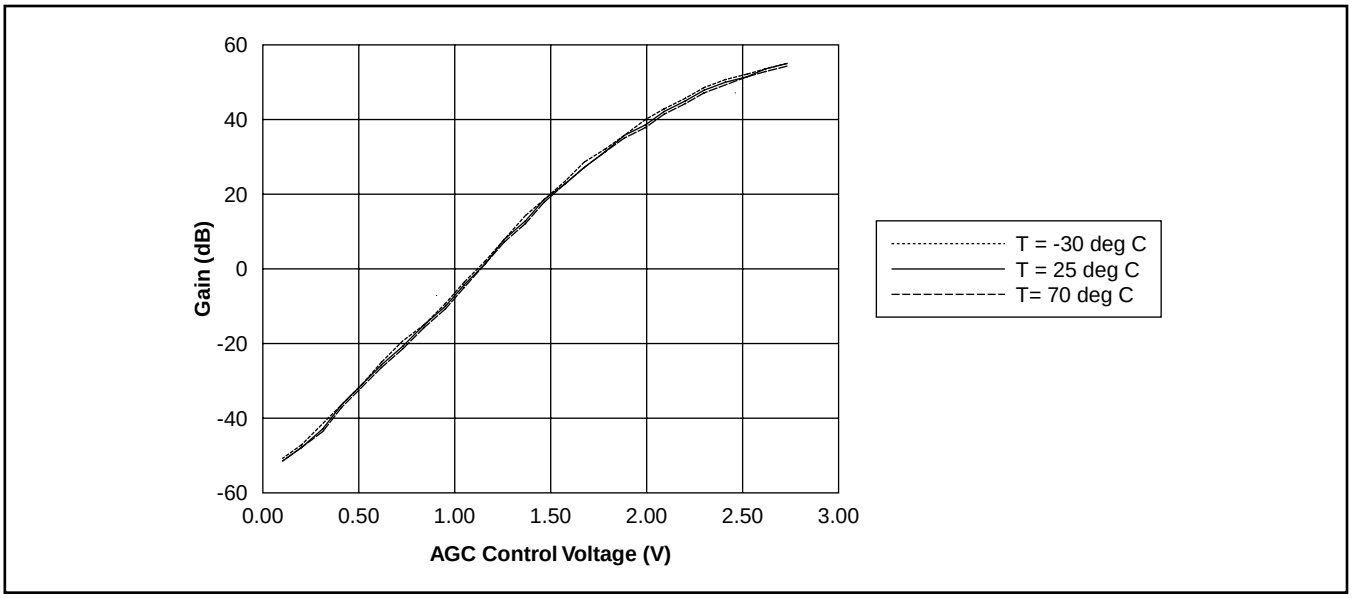


Figure 4 - FM Gain v AGC Voltage

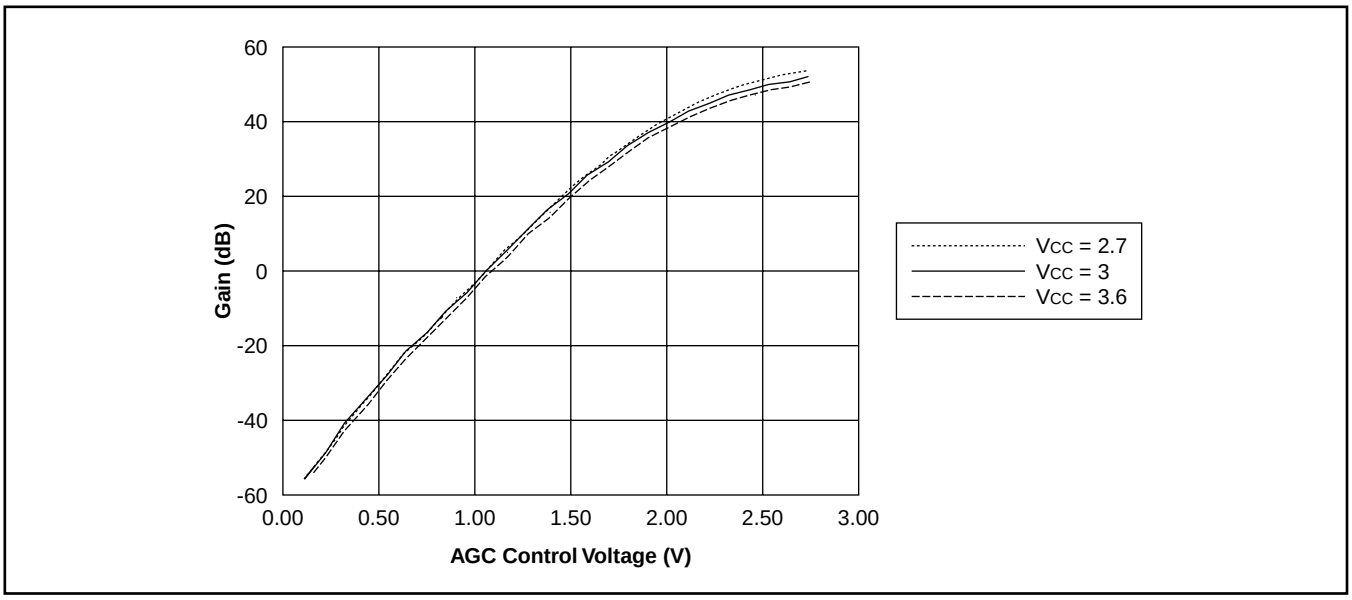


Figure 5 - CDMA Gain v AGC Voltage

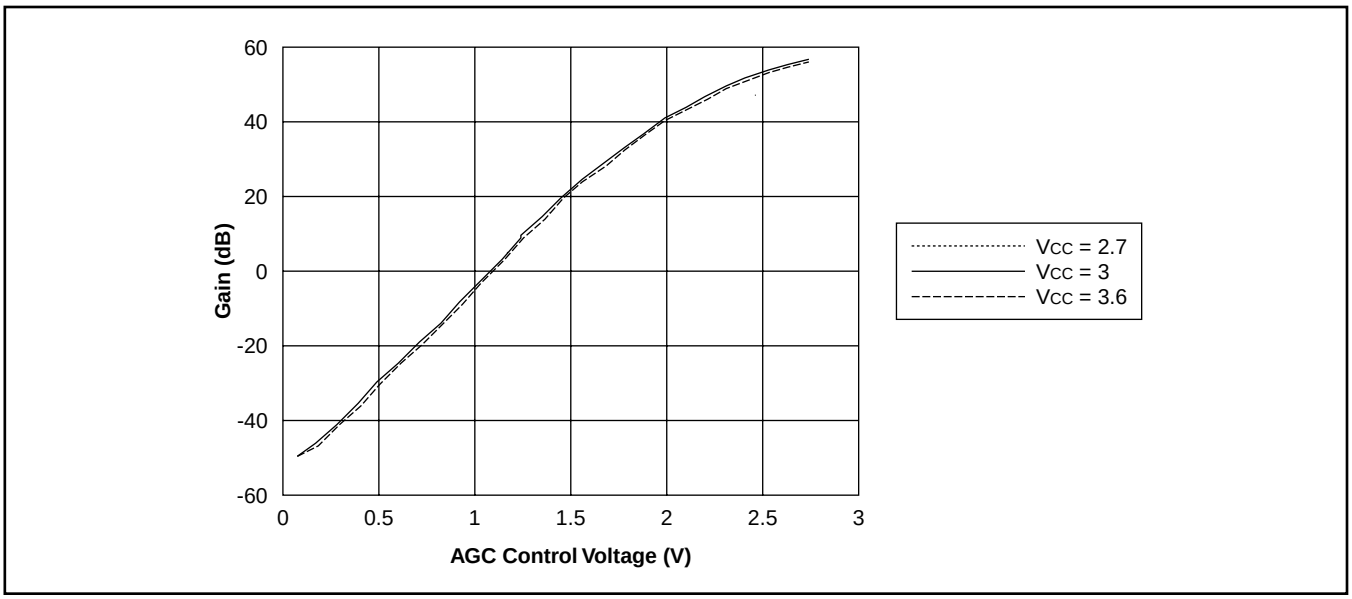
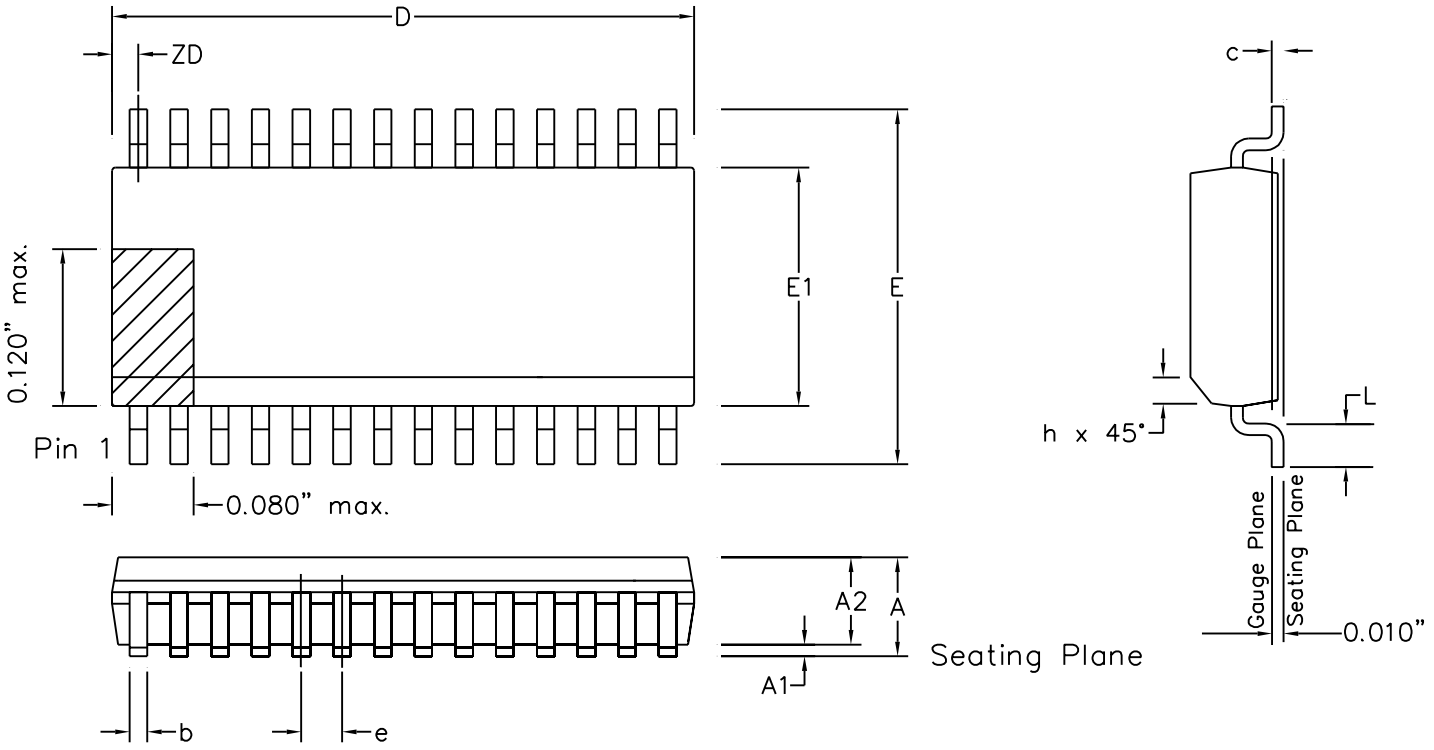


Figure 6 - FM Gain v AGC Voltage



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.386	0.394	9.80	10.01
ZD	0.033 REF.		0.84 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	28			
Conforms to JEDEC MO-137AF Iss. A				

This drawing supersedes
418/ED/51617/004 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
QP / Q

Package Code DG

Package Outline for 28 lead QSOP (0.150" Body Width)

GPD00292

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