

# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## General Description

The MAX3747/MAX3747A/MAX3747B multirate limiting amplifiers function as data quantizers for OC-3 through OC-48 synchronous optical network (SONET), Fibre-Channel, and Gigabit Ethernet optical receivers. They are pin-for-pin compatible with the SY88993V from Micrel Semiconductor, Inc. The amplifiers accept a wide range of input voltages and provide constant-level, current-mode logic (CML) output voltages with controlled edge speeds. The MAX3747 output voltage level is 500mV<sub>P-P</sub> and the MAX3747A/MAX3747B output voltages are 800mV<sub>P-P</sub>. The MAX3747B has enhanced LOS operation under overload conditions.

The MAX3747/MAX3747A/MAX3747B limiting amplifiers feature a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE) that can be combined to implement squelch.

The MAX3747/MAX3747A/MAX3747B are available in a 3mm, 10-pin  $\mu$ MAX<sup>®</sup> package ideal for small form-factor receivers.

## Applications

Gigabit Ethernet SFP/SFF Optical Transceiver Modules  
1G/2G Fibre-Channel SFP/SFF Optical Transceiver Modules  
Multirate OC-3 to OC-48 FEC SFP/SFF Optical Transceiver Modules  
10G LX4 Transceiver Modules

## Features

- ◆ Pin Compatible with Micrel SY88993V
- ◆ 155Mbps to 3.2Gbps Operation
- ◆ > 57dB of Gain
- ◆  $< 10^{-12}$  BER with 2mV<sub>P-P</sub> Input Amplitude
- ◆ 18mA Supply Current
- ◆ Chatter-Free LOS with Programmable Threshold
- ◆ Output DISABLE Function
- ◆ PECL-Compatible Inputs

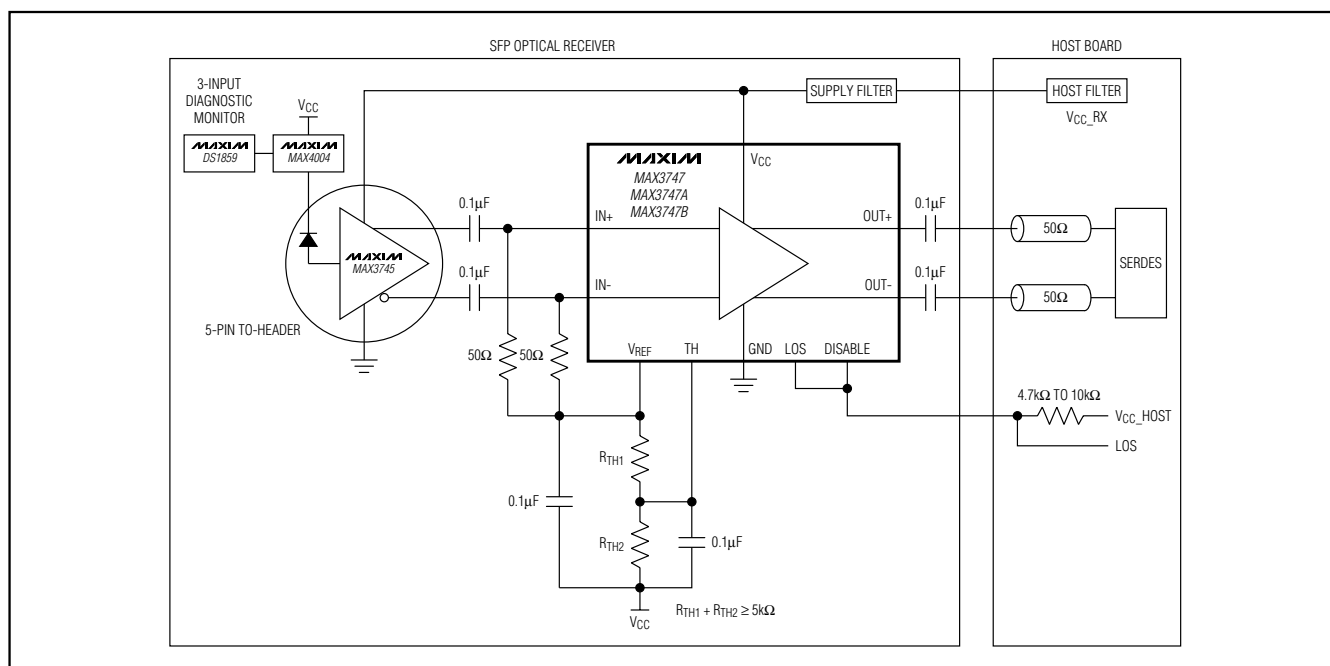
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3747EUB	-40°C to +85°C	10 $\mu$ MAX	U10C-4
MAX3747AEUB	-40°C to +85°C	10 $\mu$ MAX	U10C-4
MAX3747BEUB	-40°C to +85°C	10 $\mu$ MAX	U10C-4

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Pin Configuration appears at end of data sheet.

## Typical Application Circuit



# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage ( $V_{CC}$ )	-0.5V to +4.5V	Continuous Current at CML Outputs (OUT+, OUT-)	-25mA to +25mA
Voltage at IN+, IN-	( $V_{CC} - 2.4V$ ) to ( $V_{CC} + 0.5V$ )	Continuous Power Dissipation ( $T_A = +70^\circ C$ )	10-Pin $\mu$ MAX (derate 6.9mW/ $^\circ C$ above $+70^\circ C$ )
Voltage at DISABLE, LOS, TH, $V_{REF}$	-0.5V to ( $V_{CC} + 0.5V$ )	Operating Junction Temperature Range ( $T_J$ )	-55 $^\circ C$ to +150 $^\circ C$
Current into LOS	-1mA to +9mA	Storage Ambient Temperature Range ( $T_S$ )	-55 $^\circ C$ to +150 $^\circ C$
Current into $V_{REF}$	2mA		
Differential Input Voltage (IN+ - IN-)	2.5V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +2.97V$  to  $+3.63V$ , CML output load is  $50\Omega$  to  $V_{CC}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Current (Note 2)	$I_{CC}$	MAX3747 including the CML output current		30	35	mA
		MAX3747A including the CML output current		36	41	
		MAX3747B including the CML output current		38	43	
		MAX3747/MAX3747A excluding the CML output current		18	24	
		MAX3747B excluding the CML output current		20	26	
Power-Supply Noise Rejection	PSNR	$f < 2MHz$		30		dB
<b>INPUT SPECIFICATION</b>						
Input Sensitivity	$V_{IN-MIN}$	(Note 3)			4	mV <sub>P-P</sub>
Input Overload	$V_{IN-MAX}$	(Note 3)	1200			mV <sub>P-P</sub>
<b>OUTPUT SPECIFICATION</b>						
Output Resistance	$R_{OUT}$		42	50	58	$\Omega$
Differential Output Return Loss		DUT is powered on, $f < 3GHz$		15		dB
CML Differential Output Voltage		MAX3747A/MAX3747B $4mV_{P-P} \leq V_{IN} \leq 1200mV_{P-P}$	600	800	1000	mV <sub>P-P</sub>
		MAX3747 $4mV_{P-P} \leq V_{IN} \leq 1200mV_{P-P}$	400	500	600	
Differential Output Signal When Disabled		AC-coupled outputs, $V_{IN-MAX}$ applied to the input (Note 4)			15	mV <sub>P-P</sub>
Data-Output Transition Time		20% to 80% (Note 4)		70	120	ps
<b>TRANSFER CHARACTERISTIC</b>						
Deterministic Jitter (Notes 4, 5)	DJ	K28.5 pattern at 3.2Gbps		13.2	19	ps <sub>P-P</sub>
		PRBS $2^{23} - 1$ equivalent pattern at 2.7Gbps (Note 6)		14	25	
		K28.5 pattern at 2.1Gbps		12	17	
		PRBS $2^{23} - 1$ equivalent pattern at 155Mbps (Note 6)		85	150	
Random Jitter		$V_{IN} = 4mV_{P-P}$ (Notes 4, 7)		3.5	5	ps <sub>RMS</sub>

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MAX3747/MAX3747A/MAX3747B

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +2.97V$  to  $+3.63V$ , CML output load is  $50\Omega$  to  $V_{CC}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Referred Noise		$V_{IN} = 4mV_{P-P}$ (Note 4)		120	150	$\mu V_{RMS}$
Low-Frequency Cutoff				6.4		kHz
LOS Hysteresis		$10\log(V_{DEASSERT} / V_{ASSERT})$ (Note 4)	1.25			dB
LOS Assert/Deassert Time		MAX3747/MAX3747A (Notes 4, 8)	2.3		40.0	$\mu s$
		MAX3747B (Notes 4, 8, 9)				
Low LOS Assert Level		$V_{TH} = -1.3V$ (Notes 4, 10)	2.5	4.1	5.9	$mV_{P-P}$
Low LOS Deassert Level		$V_{TH} = -1.3V$ (Notes 4, 10)		6.2	9.3	$mV_{P-P}$
Medium LOS Assert Level		$V_{TH} = -0.68V$ (Notes 4, 10)	22.0	29.0	31.0	$mV_{P-P}$
Medium LOS Deassert Level		$V_{TH} = -0.68V$ (Notes 4, 10)		44.8	57.0	$mV_{P-P}$
High LOS Assert Level		$V_{TH} = -0.114V$ (Notes 4, 10)	36.0	53.7	63.6	$mV_{P-P}$
High LOS Deassert Level		$V_{TH} = -0.114V$ (Notes 4, 10)		86.0	115	$mV_{P-P}$
<b>TTL/CMOS I/O</b>						
$V_{REF}$ Voltage	$V_{REF}$		$V_{CC} - 1.35$	$V_{CC} - 1.3V$	$V_{CC} - 1.19$	V
LOS Output High Voltage	$V_{OH}$	$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to $V_{CC\_HOST}$ (3V)	2.4			V
LOS Output Low Voltage	$V_{OL}$	$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to $V_{CC\_HOST}$ (3.6V)			0.4	V
DISABLE Input High	$V_{IH}$		2.0			V
DISABLE Input Low	$V_{IL}$				0.8	V
DISABLE Input Current		$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to $V_{CC\_HOST}$			10	$\mu A$

**Note 1:** The data-input transition time is controlled by a 4th-order Bessel filter with  $f_{-3dB} = 0.75 \times 2.667GHz$  for all data rates of 2.667Gbps and below. The  $f_{-3dB} = 0.75 \times 3.2GHz$  for a data rate of 3.2Gbps.

**Note 2:** Supply current is measured with unterminated outputs or with AC-coupled output termination (see Figure 1).

**Note 3:** Between sensitivity and overload, all AC specifications are met and the output is 0.95 x limited output amplitude.

**Note 4:** Guaranteed by design and characterization.

**Note 5:** The deterministic jitter (DJ) caused by the input filter is not included in the DJ generation specification.

**Note 6:** The PRBS  $2^{23} - 1$  equivalent pattern consists of a K28.5 pattern plus 240 ones plus K28.5 pattern plus 240 zeros.

**Note 7:** Random jitter was measured without using a filter at the input.

**Note 8:** The signal at the input is switched between two amplitudes, Signal\_ON and Signal\_OFF, as shown in Figure 2A.

**Note 9:** The signal at the input is switched between 1.2V<sub>P-P</sub> and Signal\_OFF as shown in Figure 2B.

**Note 10:**  $V_{TH}$  is the voltage at pin 5 referenced to  $V_{CC}$  (see Figure 5).

# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

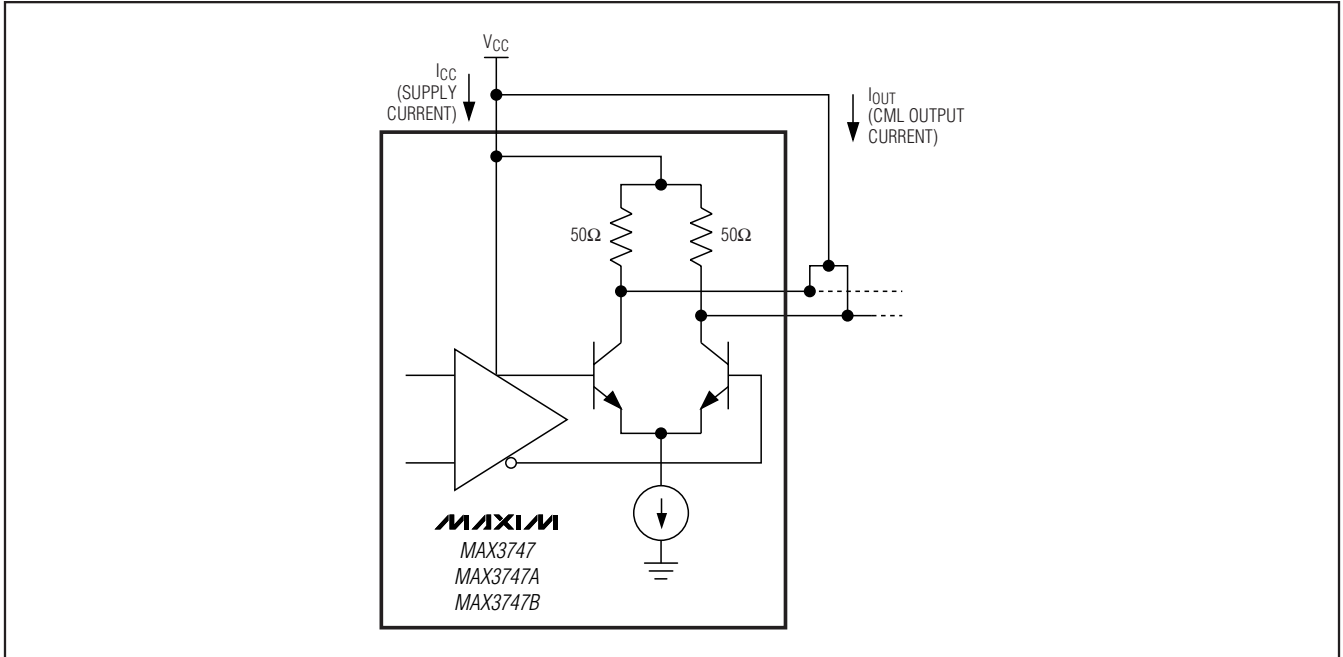


Figure 1. Power-Supply Current Measurement

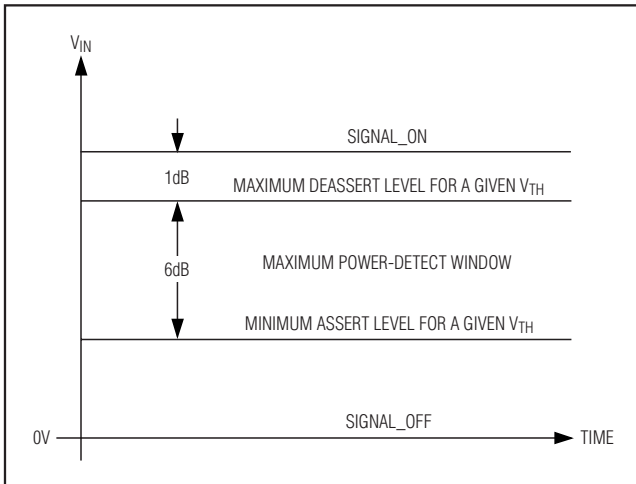


Figure 2A. LOS Deassert Threshold—Set 1dB Below Receiver Sensitivity

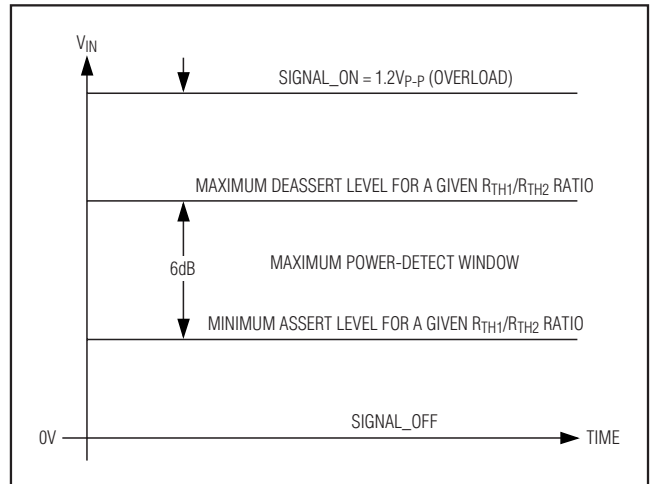


Figure 2B. LOS Deassert Threshold—Operating at Input Overload

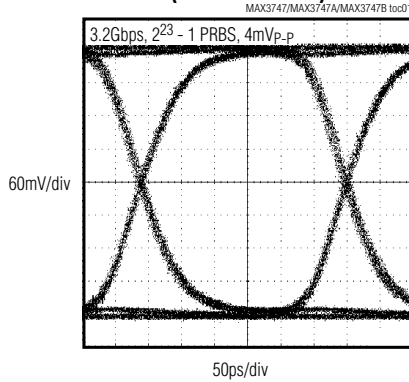
# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## Typical Operating Characteristics

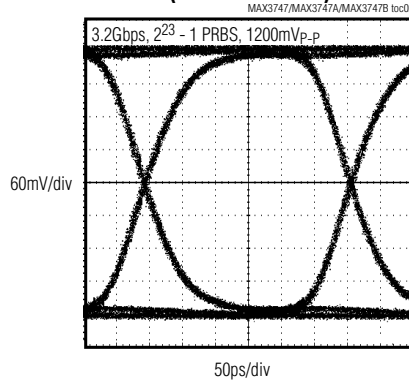
( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX3747/MAX3747A/MAX3747B

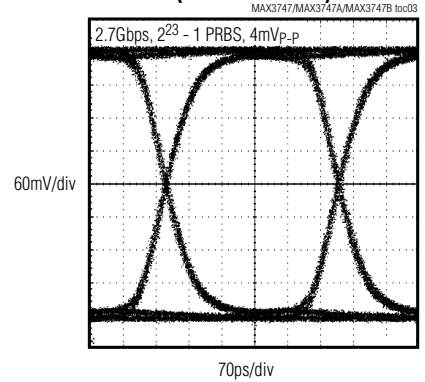
**OUTPUT EYE DIAGRAM (MINIMUM INPUT)**



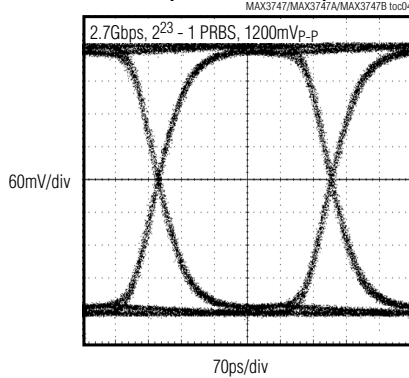
**OUTPUT EYE DIAGRAM (MAXIMUM INPUT)**



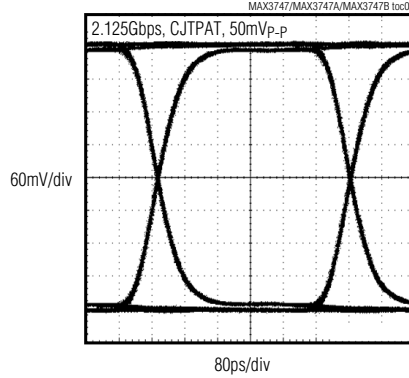
**OUTPUT EYE DIAGRAM (MINIMUM INPUT)**



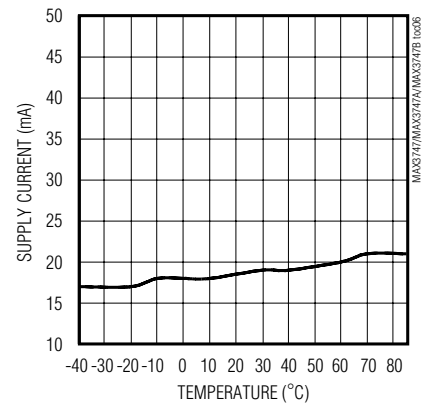
**OUTPUT EYE DIAGRAM (MAXIMUM INPUT)**



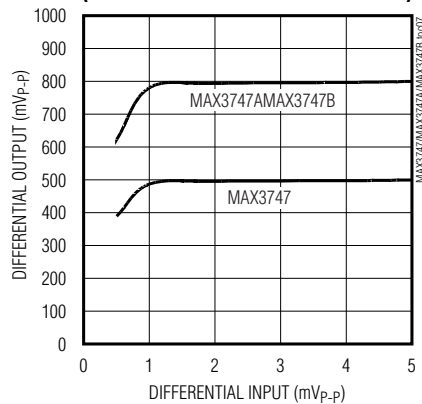
**OUTPUT EYE DIAGRAM AT +100°C**



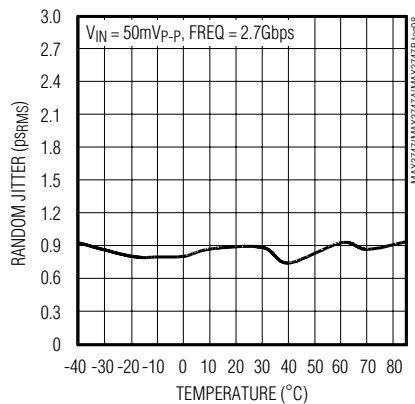
**SUPPLY CURRENT vs. TEMPERATURE (EXCLUDES OUTPUT CURRENT)**



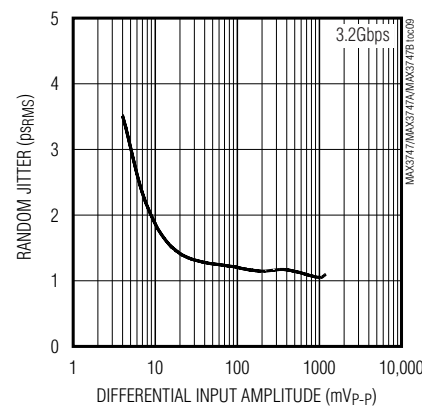
**TRANSFER FUNCTION (OUTPUT VOLTAGE vs. INPUT VOLTAGE)**



**RANDOM JITTER vs. TEMPERATURE**



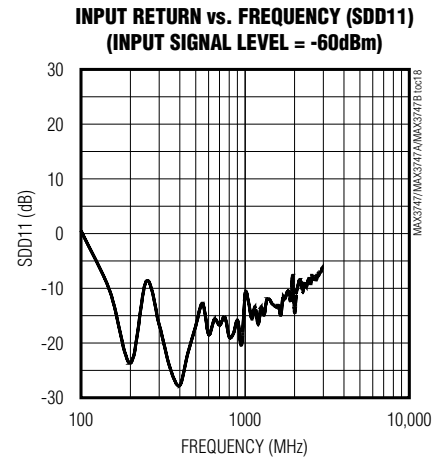
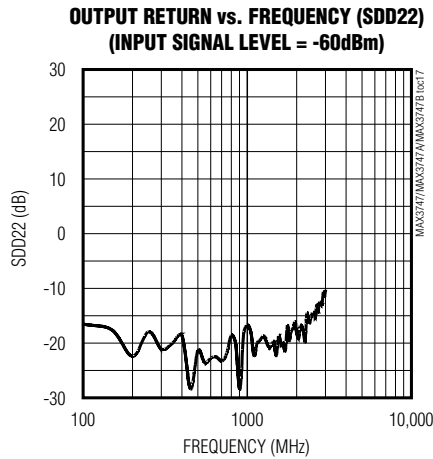
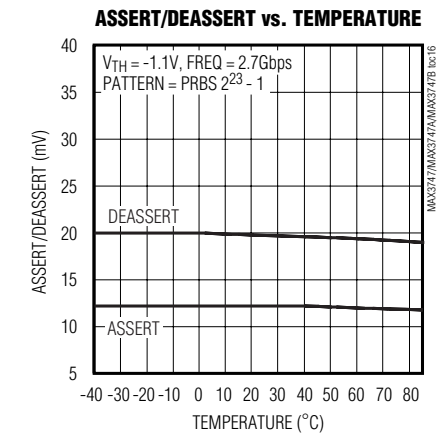
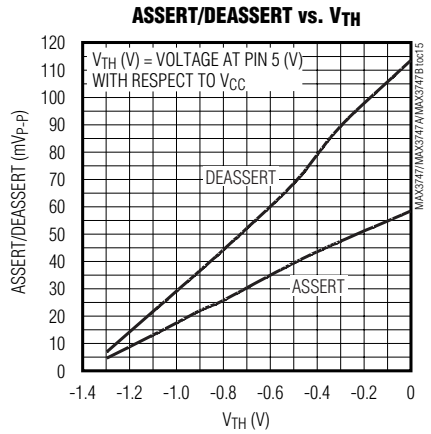
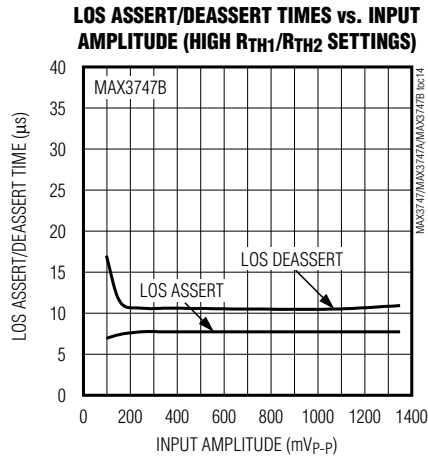
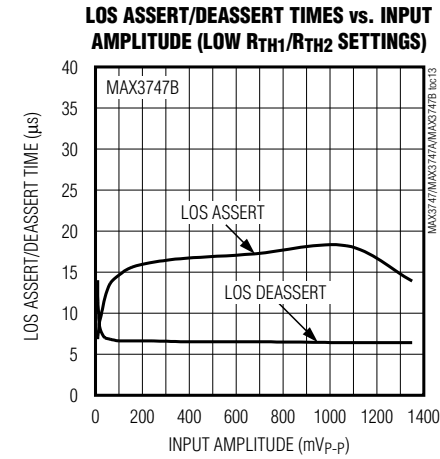
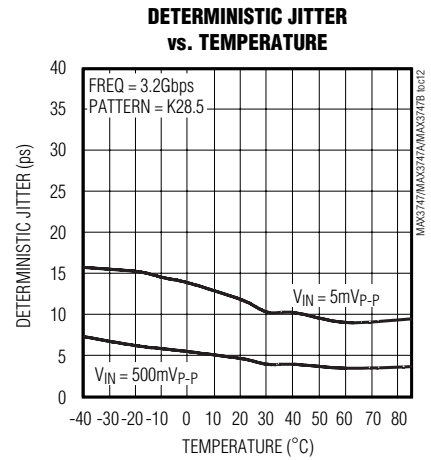
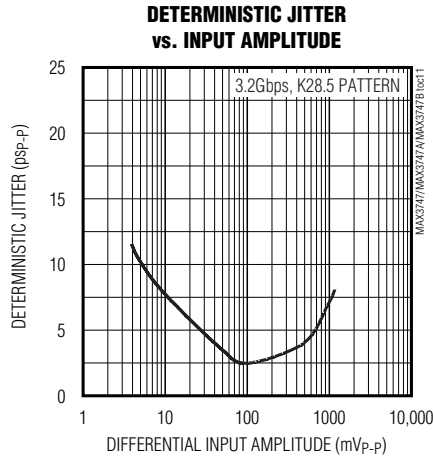
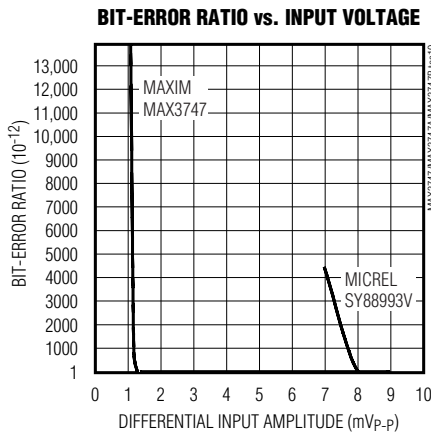
**RANDOM JITTER vs. INPUT AMPLITUDE**



# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## Pin Description

MAX3747/MAX3747A/MAX3747B

PIN	MAX3747/ MAX3747A/ MAX3747B	MICREL SY8893V	FUNCTION
	NAME	NAME	
1	DISABLE	$\overline{EN}$	Disable Function Pin. The data outputs are held static when this pin is asserted high, transistor-to-transistor logic (TTL). The data outputs are enabled when this pin is held low. LOS functions remain active when outputs are disabled. For normal operation connect to GND.
2	IN+	DIN	Noninverted Input Signal
3	IN-	$\overline{DIN}$	Inverted Input Signal
4	VREF	VREF	Reference Voltage for LOS Threshold Setting
5	TH	LOSLVL	Loss-of-Signal Level Set. A voltage on this pin created by a two-resistor divider sets the threshold level. Connect one resistor from this pin to VCC and another from this pin to VREF (see Figure 5).
6	GND	GND	Ground
7	LOS	LOS	Loss of Signal. Open collector for the MAX3747 and MAX3747A; internal 100k $\Omega$ pullup to VCC for the MAX3747B. LOS is high when the level of the input signal drops below the preset threshold set by the TH input. LOS is deasserted low when the signal level is above the threshold.
8	OUT-	$\overline{DOUT}$	Inverted Data Output, CML
9	OUT+	DOUT	Noninverted Data Output, CML
10	VCC	VCC	Positive Power Supply

## Detailed Description

The limiting amplifiers consist of a multistage amplifier, offset-correction circuitry, an output buffer, and loss-of-signal detect circuitry (see the *Functional Diagram*).

### Input Stage

The input stage is shown in Figure 3. It provides 50 $\Omega$  termination to VREF for each input signal, IN+ and IN-. The MAX3747/MAX3747A/MAX3747B should be AC-coupled.

### Multistage Amplifier

The high-bandwidth multistage amplifier provides approximately 57dB of gain for the MAX3747 and 61dB of gain for the MAX3747A/MAX3747B.

### Offset Correction Loop

The MAX3747/MAX3747A/MAX3747B are susceptible to DC offsets in the signal path because they have high gain. In communication systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated in the transimpedance amplifier appears as an input offset and is reduced by the offset correction loop.

The offset correction loop sets a low-frequency cutoff of 3.2kHz.

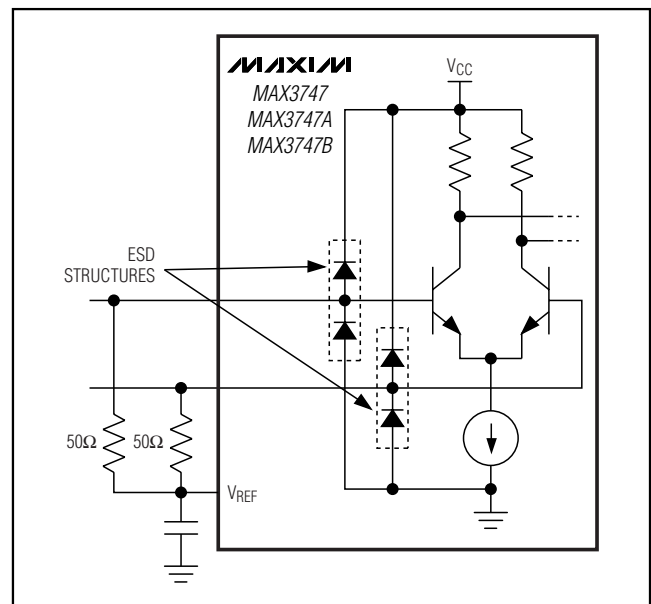
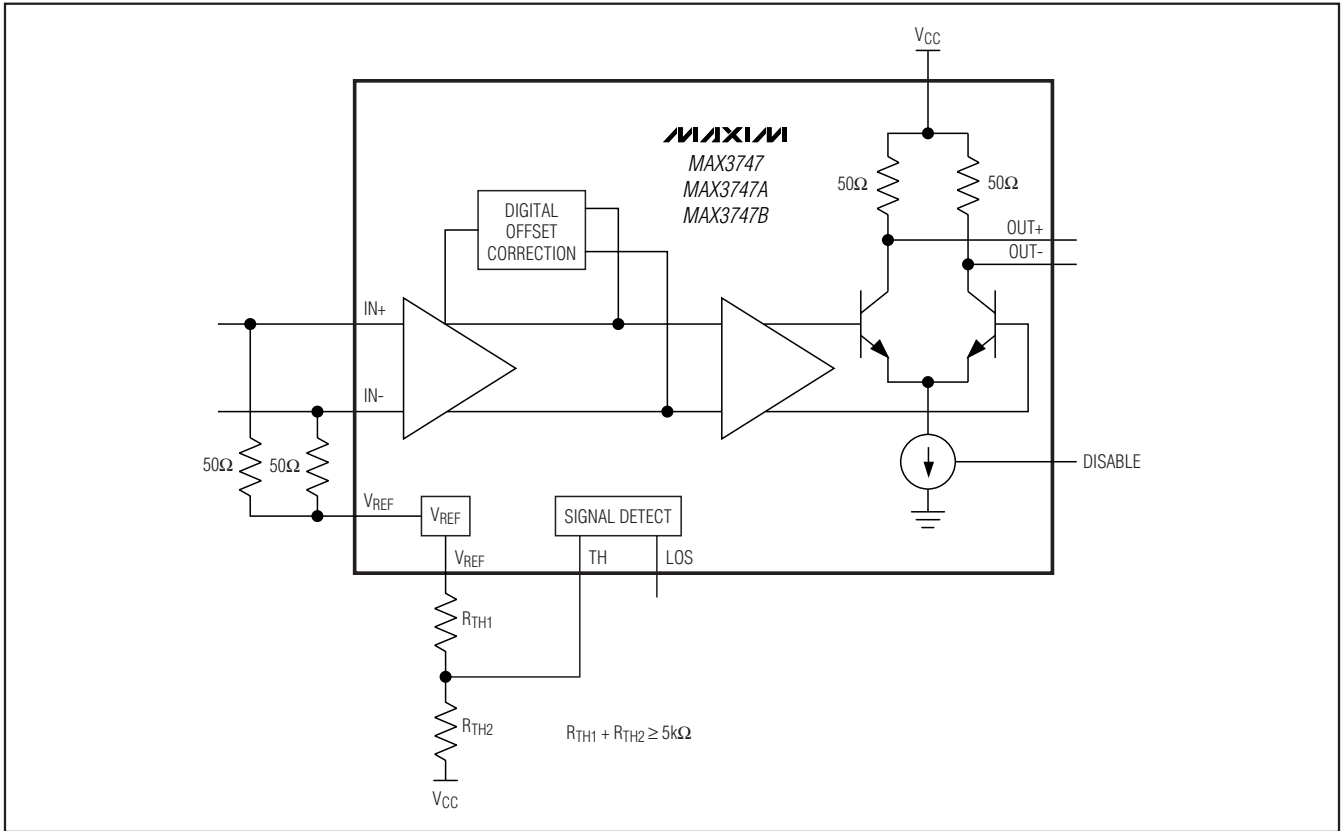


Figure 3. Differential Input Stage

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## Functional Diagram



### CML Output Buffer

The CML outputs of the MAX3747/MAX3747A/MAX3747B limiting amplifiers provide high tolerance to impedance mismatches and inductive connectors. The output current is approximately 10mA for the MAX3747 and 16mA for the MAX3747A/MAX3747B. Connecting the DISABLE pin to VCC disables the output. If the LOS pin is connected to the DISABLE pin, the outputs OUT+ and OUT- are at a static voltage (squelch) whenever the input signal level drops below the LOS threshold. The output buffer can be AC- or DC-coupled to the load (Figure 4).

The MAX3747 output is 500mV<sub>P-P</sub> and the MAX3747A/MAX3747B output is 800mV<sub>P-P</sub>.

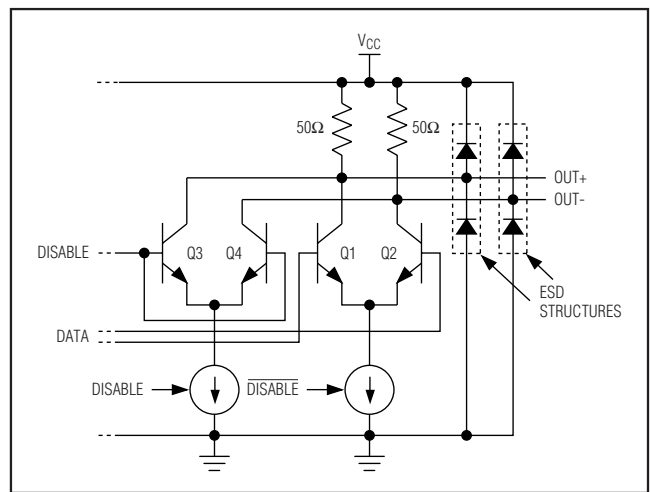


Figure 4. CML Output Buffer



# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

MAX3747/MAX3747A/MAX3747B

## Loss-of-Signal Indicator

The MAX3747/MAX3747A/MAX3747B are equipped with LOS circuitry that indicates when the input signal is below a programmable threshold, set by a voltage on the TH pin (see the *Typical Operating Characteristics*). The voltage on the TH pin is set by two resistors, one connecting from the TH pin to VCC and the other connecting from TH to VREF (Figure 5). An RMS power detector compares the input signal amplitude with this threshold and feeds the signal-detect information to the LOS output, which is open collector. To prevent LOS chatter in the region of the programmed threshold, approximately 2dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level. Figure 6 shows the LOS output circuit.

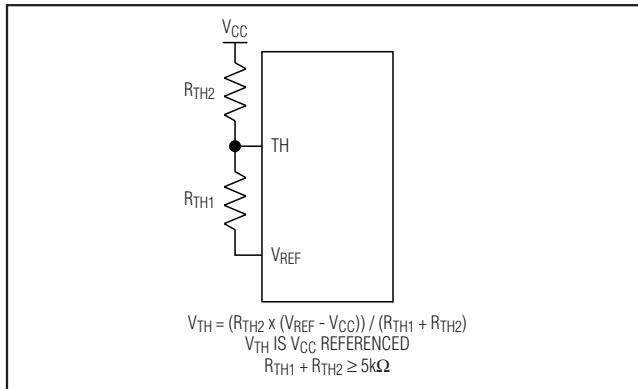


Figure 5. MAX3747/MAX3747A/MAX3747B LOS Threshold Circuit

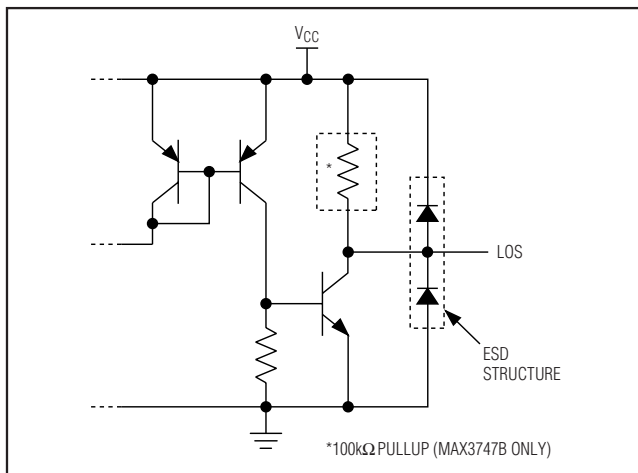


Figure 6. MAX3747/MAX3747A/MAX3747B LOS Output Circuit

## Applications Information

### Program the LOS Assert Threshold

Program the LOS assert threshold according to Figure 5. The combination of RTH1 and RTH2 should be greater than or equal to 5kΩ, see the Assert/Deassert vs. VTH graph in the *Typical Operating Characteristics*.

### Select the Coupling Capacitor

When AC-coupling is desired, coupling capacitors CIN and COUT should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (fIN) is decreased:

$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For all applications, the recommended value for CIN and COUT is 0.1μF, which provides fIN equal to 32kHz. Refer to Application Note HFAN-1.1: *Choosing AC-Coupling Capacitors* on the Maxim website ([www.maxim-ic.com](http://www.maxim-ic.com)).

# 155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

## Chip Information

TRANSISTOR COUNT: 447

PROCESS: SiGe Bipolar

## Package Information

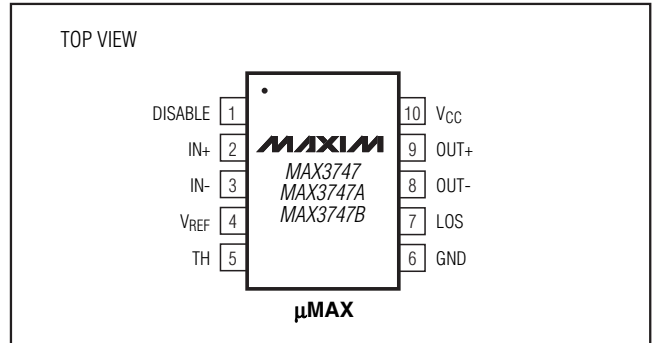
For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	DOCUMENT NO.
10 $\mu$ MAX	<a href="#">21-0061</a>

## Revision History

Pages changed at Rev 1: 1 to 10 (added MAX3747B)

## Pin Configuration



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