Applying the DLX1414
Intelligent Display® Products
Appnote 15

This application note is intended to serve as a design and application guide for users of the DLX1414 alphanumeric Intelligent Display. The information presented covers device electrical description and operation, considerations for general circuit design, and interfacing the DLX1414 to microprocessors.

Electrical & Mechanical Description

The internal electronics of the Intelligent Display eliminates all the traditional difficulties of using multi-digit light emitting displays (decoding, drivers and multiplexing). The Intelligent Display also provides internal memory for the four digits. With this approach the user can asynchronously address one of four digits and load new data without regard to the LED multiplex timing.

Figure 1 is a block diagram of the DLX1414. The device consists of four (5x7) LED arrays and a single CMOS integrated chip. The IC chip contains the column drivers and row drivers, 128 character ROM, four word x7 bit Random Access Memory, oscillator for multiplexing, multiplex counter/decoder, cursor memory, address decoder, and miscellaneous control logic.
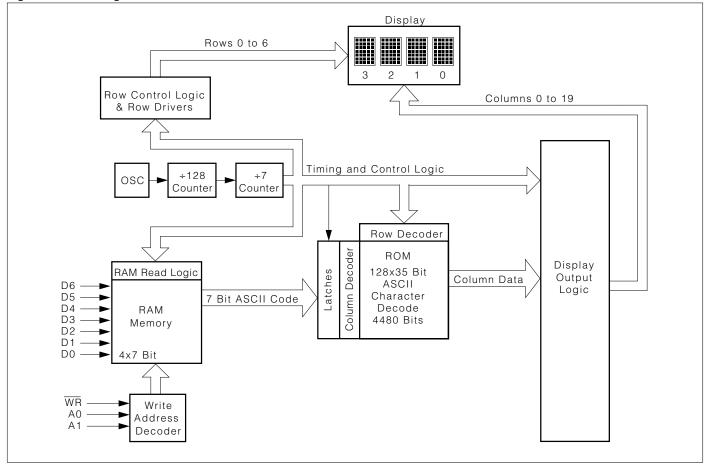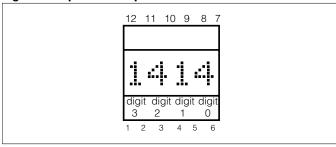
Figure 1. Block Diagram–DLX1414

Figure 2. Top view and pin outs

12 11 10 9 8 7

1414

digit digit digit digit
3 2 1 0
1 2 3 4 5 6

Pin	Function	Pin	Function
1	D5 Data Input	7	GND
2	D4 Data Input	8	D0 Data Input (LSB)
3	$\overline{WR}$ Write	9	D1 Data Input
4	A1 Digit Select	10	D2 Data Input
5	A0 Digit Select	11	D3 Data Input
6	V_{CC}	12	D6 Data Input (MSB)

Packaging

Packaging consists of an injection-molded plastic lens which covers five of the six "faces." The assembled and tested substrate is placed within the shell and the entire assembly is then filled with a waterclear IC-grade epoxy.

This yields a very rugged part which is quite impervious to moisture, shock and vibration. Although not "hermetic, the device will easily withstand total immersion in water/detergent solutions.

Figure 3. Character set–DLX1414

1. High=1 level. 2. Low=0 level. 3. Upon power up, device will initialize in a random state.

Table 1. Electrical inputs to the DLX1414

V_{CC}	Positive supply +5 V
GND	Ground
D0–D6	Data lines The seven data input lines are designed to accept the first 128 ASCII characters. See Figure 3 for the character set.
A0, A1	Address Lines The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.
$\overline{WR}$	Write (Active Low) Data and address to be loaded must be present and stable before and after the trailing edge of write. (See data sheet for timing info).

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e., synchronize before a Write can be done. This can be slow and cumbersome.
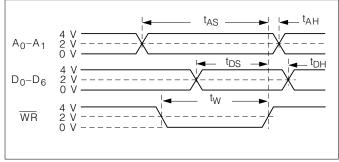
Data entry in Intelligent Displays is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

The waveforms in Figure 4 demonstrate the relationships of the signals required to generate a Write cycle. (Check individual data sheet for minimum values.) As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of Write.

General Design Considerations

Using positive true logic, address order is from right to left. For left to right address order, use the ones complement or simple inversion of the addresses.

Figure 4. Write cycle waveform

When using the DLX1414 on a separate display board with more than 6 inches of cable length, it may be necessary to buffer all inputs. This is most easily achieved with Hex non-inverting buffers such as the 74365. The object is to prevent transient current in the protection diodes. The buffers should be located on the display board near the displays.

Local power supply bypass capacitors are also needed in many cases. These should be 6 or 10 volt, tantalum type with 10 µF or greater capacitance. Low internal resistance is important due to current steps which result from the internal multiplexing of the displays.

If small wire cables are used, good engineering practice is to calculate the wire resistance of the ground plus the +5 volt wires. More than 0.1 volt drop, (at 25 mA per digit worst case) should be avoided, since this loss is in addition to any inaccuracies or load regulation limitations of the power supply.

The 5-volt power supply for the displays should be the same one supplying V_{CC} to all logic devices which drive the display devices. If a separate supply must be used, then local buffers using hex, non-inverting gates should be used on all inputs and these buffers should be powered from the display power supply. This precaution is to avoid logic inputs higher than display V_{CC} during power up or line transients.

Interfacing the DLX1414

A general and straightforward interface circuit is shown in Figure 6. This scheme can easily interface to LP systems or any other systems which can provide the seven data lines, appropriate address and control lines.

The DLX1414 does not have a chip enable input; therefore each display in a system requires its Write pulse be gated with appropriate address signals. Figure 7a shows the use of a 74154 decoder (4 lines to 16 lines) for up to a 64 character display. Using the G1 input for display select (address select in a memory mapped system) and the G2 input to gate the Write signal. Another approach (Figure 7b and 7c) which minimizes logic for a 16 or 32 digit display takes advantage of decoding scheme of the 7442 decoder.

Parallel I/O

The parallel I/O device of a microprocessor can be connected easily to the circuit in Figure 6. One eight bit output port can provide the seven input data bits. Another eight bit output port can contain the address and control signals.

Figure 5. Data loading table

	Address		Data Input							Digit 3	Digit 2	Digit 1	Digit 0
$\overline{WR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0				
H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
L	L	L	H	L	L	L	L	L	H	NC	NC	NC	A
L	L	H	H	L	L	L	L	H	L	NC	L	B	A
L	H	L	H	L	L	L	L	H	H	NC	C	B	A
L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	–	–	–	–	–	–	–	–	–	See Character Set			

X=Don't care   NC=No change

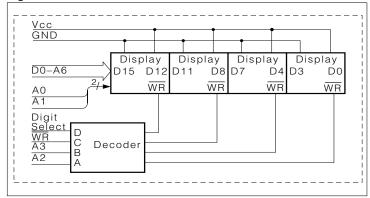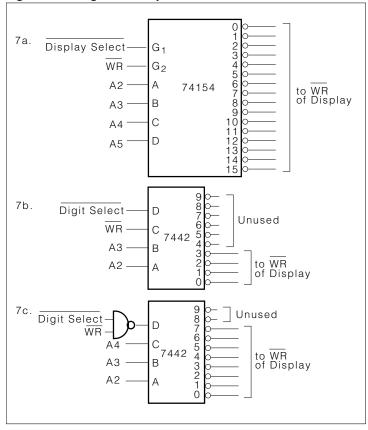**Figure 6. General interface circuit**

Figure 7. Gating the write pulse
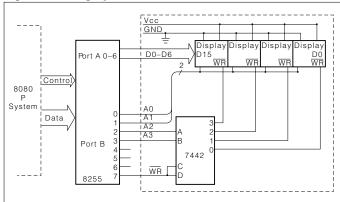
Figure 8. 16-digit parallel I/O

Figure 8 illustrates a 16-character display with an 8080 system using the 8255 programmable peripheral interface I/O device. The following program will display a simple 16 character message using this interface.

Program for 16-Character Message

INT:	MVI A,80H OUT CON- TROLMVI B,00H	;CONTROL DATA MODE 0 ;LOAD CONTROL REGISTER ;SET COUNTER =0
DISP:	LXI H, TABLE	;SET TABLE ADDRESS

DISP1:	MOV A,M
	
	OUT PORTA
	MOV A, B
	CALL DSPWT
	INX H
	INR B
	MVI A, 10H
	CMP B
	JNZ DISP1
	HALT
		;MOVE TABLE DATA TO
		ACCUMULATOR
		;LOAD DATA PORT
		
		;LOAD ADDRESS AND CONTROL
		;INCREMENT TABLE ADDRESS
		;INCREMENT COUNTER
		;SET # OF DIGITS
		
		;16 CHARACTERS ?
		;END OF PROGRAM

DSPWT:	ORI F0H OUT PORTB ANI 7FH OUT PORTB ORI F0H OUT PORTB RET	;SET CONTROL BITS OFF ;LOAD CONTROL ;SET WRITE BIT ON ;LOAD WRITE ;SET WRITE BIT OFF ;LOAD CONTROL
TABLE:	DL DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB	;0C3H ;0C9H ;0D4H ;0D3H ;0C1H ;0D4H ;0CEH ;0C1H ;0C6H ;0A0H ;0D3H ;0D4H ;0C8H ;0C7H ;0C9H ;0CCH

I/O or Memory Mapped Addressing

Some designers may wish to avoid the additional cost of a parallel I/O in their system. Structuring the addressing architecture for the DLX1414 to look like a set of peripheral or output devices (I/O mapped) or RAMs and ROMs (memory mapped), is very easy. Figure 9 shows the simplicity of interfacing to microprocessors, such as 8080, Z80 and 6502 as examples.

The interface with the 6800 microprocessor in Figure 10 illustrates the need for designers to check the timing requirements of the DLX1414 and the LP. The typical data output hold time is only 30 ns for DBE=02 timing; two inverters in the DBE line are added to increase the data output hold time for compatibility with the 50 ns minimum spec of the DLX1414.
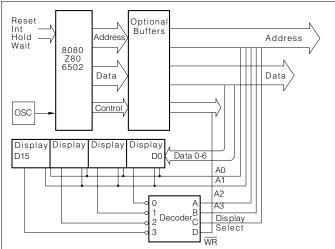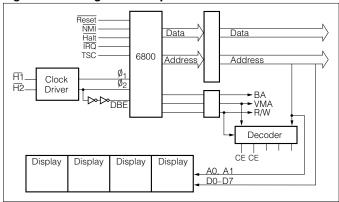
Figure 9. Mapped interface

Figure 10. Gating the write pulse

Conclusion

Although other manufacturers' products are used in examples, this application note does not imply specific endorsement, or recommendation or warranty of other manufacturer's products by Infineon / OSRAM.

The interface schemes shown demonstrate the simplicity of using the DLX1414 with microprocessors. The slight differences encountered with different microprocessors to interface with the DLX1414 are similar to those encountered when using different RAMs The techniques used in the examples were shown for their generality. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.