SONY

SP9T GSM/UMTS Dual Mode Antenna Switch

CXM3512EQ

Description

The CXM3512EQ is one of a range of low insertion loss, high linearity, low IMD and high power MMIC antenna switch modules for GSM/UMTS or CDMA dual-mode handsets.
The Sony L.F.M.* contains SP9T switch die, CMOS decoder and a dual-LPF on GSM transmit paths for suppression of transmitter harmonics.
Excellent insertion loss contributes to the good sensitivity and longer talk time. This switch also provides excellent ESD performance.

* L.F.M. = Lead Frame Module

(Applications: GSM (4 bands) / UMTS (3 bands, class I-VI) or CDMA (2 bands) dual-mode handset)

Features

- ◆ Low insertion loss
  - 0.80dB (typ.) on TX1 (915MHz)
  - 0.95dB (typ.) on TX2 (1910MHz)
  - 0.65dB (typ.) on RX (960MHz)
  - 0.65dB (typ.) on TRx (1980MHz)
- ◆ Built-in dual-LPF
  - Att –30dB (typ.) @2fo (Tx1 path)
  - Att –30dB (typ.) @2fo (Tx2 path)
- ◆ TRXs and RXs paths are changeable for band assignment.
- ◆ 4 CMOS compatible control lines
- ◆ Low voltage operation (V_{DD} = 2.5V)
- ◆ Lead-free and RoHS compliant

Package

Small package size: 30-pin LQFN (4.4 × 4.0 × 1.3mm)

Structure

GaAs Junction-gate PHEMT SW, CMOS decoder and dual-LPF
Sony PHEMT GaAs process is utilized for low insertion loss.

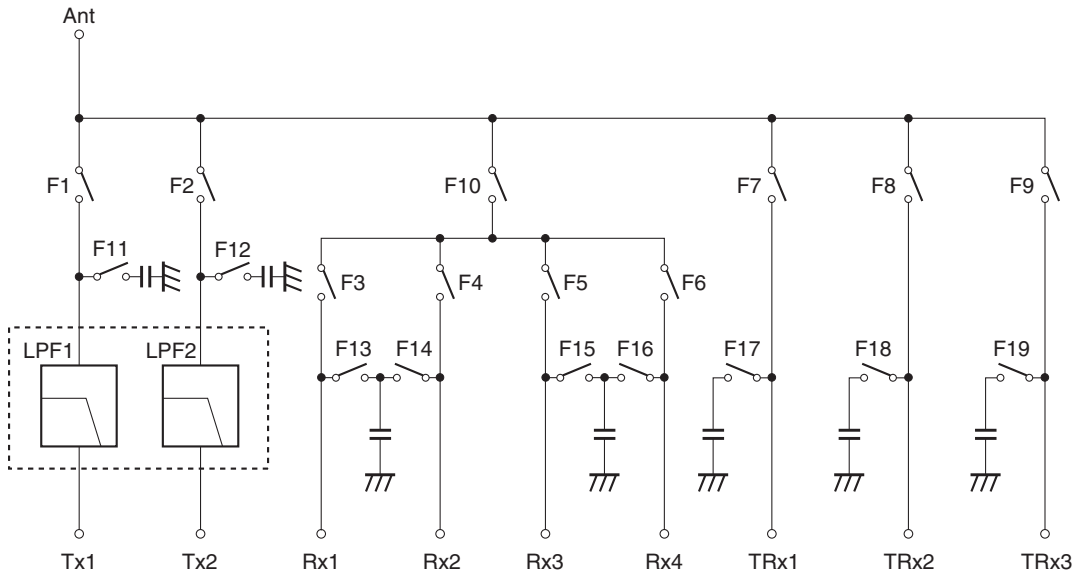
This IC is ESD sensitive device. Special handling precautions are required.

Absolute Maximum Ratings

(Ta = 25℃)

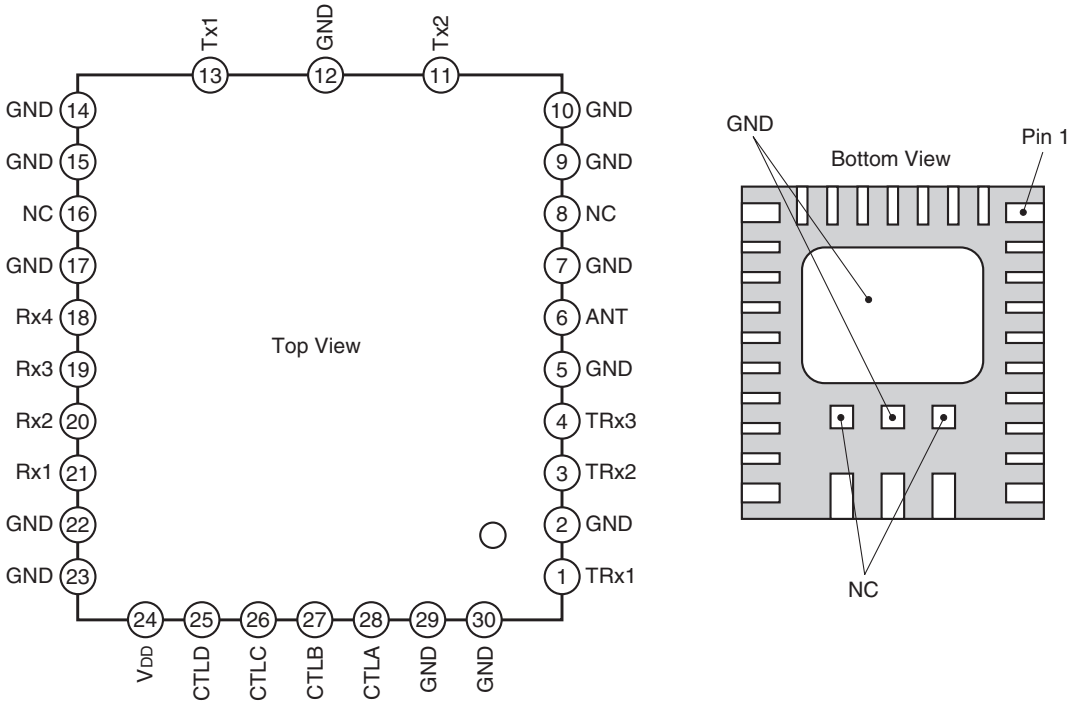
◆ Bias voltage	V_{DD}	4	V
◆ Control voltage (CTL-A/B/C/D)	Vctl	4	V
◆ Operating temperature	Topr	–20 to +90	℃
◆ Storage temperature	Tstg	–65 to +150	℃

Block Diagram



Note) Built-in SW control circuit

Pin Configuration



Note) Each RX path can be used from 869 to 1990MHz frequency. User can select these RX paths suitably.

Pin Description

Pin No.	Symbol	Pin No.	Symbol
1	TRx1	16	NC
2	GND	17	GND
3	TRx2	18	Rx4
4	TRx3	19	Rx3
5	GND	20	Rx2
6	ANT	21	Rx1
7	GND	22	GND
8	NC	23	GND
9	GND	24	V_{DD}
10	GND	25	CTLD
11	Tx2 (DCS/PCS)	26	CTLC
12	GND	27	CTLB
13	Tx1 (GSM850/900M)	28	CTLA
14	GND	29	GND
15	GND	30	GND

Truth Table

Active path	Vctl state				Switch state																	
	A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19
Tx1	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Tx2	H	L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H
Rx1*2	L	L	L	L	L	L	H	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H
Rx2*2	L	L	H	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H
Rx3*2	L	H	H	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
Rx4*2	L	H	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H
TRx1	H	L	H	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H
TRx2	H	H	H	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	L	H
TRx3	—*1	—*1	—*1	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L

*1 These states are available to set either H or L.

*2 Each RX path can be used from 869 to 1990MHz frequency. User can select these RX paths suitably.

Electrical Characteristics

(V_{DD} = 2.5V, Vctl = 2.5V, Ta = 25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx1 – Ant	*1	—	0.80	0.95	dB
		Tx2 – Ant	*2	—	0.95	1.20	
		Ant – TRx1 (Tx)	*3	—	0.40/0.65	0.55/0.85	
		Ant – TRx2 (Tx)	*3	—	0.40/0.65	0.55/0.85	
		Ant – TRx3 (Tx)	*3	—	0.40/0.65	0.55/0.85	
		Ant – Rx1	*4	—	0.65/1.10	0.80/1.25	
		Ant – Rx2	*4	—	0.65/1.10	0.80/1.25	
		Ant – Rx3	*4	—	0.65/1.10	0.80/1.25	
		Ant – Rx4	*4	—	0.65/1.10	0.80/1.25	
		Ant – TRx1 (Rx)	*5	—	0.40/0.75	0.55/0.90	
		Ant – TRx2 (Rx)	*5	—	0.40/0.75	0.55/0.90	
		Ant – TRx3 (Rx)	*5	—	0.40/0.75	0.55/0.90	

*1 Frequency = 824 to 849, 890 to 915MHz, Input signal is burst, Pin = +34dBm

*2 Frequency = 1710 to 1785, 1850 to 1910MHz, Input signal is burst, Pin = +32dBm

*3 Frequency = 810 to 855/1710 to 1980MHz, Input signal is CW, Pin = +29dBm

*4 Frequency = 869 to 894, 935 to 960/1805 to 1880, 1930 to 1990MHz, Input signal is CW, Pin = –5dBm

*5 Frequency = 855 to 900/1930 to 1990, 2110 to 2170MHz, Input signal is CW, Pin = –5dBm

(V_{DD} = 2.5V, Vctl = 2.5V, Ta = 25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	**TX Path Activated**						
	ISO.	Active path: TX1 – Ant					dB
		TX1 – RX1	824 to 915MHz	30	45	—	
		TX1 – RX2		30	50	—	
		TX1 – RX3		30	45	—	
		TX1 – RX4		30	40	—	
		TX1 – TX2		20	30	—	
			1760 to 1830MHz	20	30	—	
		TX1 – TRX1	824 to 915MHz	25	35	—	
		TX1 – TRX2		25	30	—	
		TX1 – TRX3		25	35	—	
		Active path: TX2 – Ant					
		TX2 – RX1	1710 to 1785MHz 1850 to 1910MHz	32	45	—	
		TX2 – RX2		32	45	—	
		TX2 – RX3	1850 to 1880MHz	32	45	—	
		TX2 – RX4	1710 to 1785MHz 1850 to 1910MHz	32	45	—	
		TX2 – TRX1		25	33	—	
		TX2 – TRX2		25	33	—	
		TX2 – TRX3		25	33	—	
		Active path: TRX1 – Ant					
		TRX1 – RX1	810 to 855MHz 1710 to 1980MHz	30	37	—	
		TRX1 – RX2		30	37	—	
		TRX1 – RX3		30	40	—	
		TRX1 – RX4		30	43	—	
		TRX1 – TX1		30	37	—	
		TRX1 – TX2		20	28	—	
		TRX1 – TRX2		15	19	—	
		TRX1 – TRX3		20	28	—	
		Active path: TRX2 – Ant					
		TRX2 – RX1	810 to 855MHz 1710 to 1980MHz	30	38	—	
		TRX2 – RX2		30	39	—	
		TRX2 – RX3		30	41	—	
		TRX2 – RX4		30	45	—	
		TRX2 – TX1		30	37	—	
		TRX2 – TX2		20	29	—	
		TRX2 – TRX1		20	28	—	
		TRX2 – TRX3		13	18	—	

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO.	Active path: TRX3 – Ant					dB
		TRX3 – RX1	810 to 855MHz 1710 to 1980MHz	30	36	—	
		TRX3 – RX2		30	37	—	
		TRX3 – RX3		30	40	—	
		TRX3 – RX4		30	43	—	
		TRX3 – TX1		25	36	—	
		TRX3 – TX2		20	28	—	
		TRX3 – TRX1		20	29	—	
		TRX3 – TRX2		15	21	—	
	RX Path Activated						
	ISO.	Active path: Ant – RX1					dB
		RX1 – TX1	824 to 915MHz	30	36	—	
		RX1 – TX2	1710 to 1910MHz	20	27	—	
		RX1 – TRX1	810 to 855MHz 1710 to 1980MHz	25	30	—	
		RX1 – TRX2		25	32	—	
		RX1 – TRX3		25	34	—	
		Active path: Ant – RX2					
		RX2 – TX1	824 to 915MHz	30	36	—	
		RX2 – TX2	1710 to 1910MHz	20	26	—	
		RX2 – TRX1	810 to 855MHz 1710 to 1980MHz	25	30	—	
		RX2 – TRX2		25	32	—	
		RX2 – TRX3		25	34	—	
		Active path: Ant – RX3					
		RX3 – TX1	824 to 915MHz	30	35	—	
		RX3 – TX2	1710 to 1910MHz	20	26	—	
		RX3 – TRX1	824 to 849MHz 1710 to 1980MHz	25	31	—	
		RX3 – TRX2	824 to 849MHz 1710 to 1980MHz	25	32	—	
		RX3 – TRX3	824 to 849MHz 1710 to 1980MHz	25	34	—	
		Active path: Ant – RX4					
		RX4 – TX1	824 to 915MHz	30	36	—	
		RX4 – TX2	1710 to 1910MHz	20	26	—	
		RX4 – TRX1	824 to 849MHz 1710 to 1980MHz	25	31	—	
		RX4 – TRX2	824 to 849MHz 1710 to 1980MHz	25	32	—	
		RX4 – TRX3	824 to 849MHz 1710 to 1980MHz	25	34	—	

(V_{DD} = 2.5V, Vctl = 2.5V, Ta = 25°C)

Item	Band	Condition	TRX1		TRX2		TRX3		Unit
			Min.	Typ.	Min.	Typ.	Min.	Typ.	
IIP2	IMT	fcw1 = 1950MHz, Pcw1 = +20dBm fcw2 = 190MHz, Pcw2 = –15dBm	+102	+115	+102	+112	+102	+112	dBm
	PCS	fcw1 = 1880MHz, Pcw1 = +20dBm fcw2 = 80MHz, Pcw2 = –15dBm	+102	+104	+102	+104	+102	+104	
	DCS	fcw1 = 1745MHz, Pcw1 = +20dBm fcw2 = 95MHz, Pcw2 = –15dBm	+102	+106	+102	+104	+102	+104	
	US cell	fcw1 = 835MHz, Pcw1 = +20dBm fcw2 = 45MHz, Pcw2 = –15dBm	+102	+107	+102	+104	+102	+104	
IIP3	IMT	fcw1 = 1950MHz, Pcw1 = +20dBm fcw2 = 1760MHz, Pcw2 = –15dBm	+61	+67	+61	+67	+61	+67	dBm
	PCS	fcw1 = 1880MHz, Pcw1 = +20dBm fcw2 = 1800MHz, Pcw2 = –15dBm	+61	+63	+61	+63	+61	+63	
	DCS	fcw1 = 1745MHz, Pcw1 = +20dBm fcw2 = 1650MHz, Pcw2 = –15dBm	+61	+66	+61	+66	+61	+66	
	US cell	fcw1 = 835MHz, Pcw1 = +20dBm fcw2 = 790MHz, Pcw2 = –15dBm	+61	+67	+61	+67	+61	+67	

(V_{DD} = 2.5V, Vctl = 2.5V, Ta = 25°C)

Item	Symbol	Path		Condition		Min.	Typ.	Max.	Unit
Harmonic		Tx1 – Ant*1	2nd harmonic	1648 to 1698MHz 1780 to 1830MHz	Burst Pin = +34dBm	—	–47	–36	dBm
			3rd harmonic	2472 to 2547MHz 2670 to 2745MHz		—	–42	–36	
		Tx2 – Ant*2	2nd harmonic	3420 to 3570MHz 3700 to 3820MHz	Burst Pin = +32dBm	—	–47	–35	
			3rd harmonic	5130 to 5355MHz 5550 to 5730MHz		—	–39	–35	
		TRx1 – Ant TRx2 – Ant TRx3 – Ant*3	2nd harmonic	1620 to 1710MHz 3420 to 3960MHz	CW, Pin = +29dBm	—	–60/ –50	–36	
			3rd harmonic	2430 to 2565MHz 5130 to 5940MHz		—	–52/ –50	–36	

*1 Frequency = 824 to 849, 890 to 915MHz, Input signal is burst, Pin = +34dBm

*2 Frequency = 1710 to 1785, 1850 to 1910MHz, Input signal is burst, Pin = +32dBm

*3 Frequency = 810 to 855/1710 to 1980MHz, Input signal is CW, Pin = +29dBm

(V_{DD} = 2.5V, Vctl = 2.5V, Ta = 25°C)

Item	Symbol	Path	Condition		Min.	Typ.	Max.	Unit
Attenuation		Tx1 – Ant	1648 to 1830MHz	2fo	25	30	—	dB
			2472 to 2745MHz	3fo	25	30	—	
			3296 to 3660MHz	4fo	20	30	—	
			4120 to 4575MHz	5fo	15	30	—	
			4944 to 5490MHz	6fo	15	25	—	
			5768 to 6405MHz	7fo	15	20	—	
		Tx2 – Ant	3420 to 3820MHz	2fo	25	30	—	
			5130 to 5730MHz	3fo	25	30	—	

Supply voltage

(Ta = 25℃)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V_{DD})	2.5	2.65	3.3	V

Logic value

(Ta = 25℃)

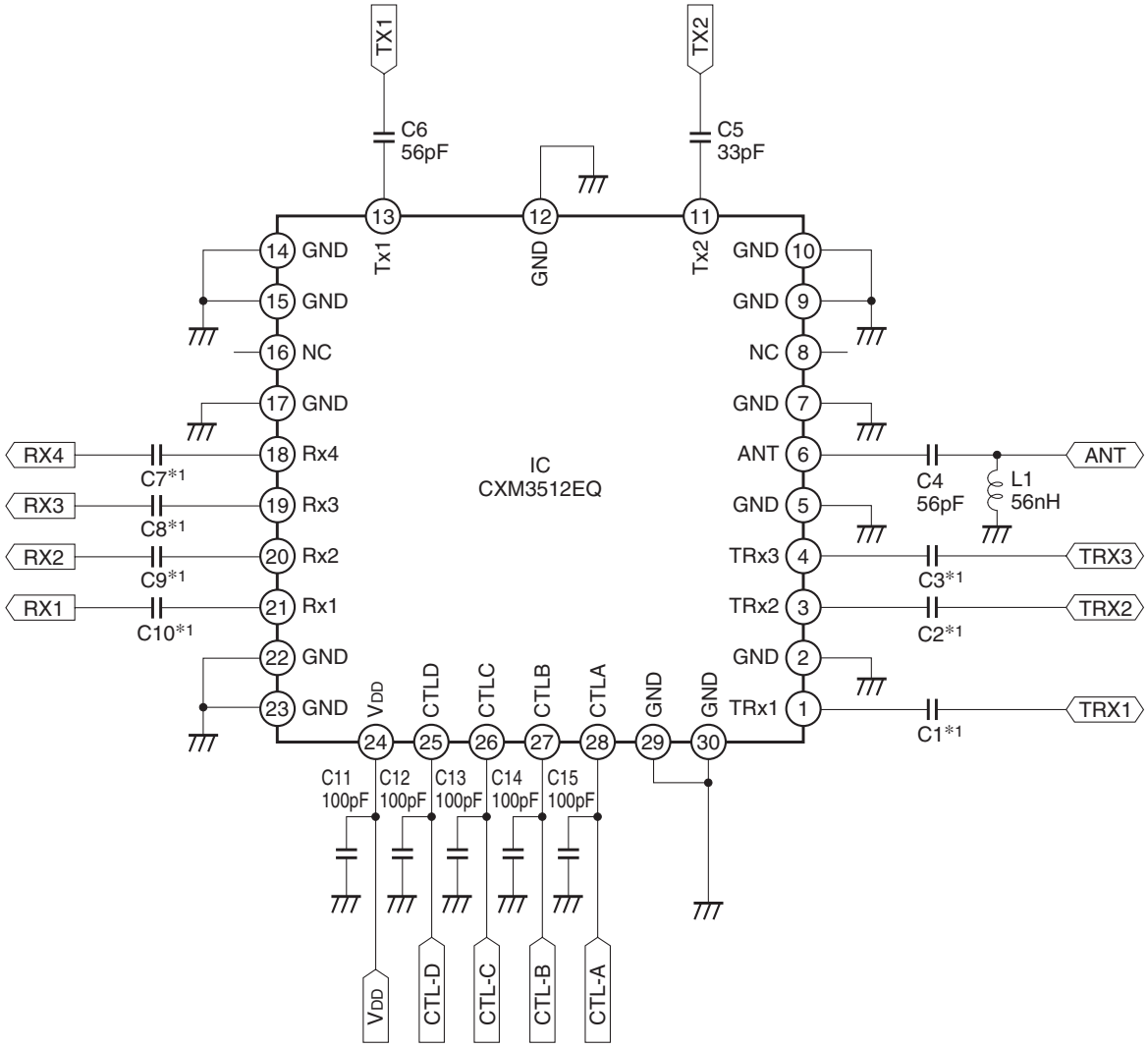
Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C)	High	1.5	2.65	3.3	V
	Low	0	—	0.3	

Current consumption

(Ta = 25℃)

Item	Condition	Min.	Typ.	Max.	Unit
Bias current	V_{DD} = 2.65V	—	100	130	μA
Control current	Vctl (H) = 2.65V/1-wire	—	2	5	

Recommended Circuit 1
GSM (4 bands)/UMTS (3 bands)

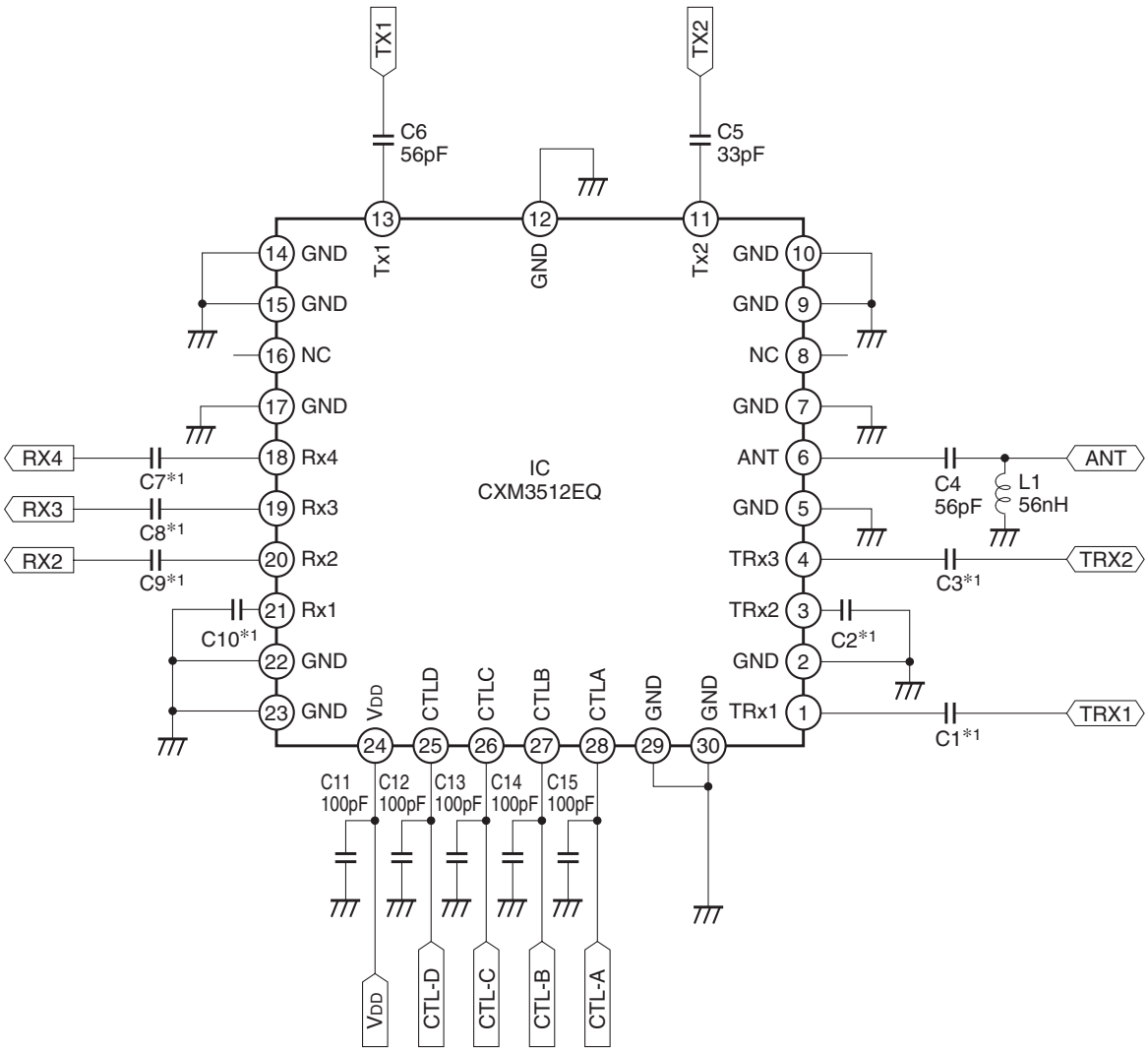


*1 Capacitors are required on all RF ports for DC blocking.
Recommended capacitance is as follows.
56pF for 800 to 960MHz signal
33pF for 1700 to 2200MHz signal

*2 C11 to C15 are not mandatory.

*3 L1 inductor (56nH) is recommended on Ant port for ESD protection.

Recommended Circuit 2
GSM (3 bands)/UMTS (2 bands)



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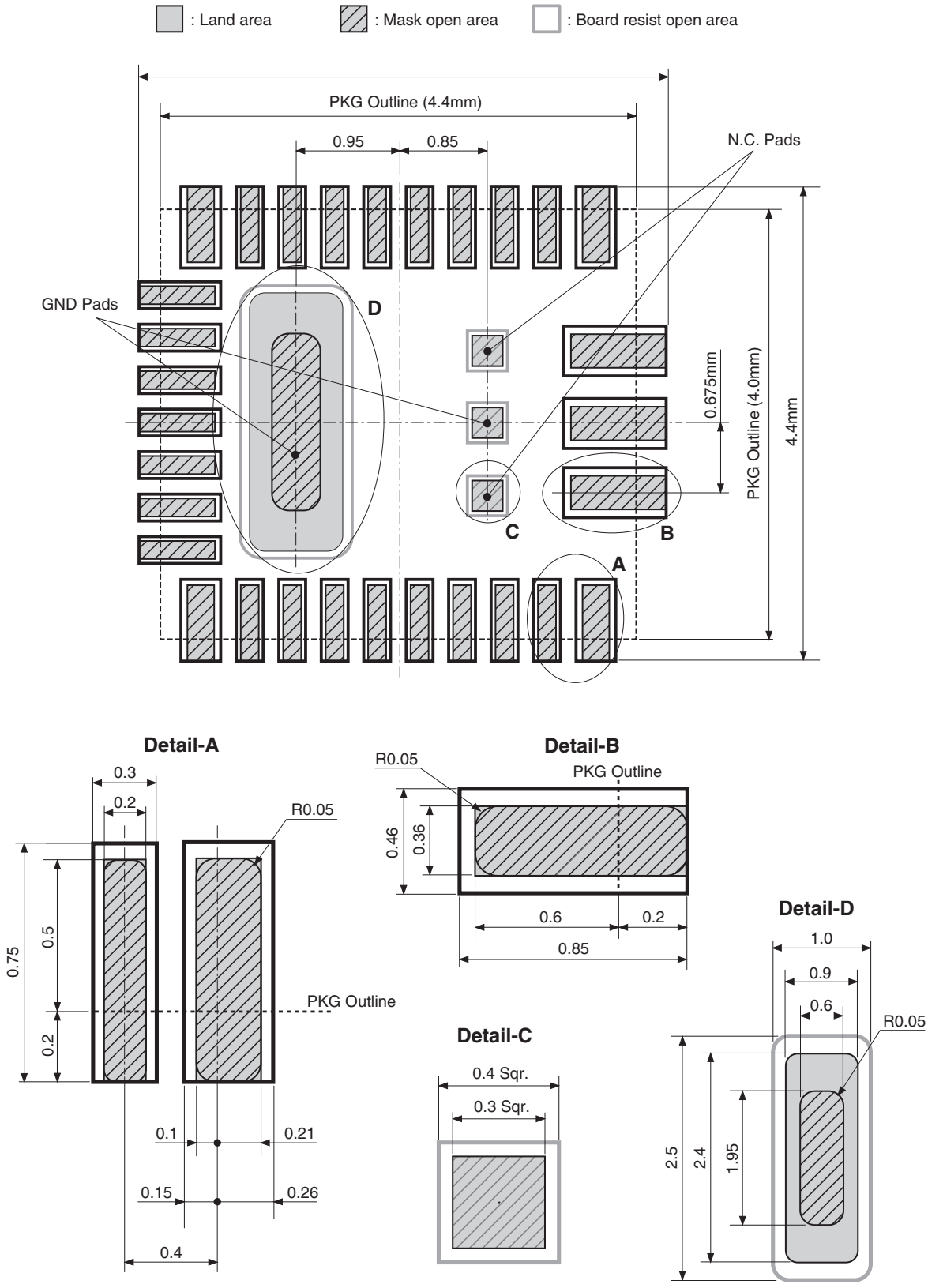
Recommended capacitance is as follows.
56pF for 800 to 960MHz signal
33pF for 1700 to 2200MHz signal

*2 C11 to C15 are not mandatory.

*3 L1 inductor (56nH) is recommended on Ant port for ESD protection.

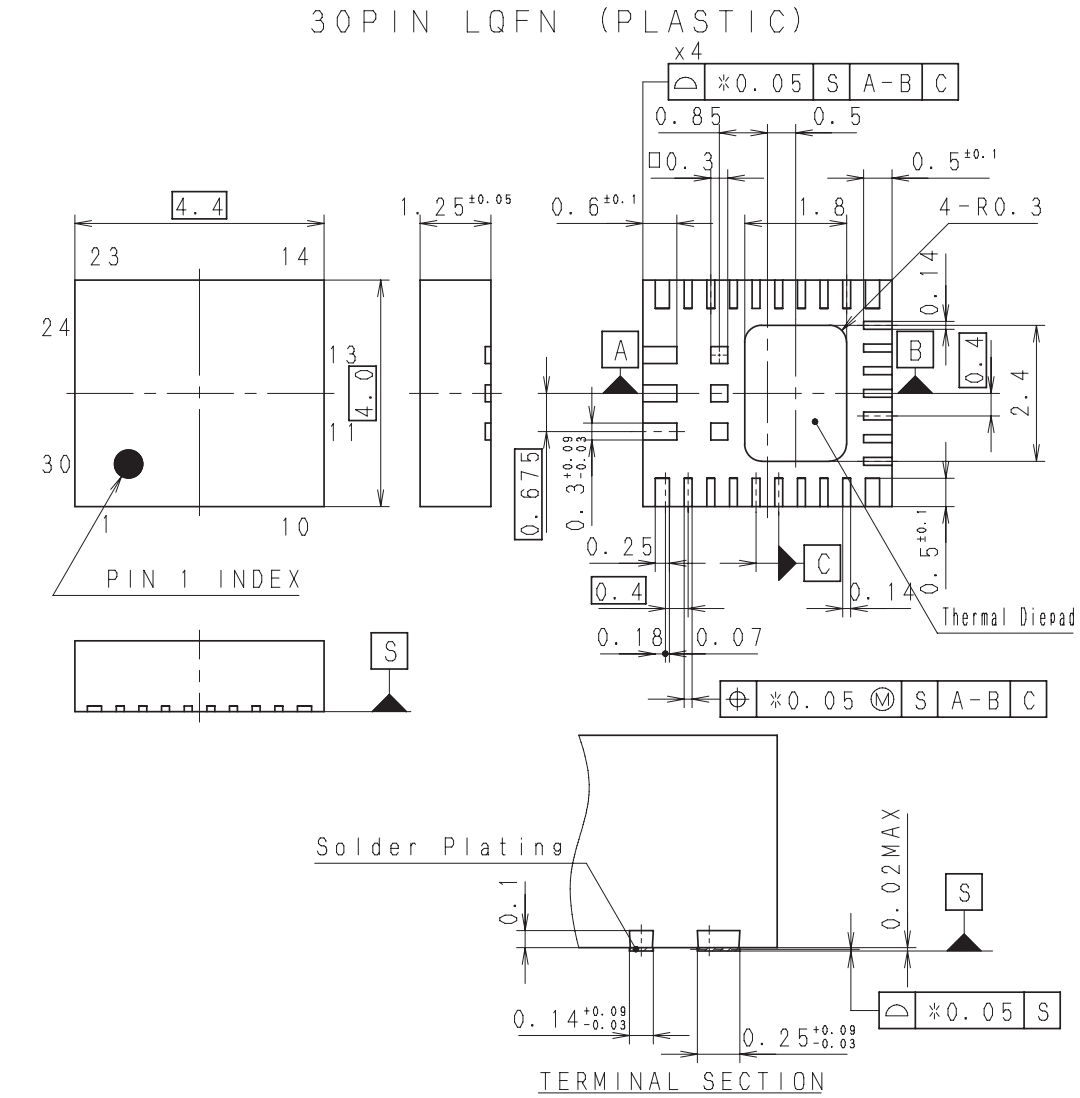
Pad Design

(Unit: mm)



Package Outline

(Unit: mm)



Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	LQFN-30P-01
JEITA CODE	————
JEDEC CODE	————

AP-4000-30013S Rev.0

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm