

# TC74HC597AP, TC74HC597AF

## 8-Bit Latch/Shift Register

The TC74HC597A is a high speed CMOS 8-BIT PARALLEL-IN/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of an 8-bit data register feeding an 8-bit shift register. The parallel data on the A to H inputs is stored in the input register on the positive going transition of RCK.

When the  $\overline{\text{SLOAD}}$  input is held low, the input register data is passed into the shift registers. When  $\overline{\text{SLOAD}}$  input is held high, the serial data input (SI) is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK.

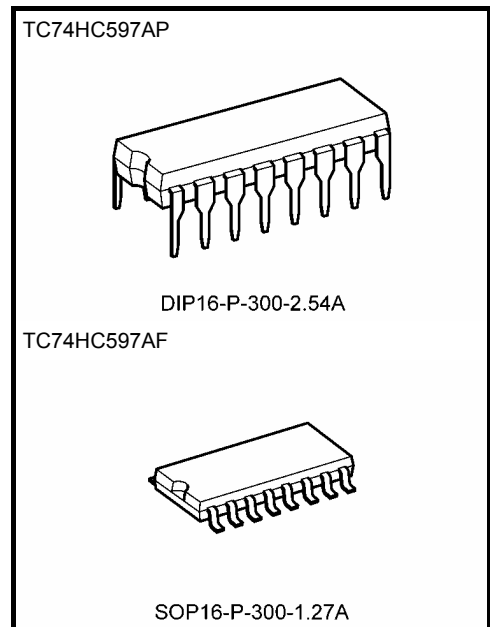
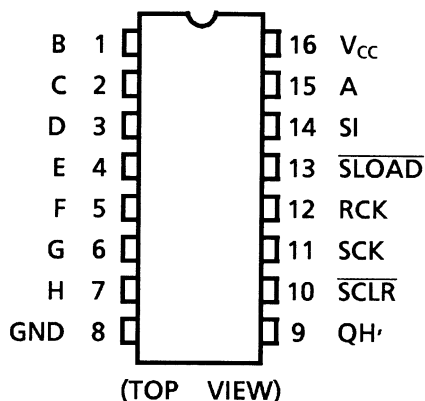
A direct clear input ( $\overline{\text{SCLR}}$ ) sets the 8-bit shift register to zero.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

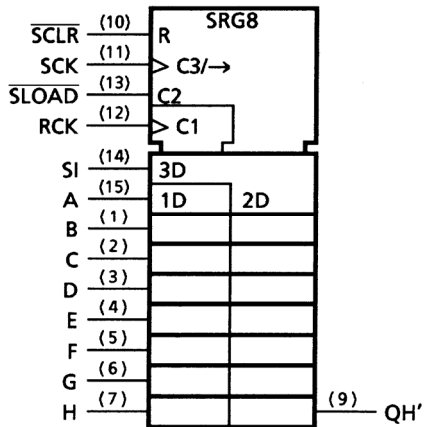
- High speed:  $f_{\text{max}} = 60 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC}} (\text{opr}) = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS597

### Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

## IEC Logic Symbol

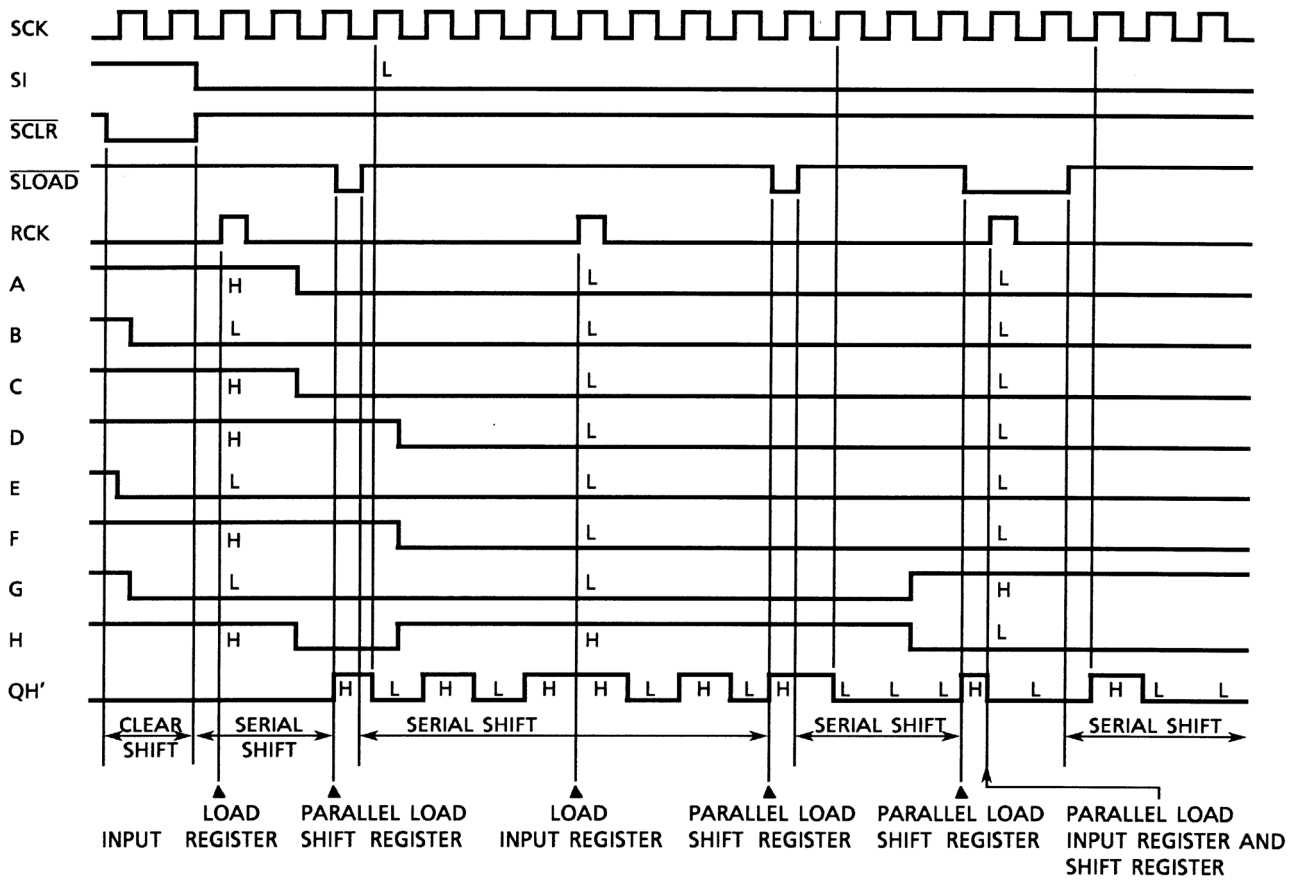


## Truth Table

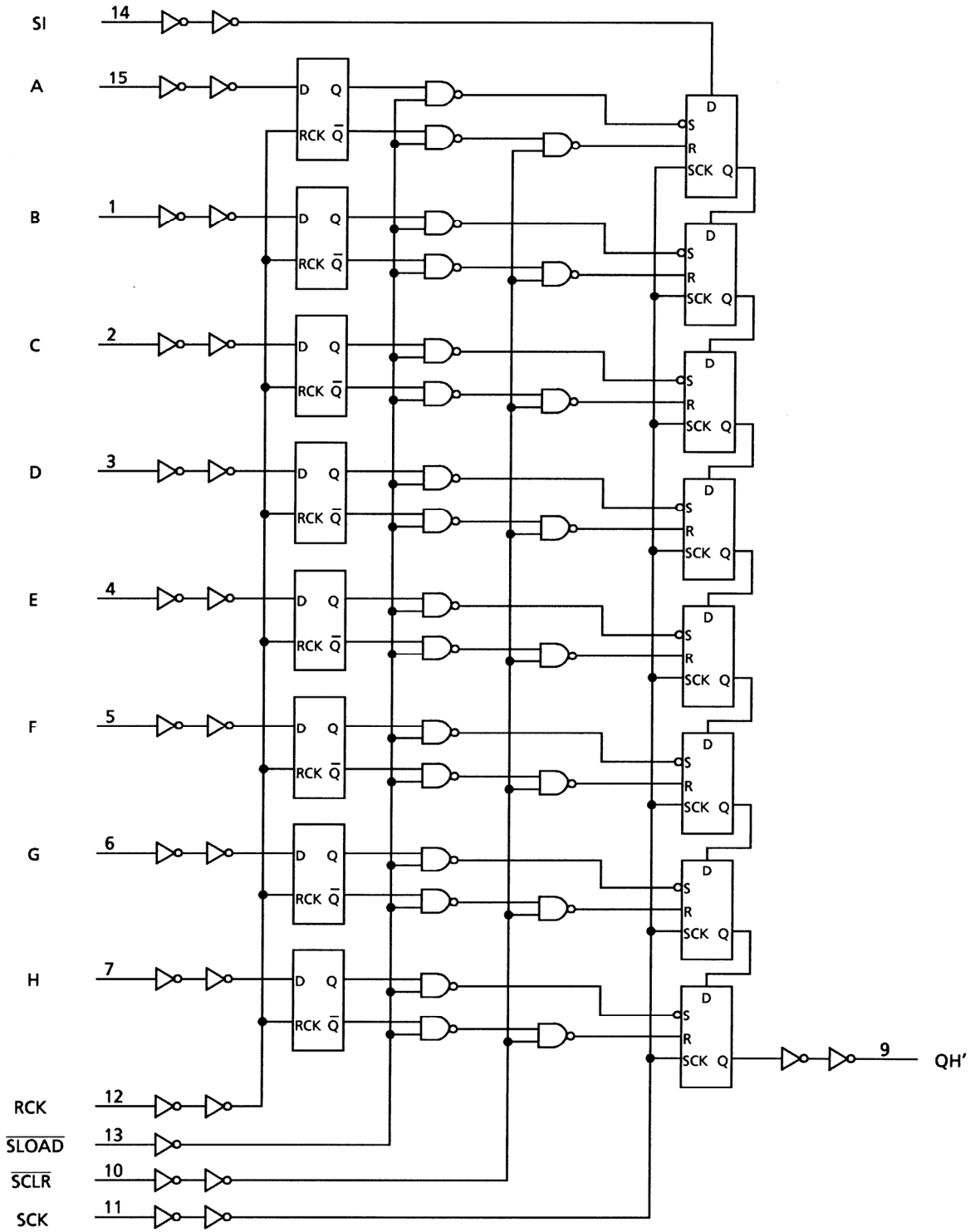
Inputs					Function
SI	SCK	$\overline{\text{SCLR}}$	$\overline{\text{SLOAD}}$	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S.R.
L		H	H	X	First stage of S.R. become "L". Other stages store the data of previous stage, respectively.
H		H	H	X	First stage of S.R. become "H". Other stages store the data of previous stage, respectively.
X		H	H	X	State of S.R. is not changed.
X	X	X	X		Input data on A to H line is stored into input register.
X	X	X	X		Storage register stage is not changed.

X: Don't care

**Timing Chart**



**System Diagram**



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
				I <sub>OH</sub> = -5.2 mA	4.5	4.18	4.31	—	4.13	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
				I <sub>OL</sub> = 5.2 mA	4.5	—	0.17	0.26	—	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA
				6.0	—	—	4.0	—	40.0	μA

## Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit	
			V <sub>CC</sub> (V)	Typ.	Limit		
Minimum pulse width (SCK, RCK)	$t_W$ (H) $t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{SCLR}}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{SLOAD}}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (RCK- $\overline{\text{SLOAD}}$ )	$t_s$	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (SI-SCK)	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (PI-RCK)	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ( $\overline{\text{SCLR}}$ , $\overline{\text{SLOAD}}$ )	$t_{rem}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

## AC Characteristics ( $C_L = 15$ pF, $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	5	8	ns
	$t_{THL}$					
Propagation delay time (SCK-QH')	$t_{pLH}$	—	—	16	25	ns
	$t_{pHL}$					
Propagation delay time ( $\overline{\text{SCLR}}$ -QH')	$t_{pHL}$	—	—	20	32	ns
Propagation delay time ( $\overline{\text{SLOAD}}$ -QH')	$t_{pLH}$ $t_{pHL}$	—	—	18	30	ns
Propagation delay time (RCK-QH')	$t_{pLH}$ $t_{pHL}$	$\overline{\text{SLOAD}} = \text{"L"}$	—	25	37	ns
Clock frequency	$f_{max}$	—	30	59	—	MHz

## AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	32	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (SCK-QH')	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	78	145	—	180	ns
			4.5	—	20	29	—	36	
			6.0	—	16	25	—	31	
Propagation delay time (SCLR-QH')	t <sub>pHL</sub>	—	2.0	—	90	175	—	220	ns
			4.5	—	24	35	—	44	
			6.0	—	20	30	—	37	
Propagation delay time (SLOAD-QH')	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	80	175	—	220	ns
			4.5	—	22	35	—	44	
			6.0	—	18	30	—	37	
Propagation delay time (RCK-QH')	t <sub>pLH</sub> t <sub>pHL</sub>	SLOAD = "L"	2.0	—	112	210	—	265	ns
			4.5	—	30	42	—	53	
			6.0	—	24	36	—	45	
Maximum clock frequency	f <sub>max</sub>	—	2.0	6	12	—	5	—	MHz
			4.5	30	48	—	24	—	
			6.0	35	50	—	28	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	60	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

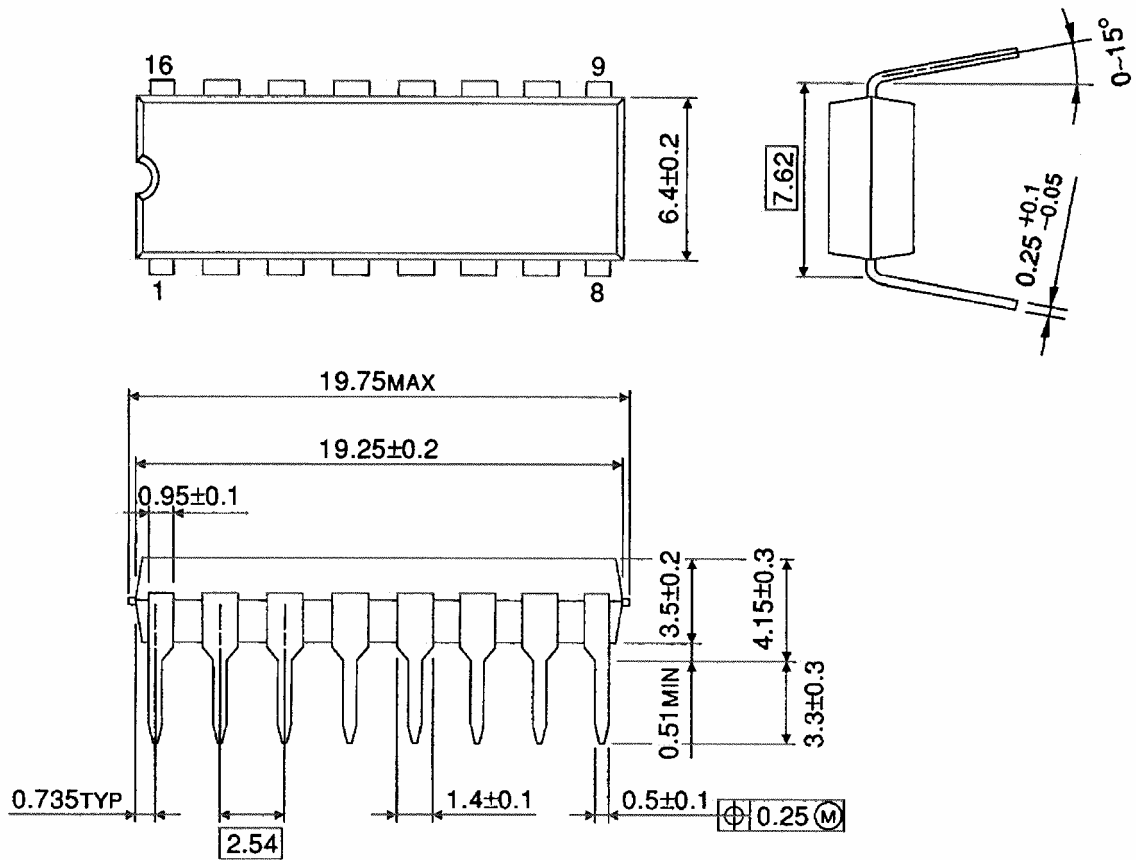
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

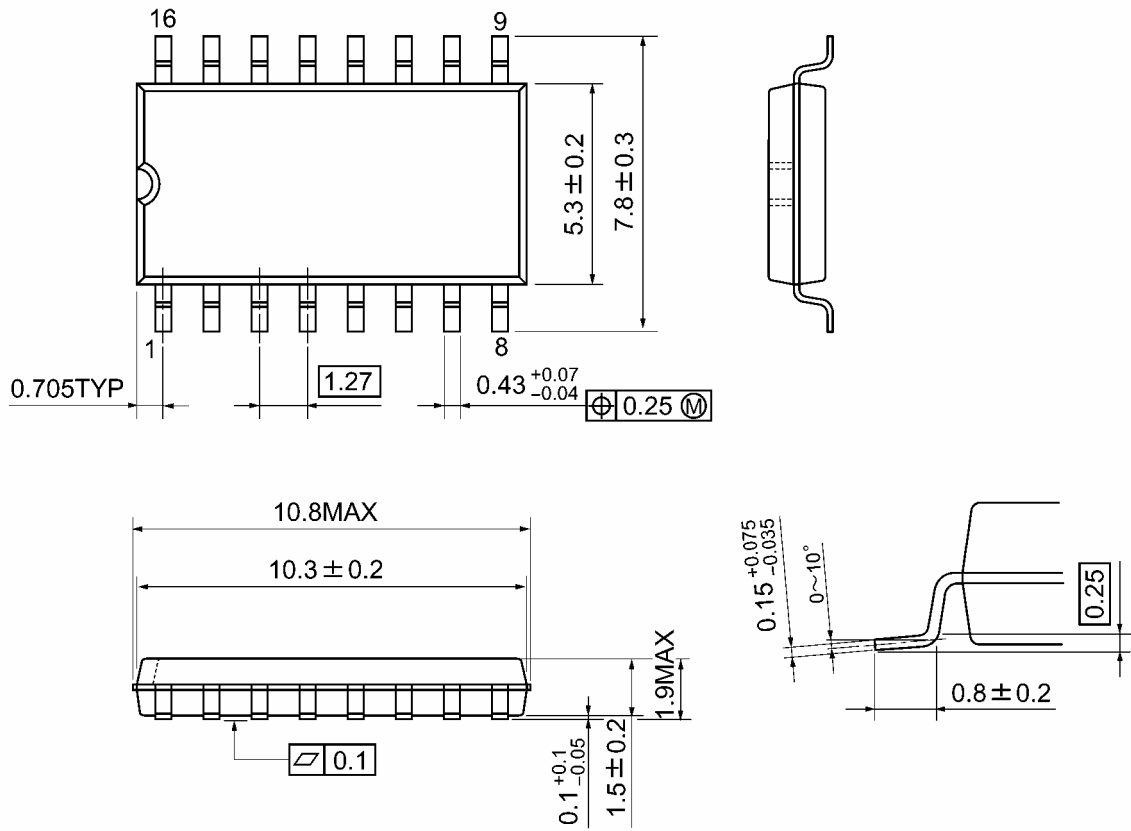


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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20070701-EN GENERAL

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