TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4020AP,TC74HC4020AF,TC74HC4020AFN
TC74HC4040AP,TC74HC4040AF,TC74HC4040AFN

TC74HC4020AP/AF/AFN 14-Stage Binary Counter

TC74HC4040AP/AF/AFN 12-Stage Binary Counter

Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74HC4020A/TC74HC4040A are high speed CMOS BINARY COUNTER/DIVIDERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operetion similar to equivalent LSTTL while maintaining the CMOS dissipation.

The TC74HC4020A is a 14-STAGE BINARY COUNTER, and the TC74HC4040A is a 12-STAGE BINARY COUNTER.

Setting CLR to high resets the counter to low.

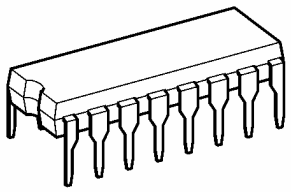
A negative transition on the CK input brings one increment into the counter.

The TC74HC4020A provides 12 divided outputs: 1'st stage and stage 4 thru stage 14. At Q14, a 1/16384 divided frequency will be output.

The TC74HC4040A provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

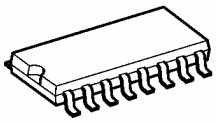
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC4020AP, TC74HC4040AP



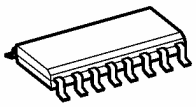
DIP16-P-300-2.54A

TC74HC4020AF, TC74HC4040AF



SOP16-P-300-1.27A

TC74HC4020AFN, TC74HC4040AFN



SOL16-P-150-1.27

Weight

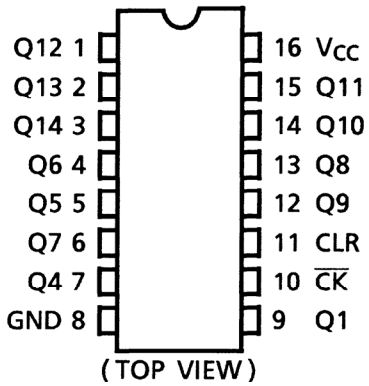
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

Features

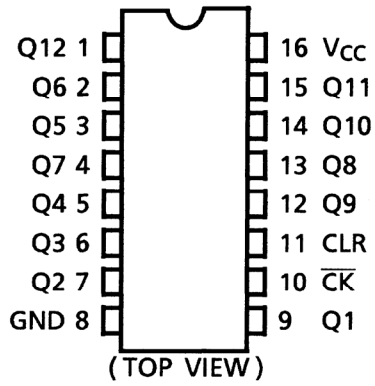
- High speed: f_{max} = 73 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2~6 V
- Pin and function compatible with 4020B/4040B

Pin Assignment

TC74HC4020A

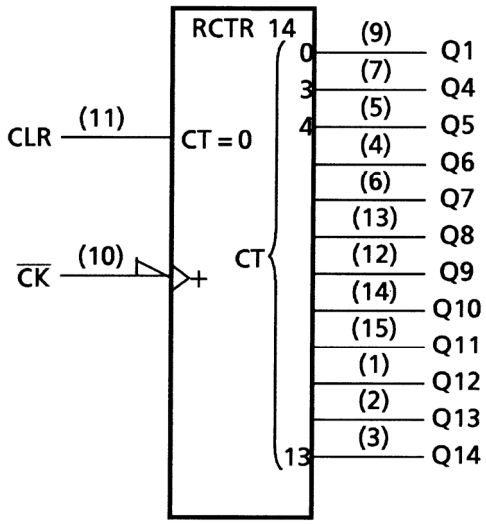


TC74HC4040A

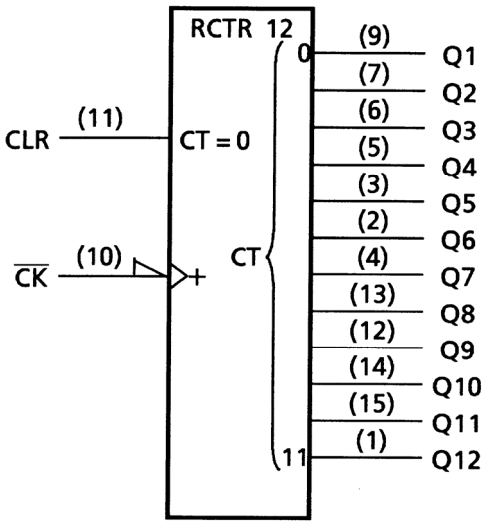


IEC Logic Symbol

TC74HC4020A



TC74HC4040A



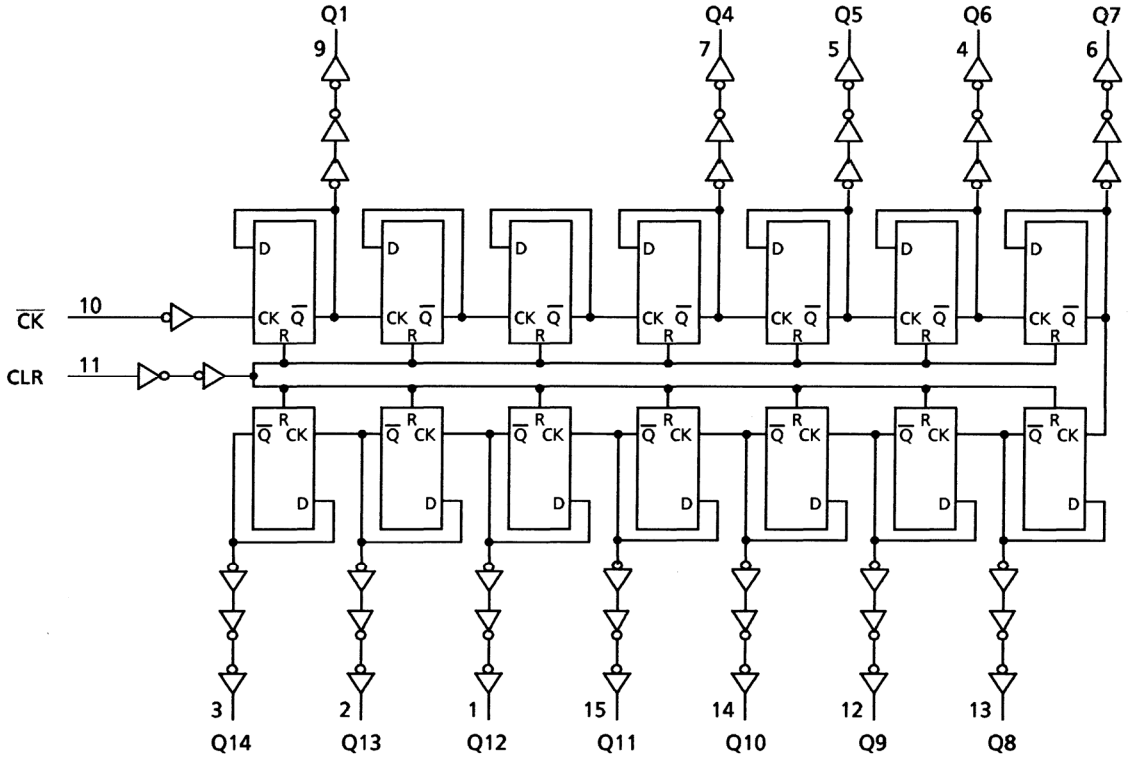
Truth Table

$\overline{CK}$	CLR	Output State
X	H	All Output = “L”
↑	L	No Change
↓	L	Adovance to Next State

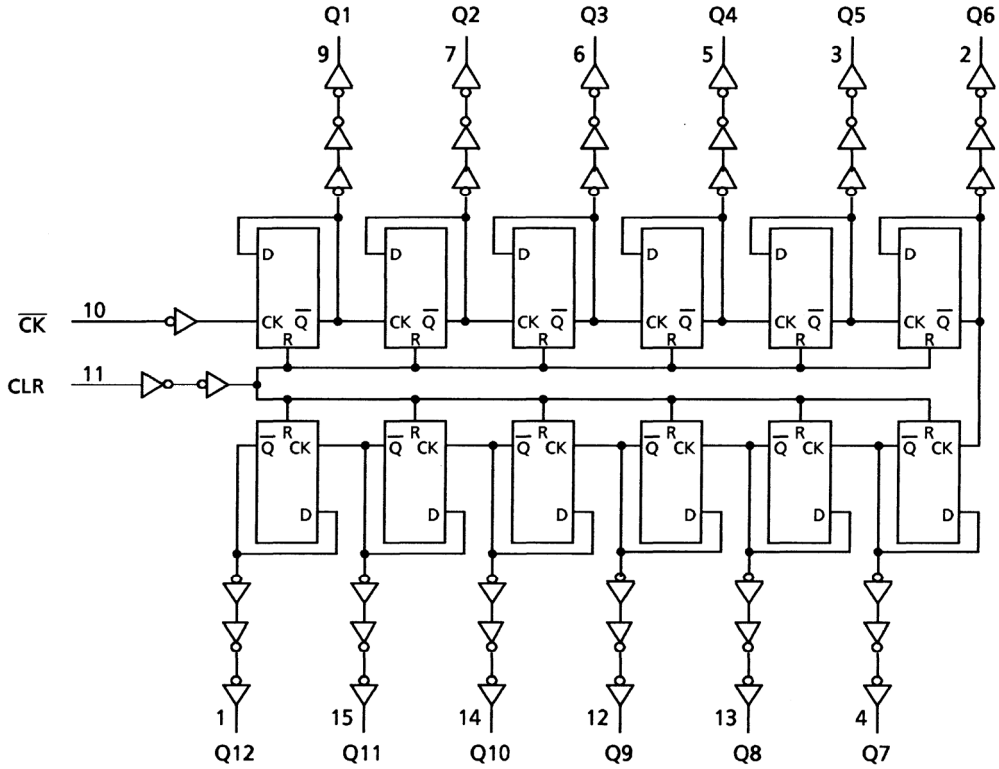
X: Don’t care

System Diagram

TC74HC4020A



TC74HC4040A



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7	V
DC input voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2~6	V
Input voltage	V_{IN}	0~V_{CC}	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	t_r, t_f	0~1000 (V_{CC} = 2.0 V) 0~500 (V_{CC} = 4.5 V) 0~400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40 ~85°C Limit	Unit
Minimum pulse width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width (CLR)	$t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum removal time	t_{rem}	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time ($\overline{CK}$ -Q1)	t_{pLH} t_{pHL}	—	—	16	24	ns
Propagation delay time (Qn-Qn + 1)	Δt_{pd}	—	—	5	14	ns
Propagation delay time (CLR)	t_{pHL}	—	—	14	24	ns
Maximum clock frequency	f_{max}	—	33	73	—	MHz

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time ($\overline{CK}$ -Q1)	t_{pLH} t_{pHL}	—	2.0	—	70	145	—	180	ns
			4.5	—	20	29	—	36	
			6.0	—	17	25	—	31	
Propagation delay time (Qn-Q + 1)	Δt_{pd}	—	2.0	—	20	75	—	95	ns
			4.5	—	6	15	—	19	
			6.0	—	4	13	—	16	
Propagation delay time (CLR)	t_{pHL}	—	2.0	—	55	140	—	175	ns
			4.5	—	17	28	—	35	
			6.0	—	14	24	—	30	
Maximum clock frequency	f_{max}	—	2.0	6	17	—	5	—	MHz
			4.5	30	66	—	24	—	
			6.0	35	78	—	28	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	TC74HC4020A		—	27	—	—	—	pF
		TC74HC4040A		—	37	—	—	—	

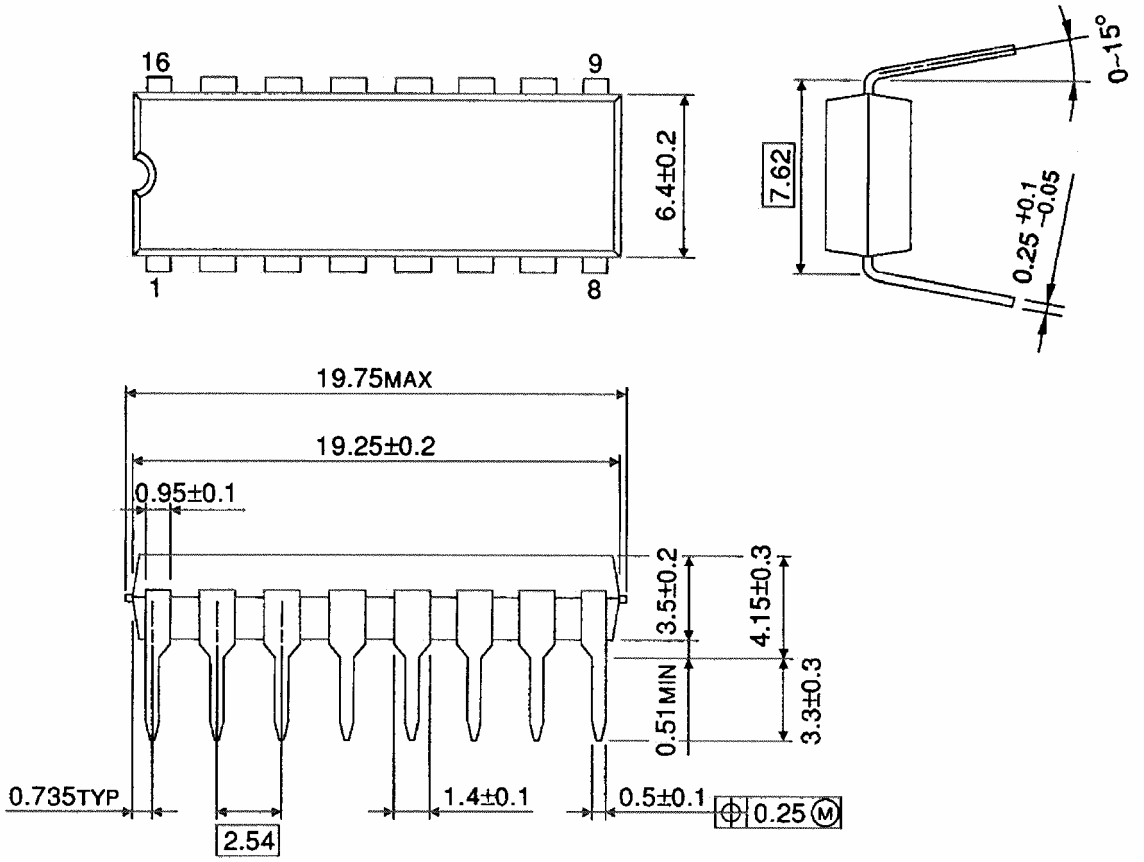
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

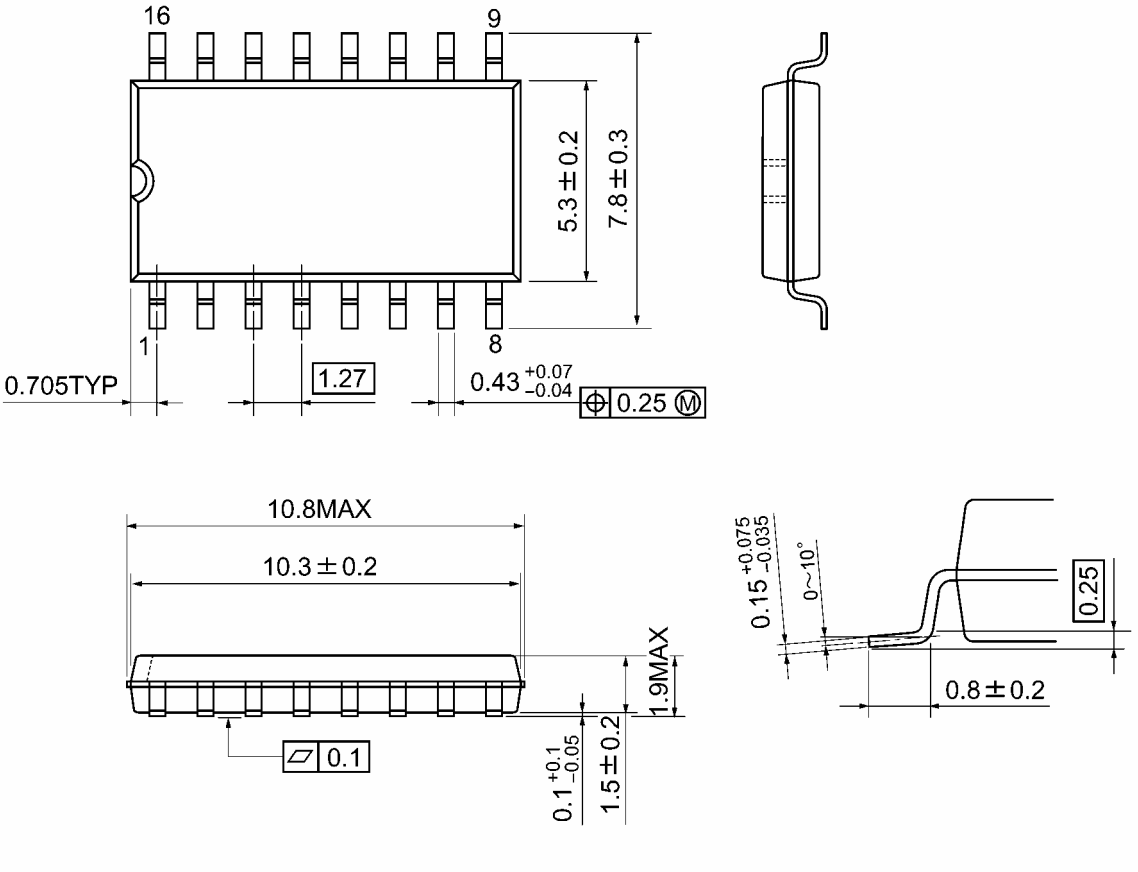
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

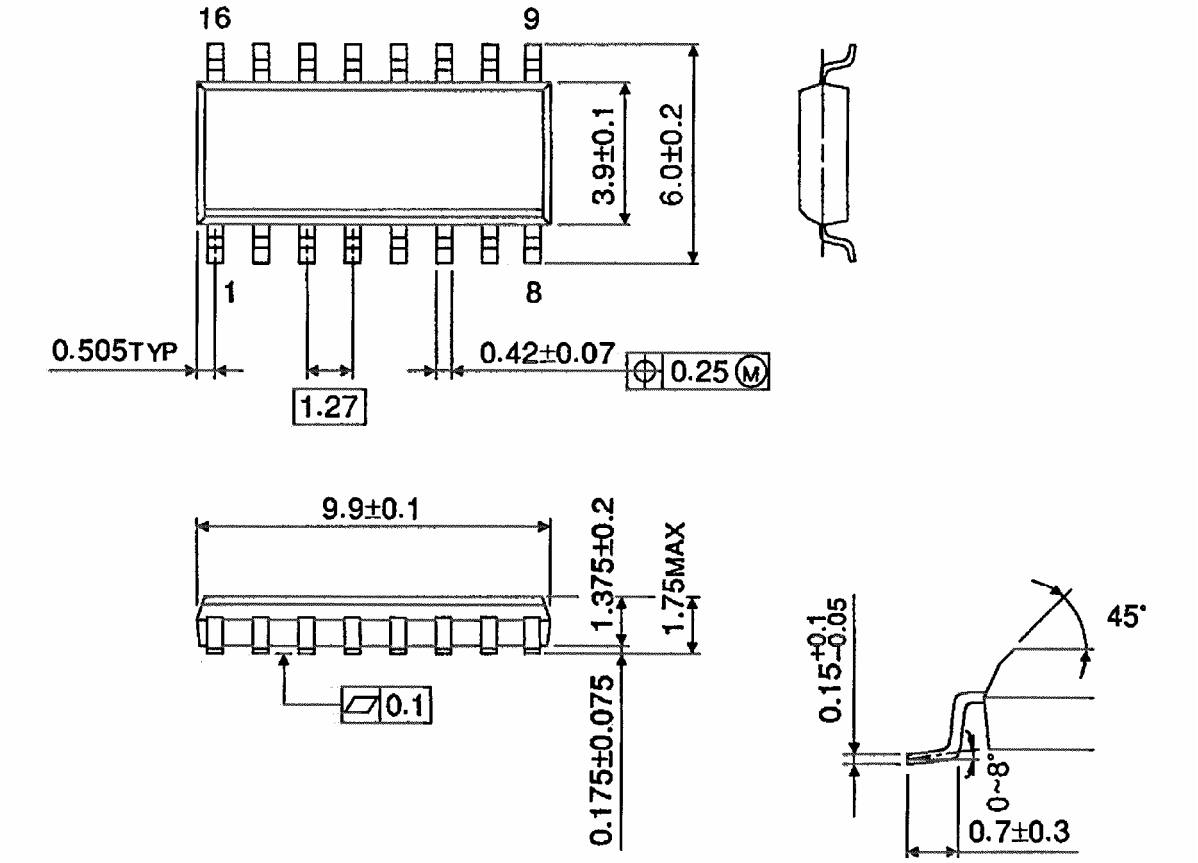
SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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