TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

# SSM3J16CT

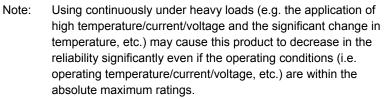
High Speed Switching Applications Analog Switch Applications

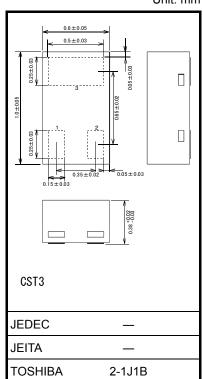
- Small package
- Low on-resistance : Ron
  - :  $R_{on} = 8 \Omega (max) (@V_{GS} = -4 V)$ :  $R_{on} = 12 \Omega (max) (@V_{GS} = -2.5 V)$

 $R_{on} = 45 \Omega (max) (@V_{GS} = -1.5 V)$ 

#### Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V <sub>DS</sub>	-20	V	
Gate-Source voltage		V <sub>GSS</sub>	±10	V	
Drain current	DC	۱ <sub>D</sub>	-100	mA	
	Pulse	I <sub>DP</sub>	-200		
Drain power dissipation (Ta = $25^{\circ}$ C)		P <sub>D</sub> (Note 1)	100	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	





Weight :0.75mg

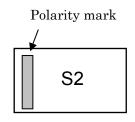
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board (10 mm  $\times$  10 mm  $\times$  1.0 t, Cu Pad: 100 mm<sup>2</sup>)

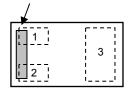
Marking (Top View)

Pin Condition (Top View)





Polarity mark (on the top)





- 2. Source
- 3. Drain
- \*Electrodes: On the bottom

### **Handling Precaution**

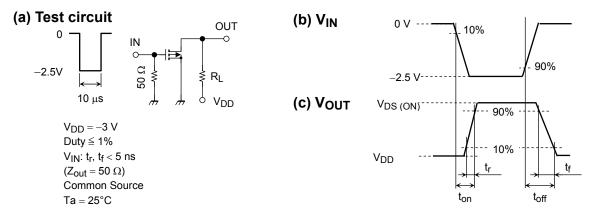
When handling individual devices that are not yet mounted on a circuit board, ensure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Unit: mm

**Electrical Characteristics (Ta = 25°C)** 

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT	
Gate leakage current		I <sub>GSS</sub>	$V_{GS}=\pm 10~V,~V_{DS}=0$	—	_	±1	μA	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-20			V	
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0$	_		-1	μA	
Gate threshold voltage		V <sub>th</sub>	$V_{DS} = -3 \text{ V}, \text{ I}_{D} = -0.1 \text{ mA}$	-0.6		-1.1	V	
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = -3 \text{ V}, \text{ I}_{D} = -10 \text{ mA}$	25			mS	
Drain-Source on-resistance		R <sub>DS (ON)</sub>	$I_D = -10$ mA, $V_{GS} = -4$ V	_	6	8	Ω	
			$I_{D} = -10$ mA, $V_{GS} = -2.5$ V	_	8	12		
			$I_D = -1 \text{ mA}, V_{GS} = -1.5 \text{ V}$	_	18	45		
Input capacitance		C <sub>iss</sub>		_	11		pF	
Reverse transfer capacitance		C <sub>rss</sub>	$V_{DS} = -3 \text{ V}, \text{ V}_{GS} = 0, \text{ f} = 1 \text{ MHz}$	_	3.7		pF	
Output capacitance		C <sub>oss</sub>			10		pF	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -3 V, I <sub>D</sub> = - 10 mA,	—	130		ns	
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0 \sim -2.5 V$	_	190			

### **Switching Time Test Circuit**

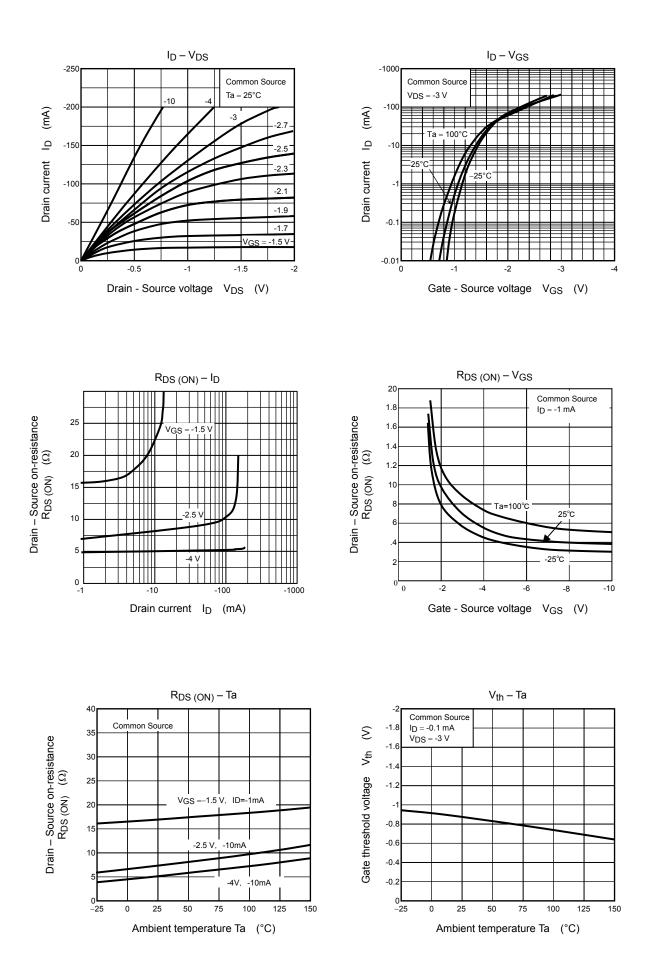


#### Precaution

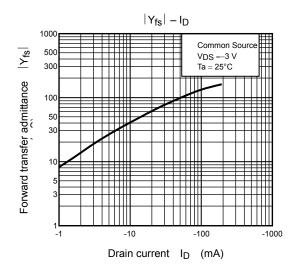
 $V_{th}$  can be expressed as the voltage between the gate and source when the low operating current value is  $I_D = 100 \ \mu A$  for this product. For normal switching operation,  $V_{GS}$  (on) requires a higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS}$  (off) <  $V_{th}$  <  $V_{GS}$  (on).) Bo sure to take this into consideration when using the device

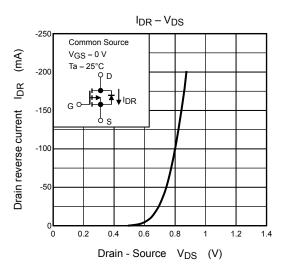
Be sure to take this into consideration when using the device.

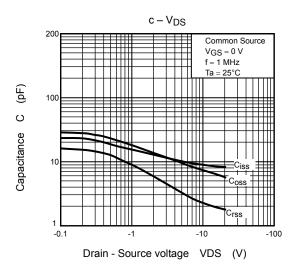
# **TOSHIBA**

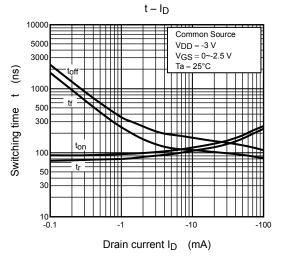


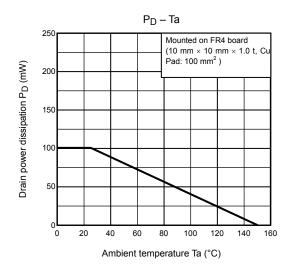
## **TOSHIBA**











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20070701-EN GENERAL

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