SC1210
High Speed, 12 V, Synchronous Power MOSFET Driver

Description

The SC1210 is a high speed, dual output driver designed to drive high-side and low-side MOSFETs in a synchronous Buck converter. These drivers can work with many Semtech PWM controllers to provide a cost effective multi-phase voltage regulator for advanced microprocessors.

A 30ns max propagation delay from input transition to the gate of the power FET's guarantees operation at high switching frequencies. Internal overlap protection circuit prevents shoot-through from Vin to PGND in the main and synchronous MOSFETs. The adaptive overlap protection circuit ensures the bottom FET does not turn on until the top FET source has reached 1V, to prevent cross-conduction.

8.5V gate drive provides optimum enhancement of MOSFETs at minimum driver and MOSFET switching loss. High current drive capability allows fast switching, thus reducing switching losses at high (up to 1.5MHz) frequencies without causing thermal stress on the driver.

Under-voltage-lockout and over-temperature shutdown features are included for proper protection and safe operation. Timed latches and improved robustness are built into the safty functions such as the Under Voltage Lockout and adaptive Shoot-through protection circuitry to prevent false triggering. The SC1210 is offered in a standard SO-8 package.

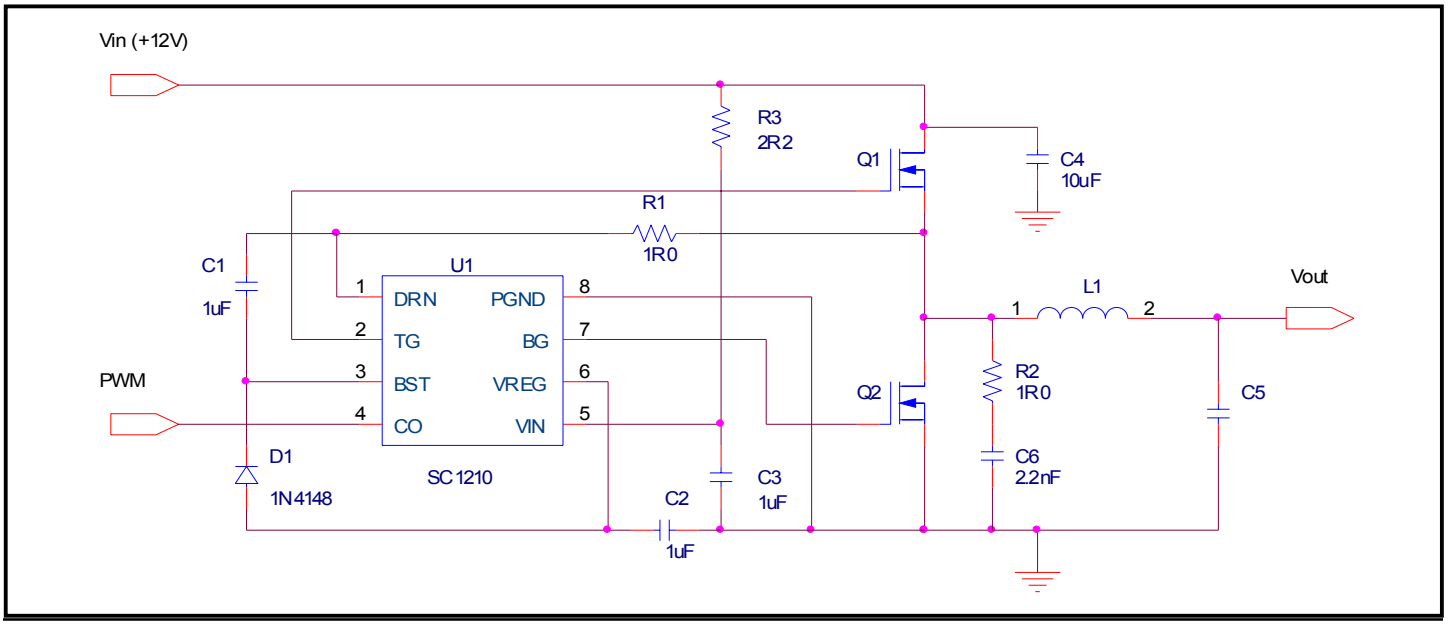
Features

- High efficiency
- +12V supply voltage with internal LDO for optimum gate drive
- High peak drive current
- Adaptive non-overlapping gate drives provide shoot-through protection
- Fast rise and fall times (15ns typical with 3000pf load)
- Ultra-low (<30ns) propagation delay (BG going low)
- Floating top gate drive
- Crowbar function for over voltage protection
- High frequency (to 1.5 MHz) operation allows use of small inductors and low cost ceramic capacitors
- Under-voltage-lockout
- Low quiescent current

Applications

- Intel Pentium™ processor power supplies
- AMD Athlon™ and K8™ processor power supplies
- High current low voltage DC-DC converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V_{IN} Supply Voltage	V_{IN}		16	V
BST to DRN	$V_{BST-DRN}$		11	V
BST to PGND	$V_{BST-PGND}$		40	V
BST to PGND Pulse	$V_{BST-PULSE}$	t_{PULSE} < 100ns	45	V
DRN to PGND	$V_{DRN-PGND}$		-2 to 30	V
DRN to PGND Pulse	$V_{DRN-PULSE}$	t_{PULSE} < 200ns	-5 to 35	V
PWM Input	CO		-0.3 to 8.5	V
Thermal Resistance Junction to Case	θ_{JC}		40	°C/W
Operating Junction Temperature Range	T_J		0 to +125	°C
Storage Temperature Range	T_{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}		300	°C

Electrical Characteristics

Unless specified: T_A = 25°C; V_{IN} = 12V; V_{REG} = 8.5V

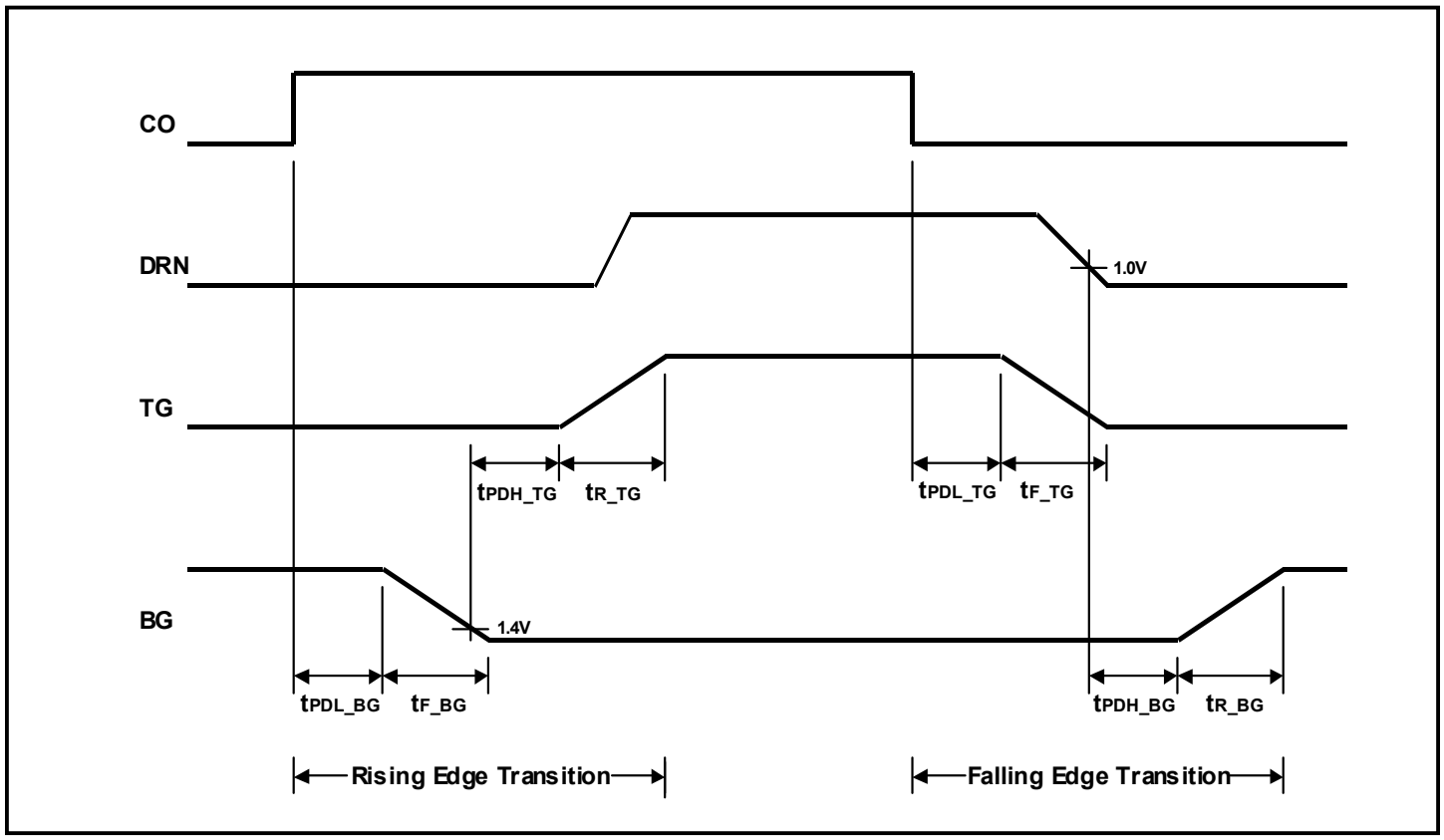
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{IN}		9	12	15	V
Quiescent Current, Operating	Iq_op			3.0		mA
Under Voltage Lockout						
Start Threshold of V_{REG} Voltage	V_{REG_START}			4	4.3	V
Hysteresis	$Vhys_{UVLO}$			160		mV
Internal LDO						
LDO Output	V_{REG}	V_{IN} = 9V to 16V		8.5		V
Drop Out Voltage	V_{DROP}	V_{IN} = 5V to 8.8V		0.3		V

Electrical Characteristics (Cont.)

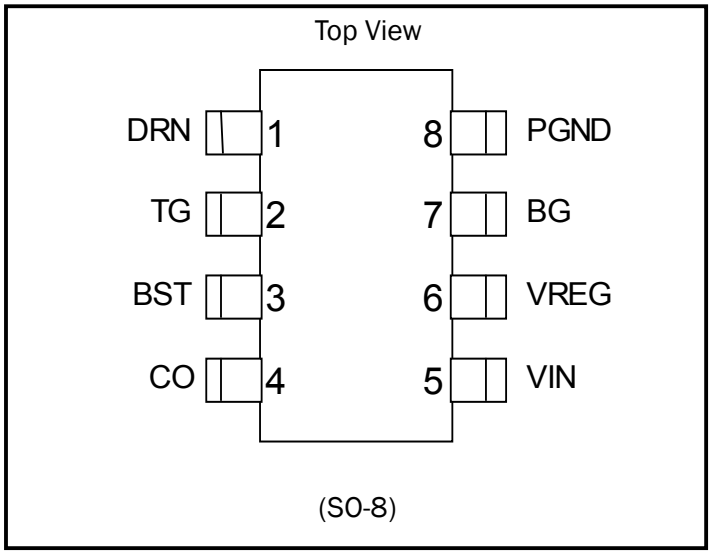
Unless specified: T_A = 25°C; V_{IN} = 12V; V_{REG} = 8.5V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CO						
Logic High Input Voltage	V_{CO_H}		2.0			V
Logic Low Input Voltage	V_{CO_L}				0.8	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			155		°C
Hysteresis	T_{HYST}			10		°C
High Side Driver (TG)						
Output Impedance	R_{SRC_TG}	V_{BST} - V_{DRN} = 8.5V		1.5	3.0	Ω
	R_{SINK_TG}			1.0	2.0	
Rise Time	t_{R_TG}	CL = 3nF, V_{BST} - V_{DRN} = 8.5V		15		ns
Fall Time	t_{F_TG}	CL = 3nF, V_{BST} - V_{DRN} = 8.5V		10		ns
Propagation Delay, TG Going High	t_{PDH_TG}	V_{BST} - V_{DRN} = 8.5V		37		ns
Propagation Delay, TG Going Low	t_{PDL_TG}	V_{BST} - V_{DRN} = 8.5V		30		ns
Low-Side Driver (BG)						
Output Impedance	R_{SRC_BG}	V_{BST} - V_{DRN} = 8.5V		1.5	3.0	Ω
	R_{SINK_BG}			1.5	3.0	
Rise Time	t_{R_BG}	CL = 3nF, V_{BST} - V_{DRN} = 8.5V		10		ns
Fall Time	t_{F_BG}	CL = 3nF, V_{BST} - V_{DRN} = 8.5V		10		ns
Propagation Delay, BG Going High	t_{PDH_BG}	V_{BST} - V_{DRN} = 8.5V		20		ns
Propagation Delay, BG Going Low	t_{PDL_BG}	V_{BST} - V_{DRN} = 8.5V		27		ns
Under-Voltage-Lockout Time Delay						
V_{REG} ramping up	t_{PDH_UVLO}			2		µs
V_{REG} ramping down	t_{PDL_UVLO}			2		µs

Timing Diagrams



Pin Configuration



Ordering Information

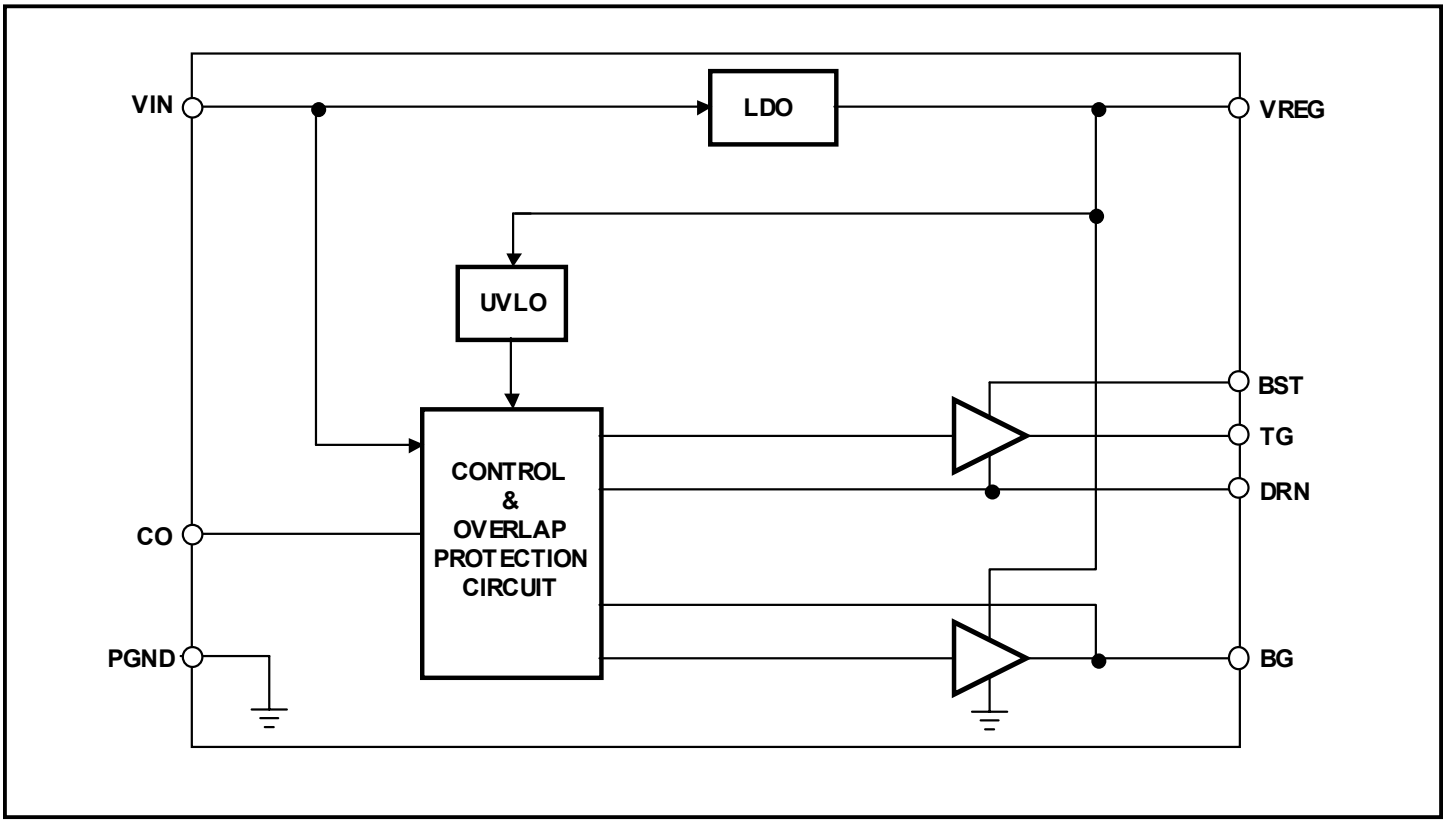
Device (1)	Package	Temp Range (T_J)
SC1210STR	SO-8	0° to 125°C

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	DRN	The drain node of the low-side MOSFET (or switching node) of the synchronous buck converter.
2	TG	Output gate drive for the switching (top) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically 1µF (ceramic).
4	CO	Logic level PWM input signal to the SC1210 supplied by external controller. An internal 50kohm resistor is connected from this pin to PGND.
5	VIN	Supply power for LDO. Connect to input power rail of the converter.
6	VREG	LDO output. Decouple with 1µF to 4.7µF (ceramic) with lead length no more than 0.2" (5mm).
7	BG	Output gate drive for the synchronous (bottom) MOSFET.
8	PGND	Ground. Keep this pin close to the synchronous MOSFETs source.

Block Diagram



Applications Information

THEORY OF OPERATION

The SC1210 is a high speed, dual output driver designed to drive top and bottom MOSFETs in a synchronous Buck converter. It features adaptive delay for shoot-through protection, VID-on-Fly operation, and internal LDO for optimum gate drive voltage. These drivers combined with variety of Semtech PWM controllers form multi-phase voltage regulators for advanced microprocessors.

UVLO

A supply voltage has to be applied to VIN pin of the SC1210. The top and bottom gates are held low until VIN exceeds UVLO threshold of the driver. Then the top gate remains low and the bottom gate is pulled high to turn on the bottom FET.

Gate Transition and Shoot Through Protection

Refer to the timing diagrams section, the rising edge of the PWM input initiates the bottom FET turn-off and the top FET turn-on. After a short propagation delay (t_{PDL_BG}), the bottom gate begins to fall (t_{F_BG}). An adaptive circuit in the SC1210 monitors the bottom gate voltage to drop below 1.4V. Then after a preset delay time (t_{PDH_TG}) is expired, the top gate turns on. The delay time is set to be 20ns typically. This prevents the top FET from turning on until the bottom FET is off. During the transition, the inductor current is freewheeling through the body diode of either bottom FET or top FET, upon the direction of the inductor current. The phase node could be low (ground) or high (VIN).

The falling edge of the PWM input controls the top FET turn-off and the bottom FET turn-on. After a short propagation delay (t_{PDL_TG}), the top gate begins to fall (t_{F_TG}). As the inductor current is commutated from the top FET to the body diode of the bottom FET, the phase node begins to fall. The adaptive circuit in the SC1210 detects the phase node voltage. It holds the bottom FET off until the phase node voltage has dropped below 1.0V. This prevents the top and bottom FETs from conducting simultaneously or shoot-through.

VID-on-Fly Operation

Certain new processors have required to changing the VID dynamically during the operation, or refered as VID-on-Fly operation. A VID-on-Fly can occur under light load or heavy load conditions. At light load, it could force the converter to sink current. Upon turn-off of the top FET, the reversed inductor current has to be freewheeling through the body diode of the top FET instead of the bottom FET. As a result, the phase node voltage remains high. The SC1210 incorporates the ability by pulling the bottom gate to high internally, which over rides the adaptive circuit and turns the bottom FET on. The delay time from the PWM falling egde to the bottom gate turn-on is set at 200ns typically.

Optimized Gate Drive Voltage

With the supply voltage in between 9V to 16V, an internal LDO is designed with the SC1210 to bring the voltage to a lower level for gate drive. An external Ceramic capacitor(1uF to 4.7uF) connected in between Vreg to ground is needed to decouple the LDO. The LDO output powers up the low gate driver, and the high gate drive is powered by the external bootstrap circuit. The LDO output voltage is set at 8.5V. The manufacture data and bench tested results show that, for low R_{dson} FETs run at applied load current, the optimum gate drive voltage is around 8.5V, where the total power losses of power FETs, including conduction loss, switching loss, and the gate drive loss, are minimized.

Thermal Shut Down

The SC1210 will shut down by pulling both driver outputs low if its junction temperature, T_j, exceeds 155°C.

COMPONENT SELECTION

Bootstrap Circuit

The SC1210 uses an external bootstrap circuit to provide a voltage for the top FET drive. This voltage, referring to the Phase Node, is held up by a bootstrap capacitor.

Typically, it is recommended to use a 1uF ceramic capacitor with 25V rating and a commonly available diode IN4148 for the bootstrap circuit. In addition, a small resistor may be added in between DRN of the SC1210 and the Phase Node. The resistor is used to allievate the stress of the SC1210 from exposing to the negative spike on the DRN pin. A negative spike could occur at

the Phase Node during the top FET turn-off due to parasitic inductance in the switching loop. The spike could be minimized with a careful PCB layout. In those applications with TO-220 package FETs, it is recommended to use a clamping diode on the DRN pin to mitigate the impact of the excessive phase node negative spike.

Filters for Supply Power

For VREG pin of the SC1210, it is recommended to use a 1uF to 4.7uF, 25V rating ceramic capacitor for decoupling.

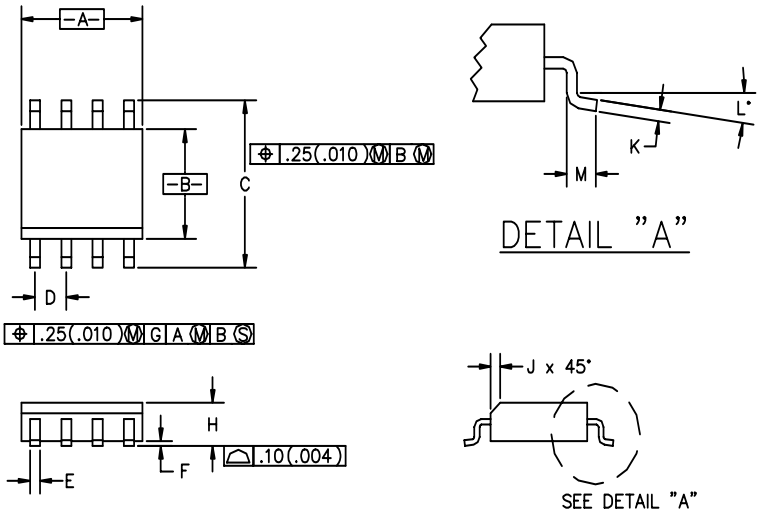
LAYOUT GUIDELINES

The switching regulator is a high di/dt power circuit. Its Printed Circuit Board (PCB) layout is critical. A good layout can achieve an optimum circuit performance while minimized the component stress, resulting in better system reliability. For a multi-phase voltage regulator, the SC1210 driver, FETs, inductor, and supply decoupling capacitors in each phase have to be considered to yield a proper PCB layout.

For the SC1210 driver, the following guidelines are typically recommended during PCB layout:

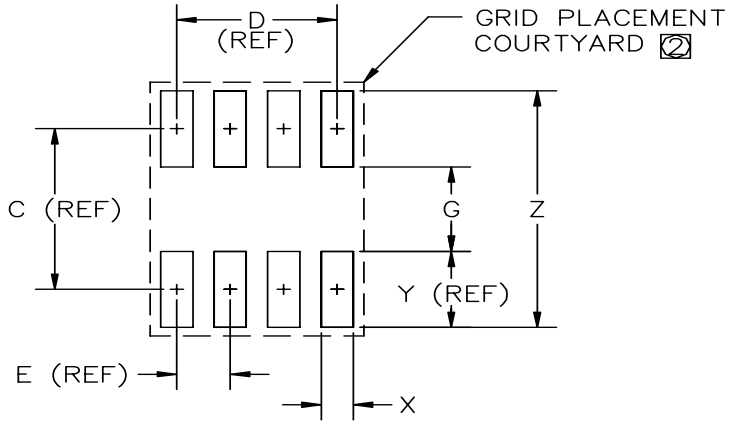
1. Place the SC1210 close to the FETs for shortest gate drive traces and ground return paths.
2. Connect bypass capacitors as close as possible to decoupling pins (VREG and VIN) and PGND. The trace length of the decoupling capacitor on VREG pin should be no more than 0.2” (5mm).
3. Locate the components of the bootstrap circuit close to the SC1210.
4. Provide a proper decoupling for the FETs to reduce the inductive kick seen by the DRN pin.

Outline Drawing - SOIC-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - SOIC-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.19	—	5.00	—
D	—	.15	—	3.81	—
E	—	.05	—	1.27	—
G	.10	.11	2.60	2.80	—
X	.02	.03	.60	.80	—
Y	—	.09	—	2.40	—
Z	—	.29	7.20	7.40	—

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

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