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RF5110G

3V GSM POWER AMPLIFIER

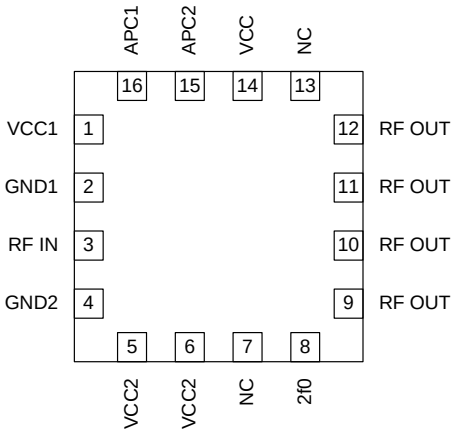
RoHS & Pb-Free Product
Package Style: QFN, 16-Pin, 3 x 3

Features

- Single 2.7V to 4.8V Supply Voltage
- +36dBm Output Power at 3.5V
- 32dB Gain with Analog Gain Control
- 57% Efficiency
- 800MHz to 950MHz Operation
- Supports GSM and E-GSM

Applications

- 3V GSM Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- GPRS Compatible
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- FM Radio Applications: 150MHz/220MHz/ 450MHz/865MHz/915MHz



Functional Block Diagram

Product Description

The RF5110G is a high-power, high-efficiency power amplifier module offering high performance in GSM OR GPRS applications. The device is manufactured on an advanced GaAs HBT process, and has been designed for use as the final RF amplifier in GSM hand-held digital cellular equipment and other applications in the 800MHz to 950MHz band. On-board power control provides over 70dB of control range with an analog voltage input, and provides power down with a logic “low” for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics. The RF5110G can be used together with the RF5111 for dual-band operation. The device is packaged in an ultra-small 3mmx3mmx1mm plastic package, minimizing the required board space.

Ordering Information

RF5110G	3V GSM Power Amplifier
RF5110GPCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage ($V_{APC1,2}$)	-0.5 to +3.0	V
DC Supply Current	2400	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temp=25°C, V_{CC}=3.6V, $V_{APC1,2}$=2.8V, P_{IN}=+4.5dBm, Freq=880MHz to 915MHz, 37.5% Duty Cycle, pulse width=1731µs
Operating Frequency Range		880 to 915		MHz	See evaluation board schematic.
Usable Frequency Range		800 to 950		MHz	Using different evaluation board tune.
Maximum Output Power	33.8	34.5		dBm	Temp=25°C, V_{CC}=3.6V, $V_{APC1,2}$=2.8V
	33.1			dBm	Temp=+60°C, V_{CC}=3.3V, $V_{APC1,2}$=2.8V
Total Efficiency	50	57		%	At $P_{OUT,MAX}$, V_{CC}=3.6V
		12		%	P_{OUT}=+20dBm
		5		%	P_{OUT}=+10dBm
Input Power for Max Output	+4.5	+7.0	+9.5	dBm	
Output Noise Power			-72	dBm	RBW=100kHz, 925MHz to 935MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.3V to 5.0V
			-81	dBm	RBW=100kHz, 935MHz to 960MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.3V to 5.0V
Forward Isolation			-22	dBm	$V_{APC1,2}$=0.3V, P_{IN}=+9.5dBm
Second Harmonic		-20	-7	dBm	P_{IN}=+9.5dBm
Third Harmonic		-25	-7	dBm	P_{IN}=+9.5dBm
All Other Non-Harmonic Spurious			-36	dBm	
Input Impedance		50		Ω	
Optimum Source Impedance		40+j10		Ω	For best noise performance
Input VSWR			2.5:1		$P_{OUT,MAX}$-5dB<P_{OUT}<$P_{OUT,MAX}$
			4:1		P_{OUT}<$P_{OUT,MAX}$-5dB
Output Load VSWR					
Stability	8:1				Spurious<-36dBm, $V_{APC1,2}$=0.3V to 2.6V, RBW=100kHz
Ruggedness	10:1				No damage
Output Load Impedance		2.6-j1.5		Ω	Load Impedance presented at RF OUT pad

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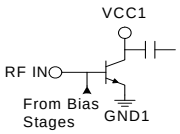
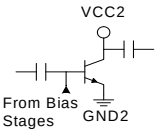
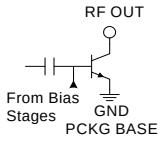
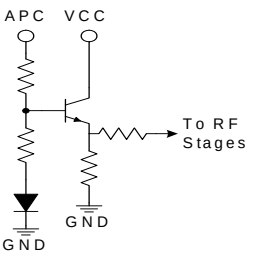
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Control V_{APC1} V_{APC2}					
Power Control "ON"	2.6			V	Maximum P_{OUT}, Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P_{OUT}, Voltage supplied to the input
Power Control Range	75			dB	$V_{APC1,2}$=0.2V to 2.6V
Gain Control Slope	5	100	150	dB/V	P_{OUT}=-10dBm to +35dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	$V_{APC1,2}$=2.8V
			25	µA	$V_{APC1,2}$=0V
Turn On/Off Time			100	ns	$V_{APC1,2}$=0 to 2.8V
Power Supply					
Power Supply Voltage		3.5		V	Specifications
	2.7		4.8	V	Nominal operating limits, P_{OUT}<+35dBm
			5.5	V	With maximum output load VSWR 6:1, P_{OUT}<+35dBm
Power Supply Current		2		A	DC Current at $P_{OUT,MAX}$
	15	200	335	mA	Idle Current, P_{IN}<-30dBm
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V, Temp=+85°C

Pin	Function	Description	Interface Schematic
1	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Refer to the application schematic for proper configuration. Note that position and value of the components are important.	See pin 3.
2	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 1.
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	GND2	Ground connection for the driver stage. To minimize the noise power at the output, it is recommended to connect this pin with a trace of about 40mil to the ground plane. This will slightly reduce the small signal gain, and lower the noise power. It is important for stability that this pin have it's own vias to the ground plane, minimizing common inductance.	See pin 3.
5	VCC2	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	
6	VCC2	Same as pin 5.	
7	NC	Not connected.	
8	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 9.
9	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
10	RF OUT	Same as pin 9.	Same as pin 9.
11	RF OUT	Same as pin 9.	Same as pin 9.
12	RF OUT	Same as pin 9.	
13	NC	Not connected.	
14	VCC	Power supply for the bias circuits.	
15	APC2	Power Control for the output stage. See pin 16 for more details.	See pin 16.
16	APC1	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +35dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when V_{APC1}=2.6V, and 0mA when V_{APC}=0V.	
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the ground plane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

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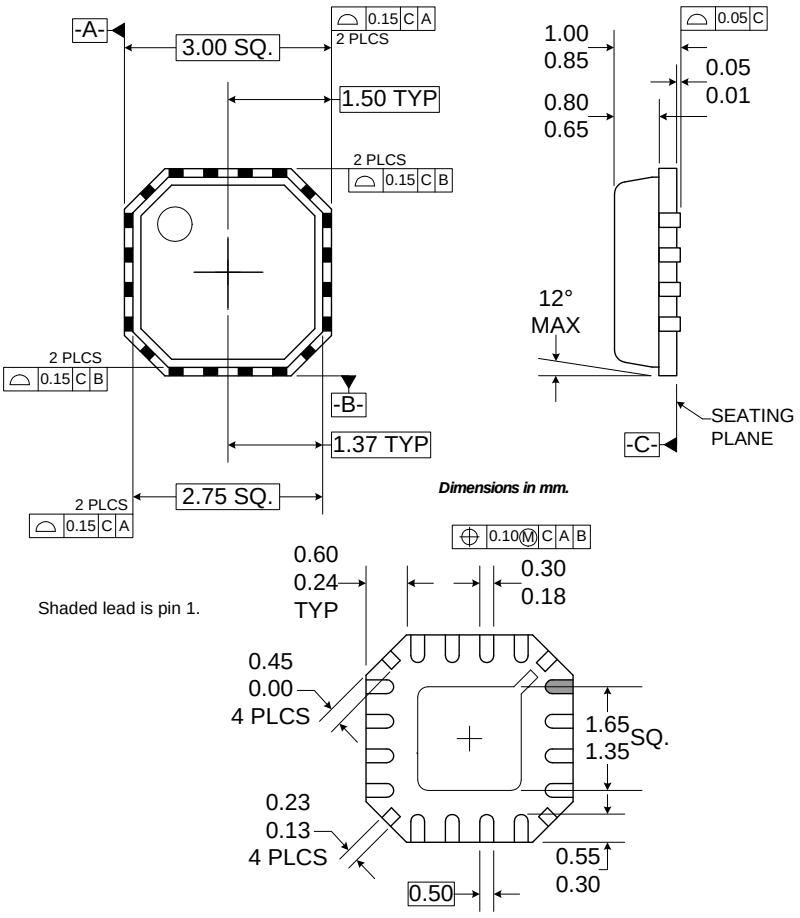
Package Drawing



Theory of Operation

General Purpose Radio Applications

RF5110G has seen widespread use in GSM handset applications, but it can also be used as a final transmit PA for general purpose radio (FSK, ASK). The application schematics in this data sheet outline matching for commonly used frequency bands. Matching is shown for 150MHz, 220MHz, 450MHz, and 865MHz to 928MHz. The standard 900MHz GSM evaluation board can be easily converted for these bands, using the values indicated. The 865MHZ to 928MHz conversion is the most direct, with adjustment required only on output match. The others show changes at input, 1st interstage, 2nd interstage, and output. Common components can be used in most cases. The only key component is the choke seen on RF output. During development of the matches, one goal was to achieve stability (no spurious) into 5:1 output VSWR. The 1μH value and construction proved essential in achieving this level of stability.

This Theory of Operation applies to an open loop system utilizing no power control. In the traditional GSM application, power is sampled at the RF5110G's output and fed back to a log detect function. DAC voltage (V_{SET}) is also input to the log detector. Log detector output drives the V_{APC} pin of RF5110G such that output power corresponding to V_{SET} is obtained, with constant input power>0dBm applied. Power can be set over the full range of defined levels, ranging from small signal to compression. In addition, the control loop is used for ramping in accordance with GSM specifications. If power control is used in the system under consideration, most of the open loop constraints covered here will not apply, aside from thermal considerations discussed below.

When used in an open loop system, RF5110G should be operated in compression. When running small signal, some variation in gain (and therefore output power) will be seen over temperature extremes between -40°C and 85°C. When operated in compression, the impact of this variation is substantially mitigated, making open loop application practical. "Compression" in this case is defined where efficiency exceeds 45%. In the graph section of this data sheet, curves in each frequency band are shown for gain/efficiency/junction temperature versus P_{OUT}/V_{CC}. As indicated in the graphs, high efficiency can be obtained at compressed output power with appropriate choice of supply voltage (V_{CC}). For example, see the efficiency curves for 450MHz. Operation at 31dBm shows efficiency=49% for V_{CC}=2.8V. If 32dBm output is required in design, using V_{CC}=3.3V gives 47% efficiency. So, the system designer can choose an appropriate supply voltage which provides high efficiency at target P_{OUT}.

One important detail to consider is voltage level at V_{APC}. As noted earlier, V_{APC} level varies when operating within a power control loop. This voltage controls output power from the PA. In open loop mode, V_{APC} should be set at 2.8V to ensure consistent output power from RF5110G in volume production.

Another design consideration is maintaining acceptable junction temperature. In the GSM radio, output power in excess of 34dBm is common. This is allowable due to the limit on transmit duty cycle and pulse width. The worst case condition sees duty cycle at 50%, with pulse width equal to approximately 2msec. In this situation, the PA cuts off before junction temperature reaches the maximum that would be seen with longer pulse width. For the non–GSM radio, it is assumed pulse width will exceed 2msec. Thus, restrictions must be imposed on allowable maximum output power. The most conservative analysis is used, that for 100% duty cycle. Thermal scans have shown R_{TH} (thermal resistance) of RF5110G+the evaluation board to be 36°C/W. R_{TH} for the evaluation board has been calculated at 10.4°C/W, giving RF5110G R_{TH_JC}=25.6°C/W. Data sheet curves show projected junction temperatures (T_J) for each general purpose radio frequency band. R_{TH} of RF5110G+the evaluation board is taken into account. A conservative goal is $T_J \leq 150$°C when operating at a maximum specified ambient temperature of 85°C. Maximum output power will then be bounded by that limit. Observing the T_J curves in bands from 150MHz to 928MHz, one sees that 32dBm is always at or below 150°C. This shows that the output load line in each match was intentionally set for high efficiency. To ensure equivalent performance in one's system, care should be taken to achieve efficiency equal to or better than that seen in the data. Thermal performance can be predicted with a simple calculation at a desired output power:

$P\_DC = V_{CC} \times I_{CC}$

P_{OUT} (Watt)=[10^(P_{OUT} (dBm)/10)]/1000

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Dissipated Power = $P_{DISS} = P\_DC - P_{OUT}$

$R_{TH} = R_{TH\_JC\_RF5110G} + R_{TH\_SYSTEM\_BOARD}$ ($R_{TH\_JC\_RF5110G} = 25.6°C/W$)

Junction Temperature @ 85°C ambient = $T_J = 85°C + P_{DISS} \times R_{TH}$

Efficiency calculation alone may not suffice, as the system board may be substantially thicker than that of the RF5110G evaluation board. This will increase R_{TH} for the system, and likewise T_J.

Layout considerations are important in repeating RF5110G evaluation board performance in a system design. Via arrangement underneath the part is critical, as are other via arrangements and supply trace routings (see "GSM Applications" section for the GSM case). Layout files for the RF5110G evaluation board can be obtained by contacting RFMD applications/sales.

As already stated, output match is a primary consideration in achieving desired performance. In moving from the RF5110G evaluation board to the system board, the first approach would be to implement the same matching topology/values as seen in application schematics. Performance on the system board can then be checked, particularly with regard to gain and efficiency at target output power. If needed, matching values can be adjusted to obtain equivalent performance. Observing each output match from 150MHz to 900MHz, it can be seen that topology takes 1 of 2 possible configurations:

C – L – C: 150MHz, 220MHz, 900MHz

L – C: 450MHz

Other areas which impact response are the 1st and 2nd interstage matches, found at pins 1 and 5/6, respectively. Small signal responses for each match are shown in this data sheet. Checking response on the system board will verify that input/interstage matches are in line (output to some extent as well). This verification can be done by placing SMA connectors at the input/output of RF5110G, and observing small signal response.

Following the guidelines contained within this section should ensure successful implementation of RF5110G in general radio applications.

GSM Applications

The RF5110G is a three-stage device with 32 dB gain at full power. Therefore, the drive required to fully saturate the output is +3dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called "local ground plane" on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 2000mA. The optimum load for the output stage is approximately 2.6Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is 2.6-j1.5Ω. With this match, a 50Ω terminal impedance is achieved. The input is internally matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

$V_{CC}1$ and $V_{CC}2$ provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially, the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 2A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600µs pulse, unless specified otherwise.

The part will operate over a 3.0V to 5.0V range. Under nominal conditions, the power at 3.5V will be greater than +34.5dBm at +90°C. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This must occur during operation, or the device may be damaged from too much power dissipation. At 5.0V, over +38dBm may be produced; however, this level of power is not recommended, and can cause damage to the device.

The HBT breakdown voltage is >20V, so there are no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current de device will sink, and the safe current densities could be exceeded.

High current conditions are potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF5110G includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

To avoid excessively high currents it is important to control the V_{APC} when operating at supply voltages higher than 4.0V, such that the maximum output power is not exceeded.

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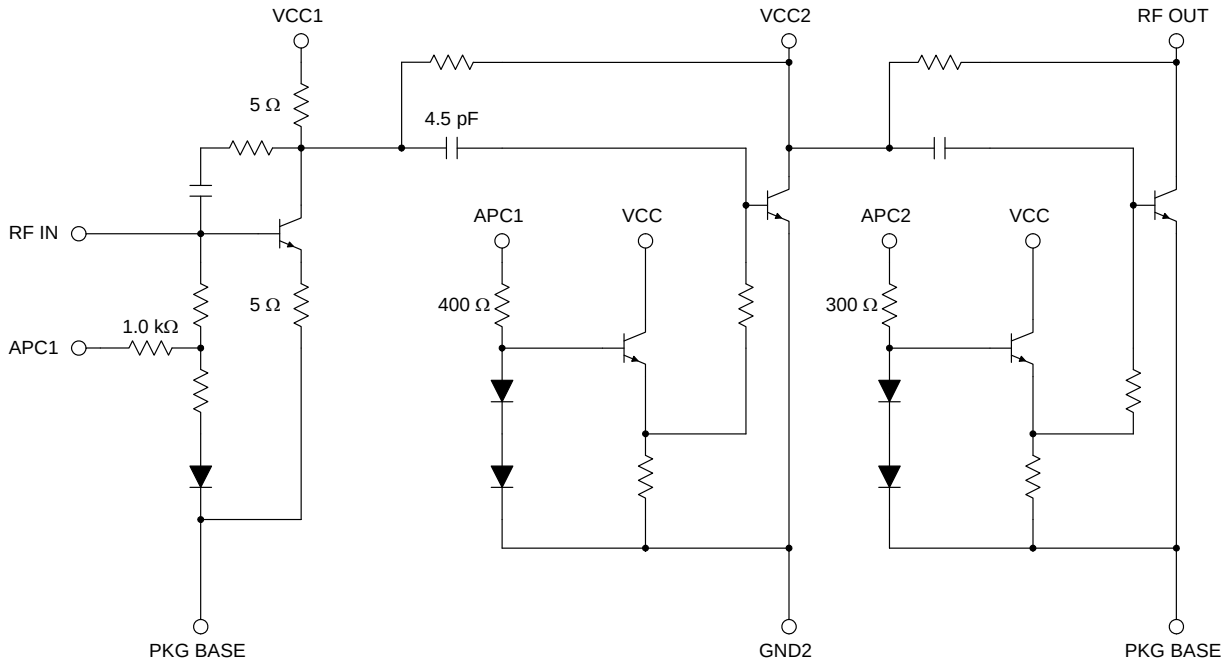
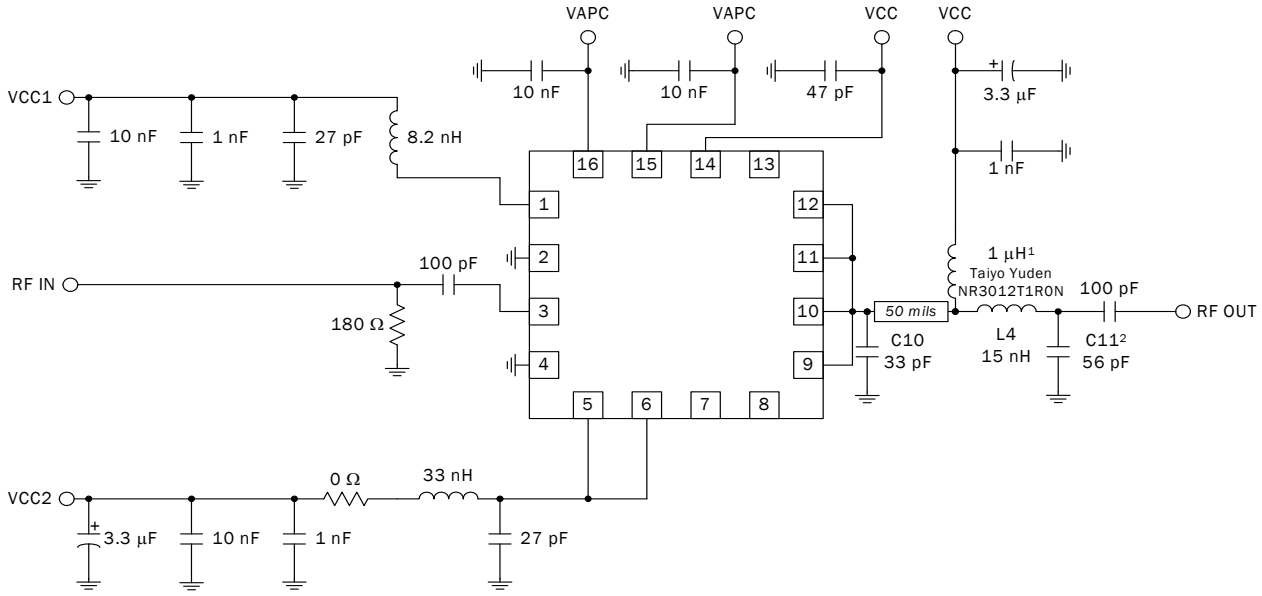
Internal Schematic

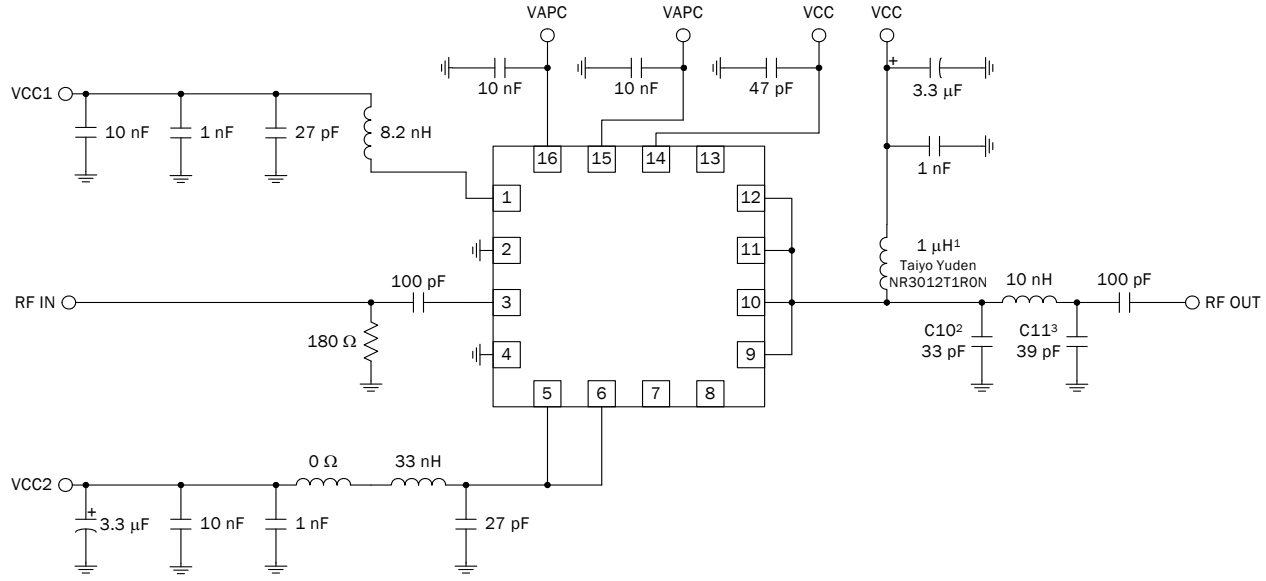


Application Schematic
150MHz FM Band



[1]Requires layout change to standard evaluation board.
[2]C11 adjacent to L4.

Application Schematic
220MHz FM Band



[1]Requires layout change to standard evaluation board.
[2]C10 is adjacent to L4.
[3]C11 is 140 mils from L4.

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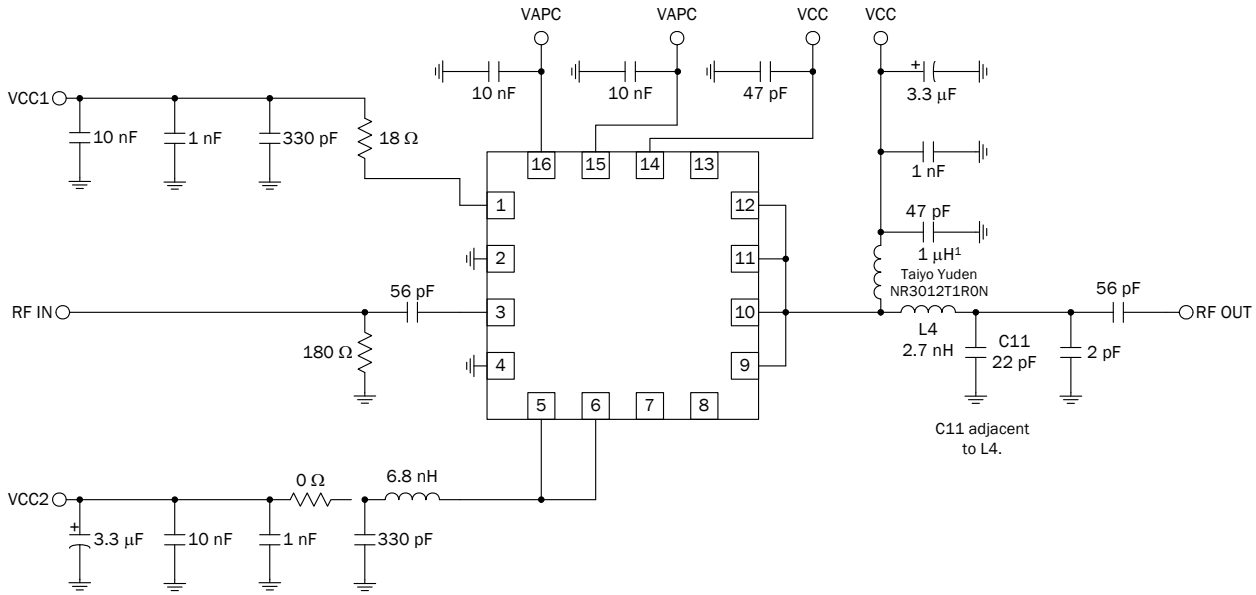
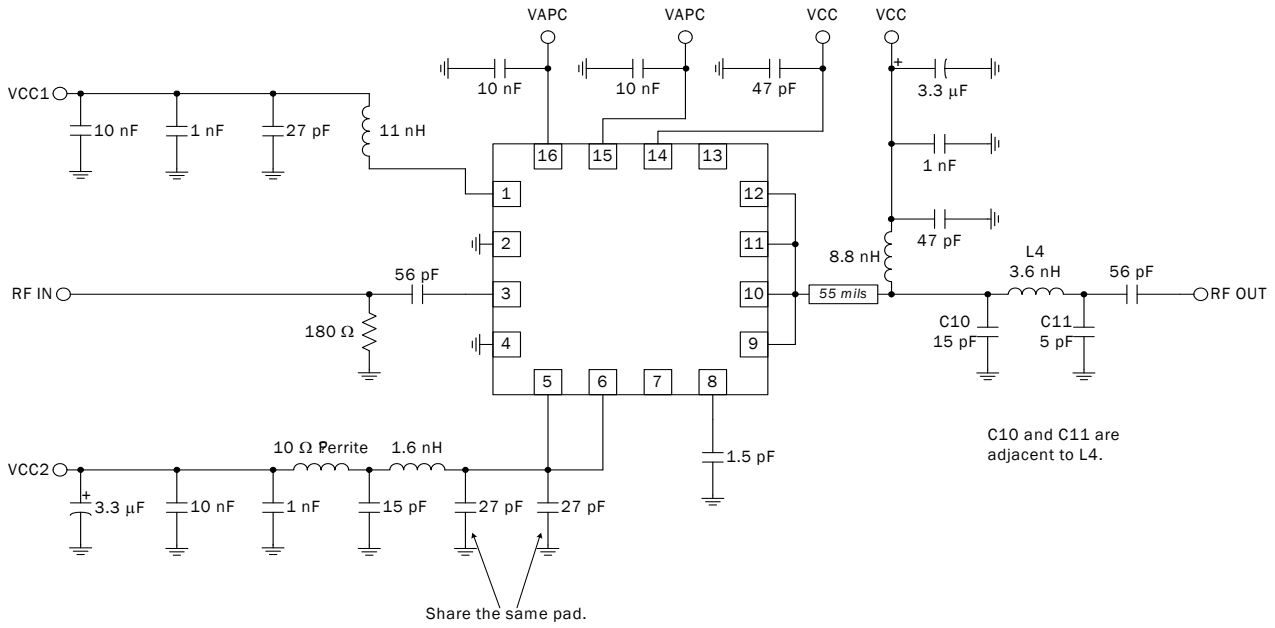
Application Schematic
450MHz FM Band



[1]Requires layout change to standard evaluation board.

Application Schematic
865MHz and 902MHz to 928MHz ISM Bands



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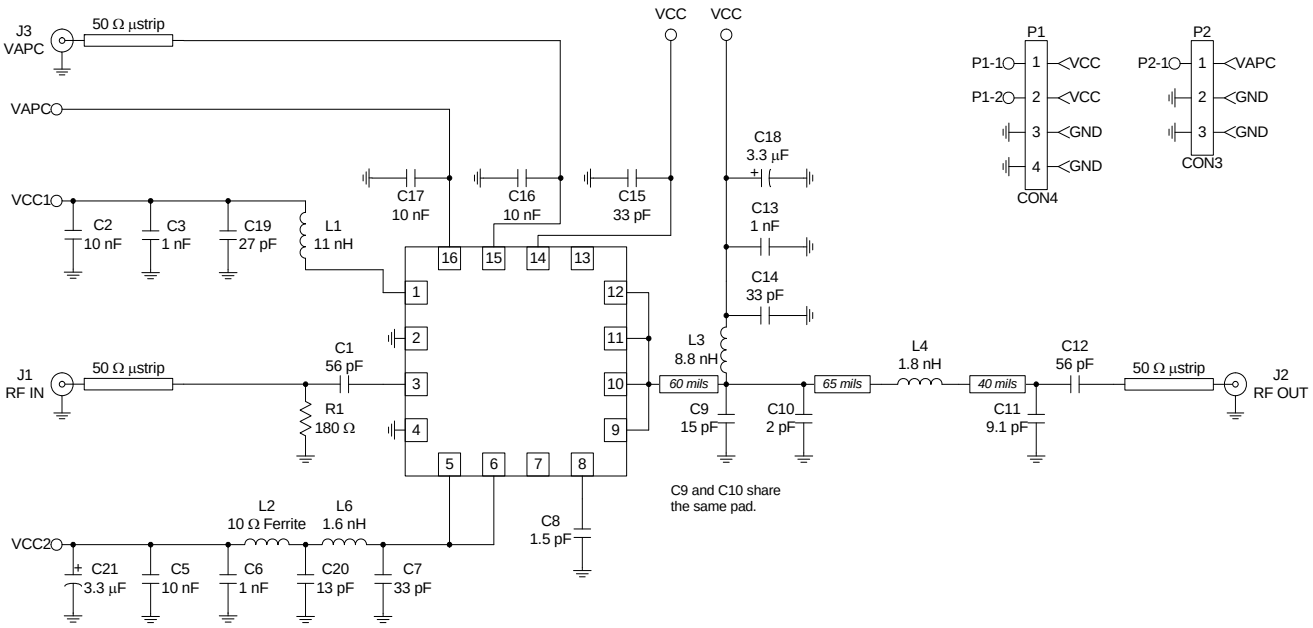
Evaluation Board Schematic
GSM850 Lumped Element



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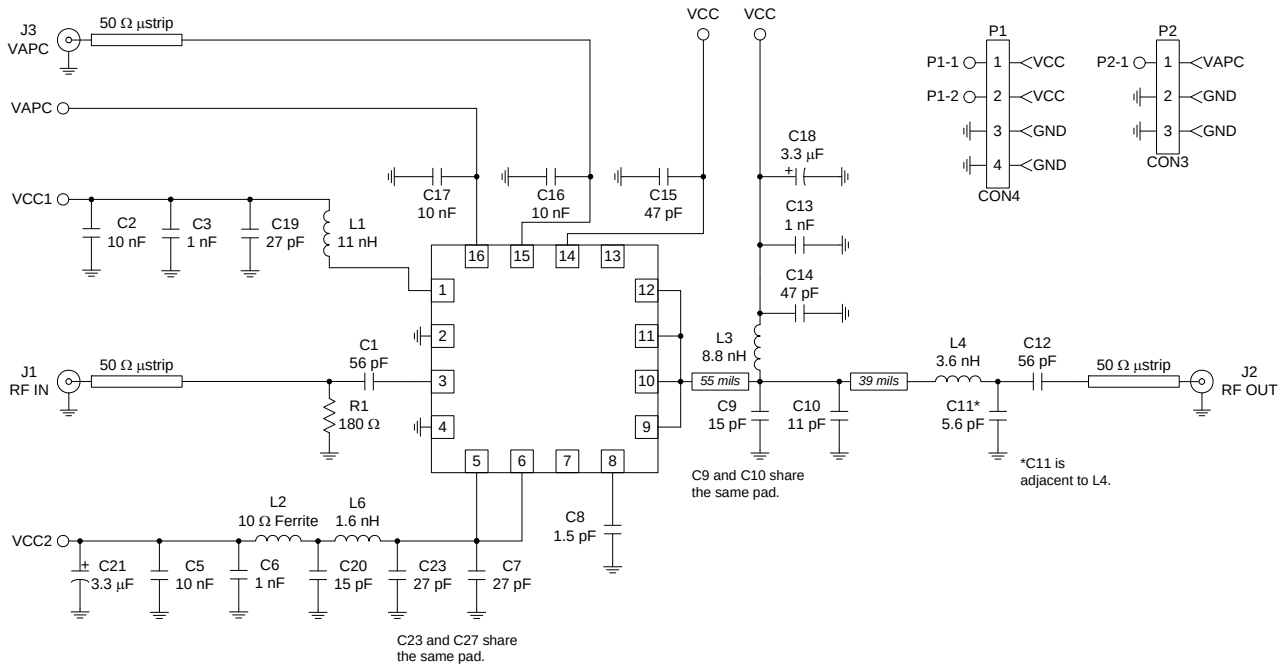
Evaluation Board Schematic
GSM900 Lumped Element



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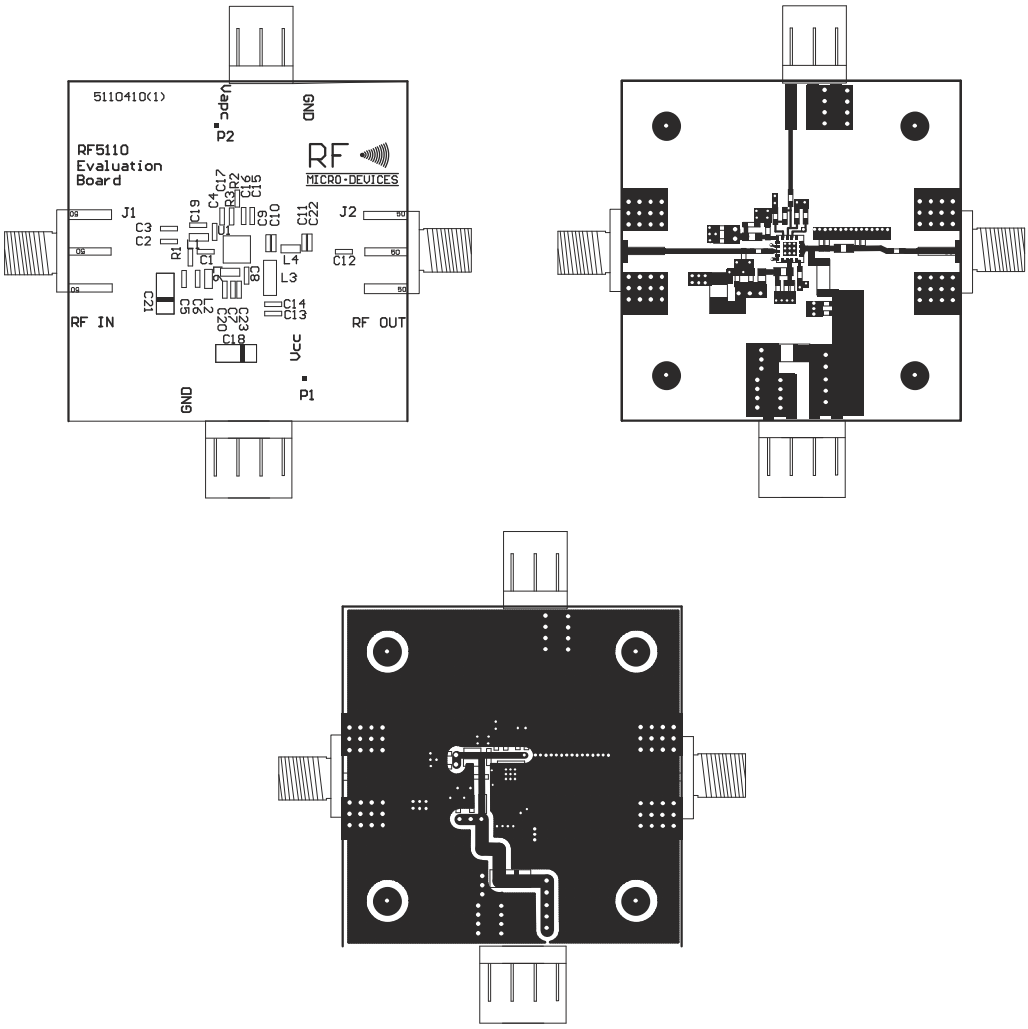
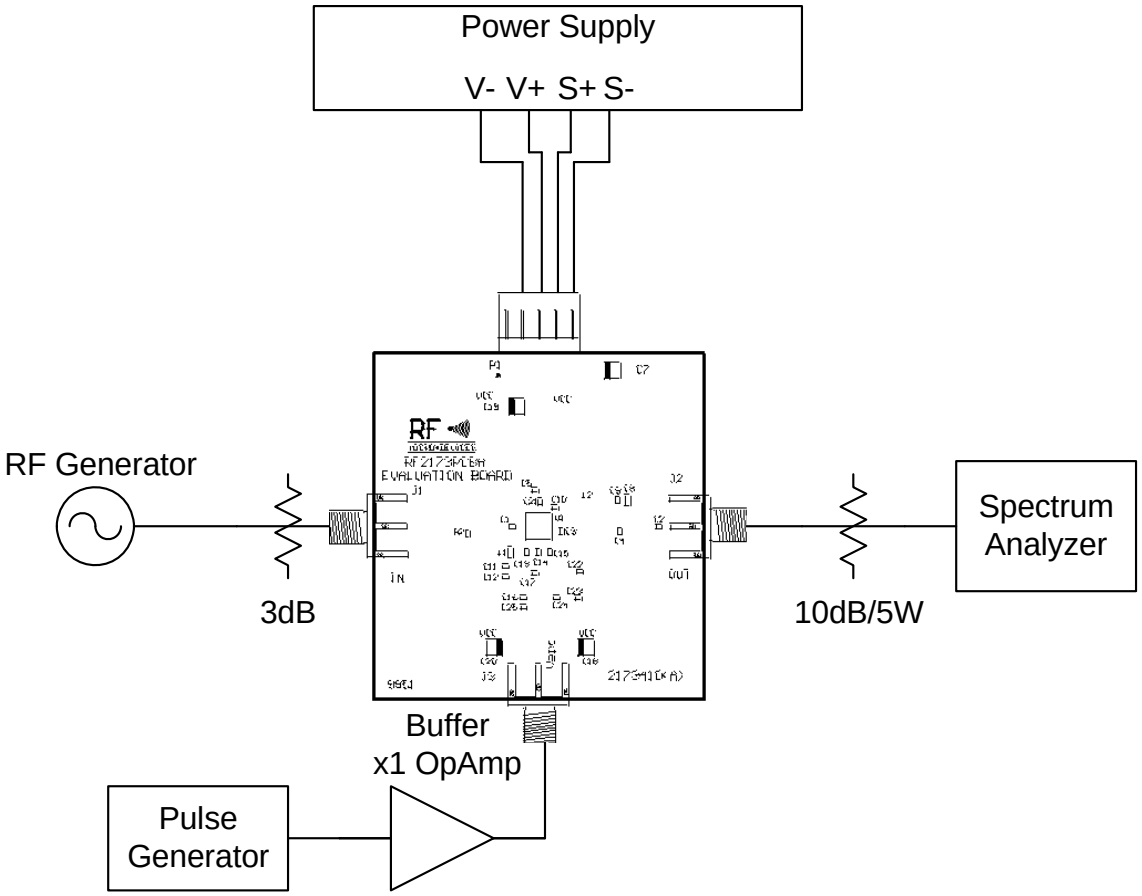
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.032”; Board Material FR-4; Multi-Layer



Typical Test Setup



A buffer amplifier is recommended because the current into the V_{APC} changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

Notes about testing the RF5110G

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effect on the signal generator as a result of switching the input impedance of the PA. When V_{APC} is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be sized accordingly to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the V_{APC} should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and V_{APC} needs to be adjusted accordingly. This simulates the behavior for the power control loop. To avoid damage, it is recommended to set the power supply to limit the current during the burst not to exceed the maximum current rating.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

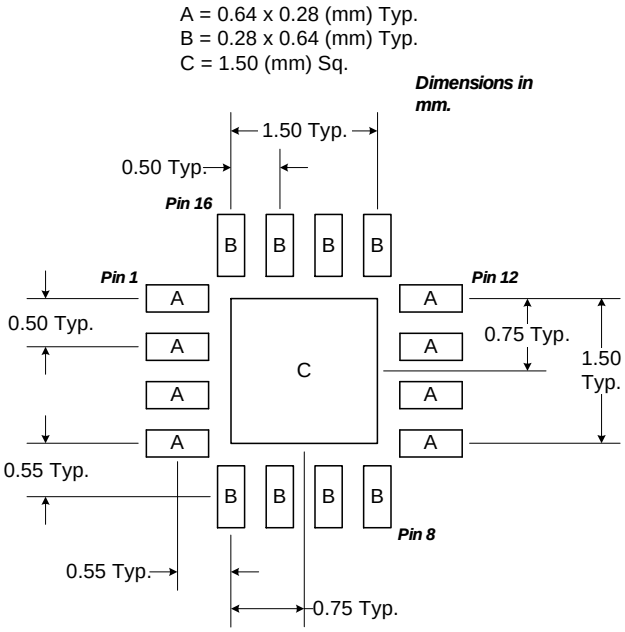

Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

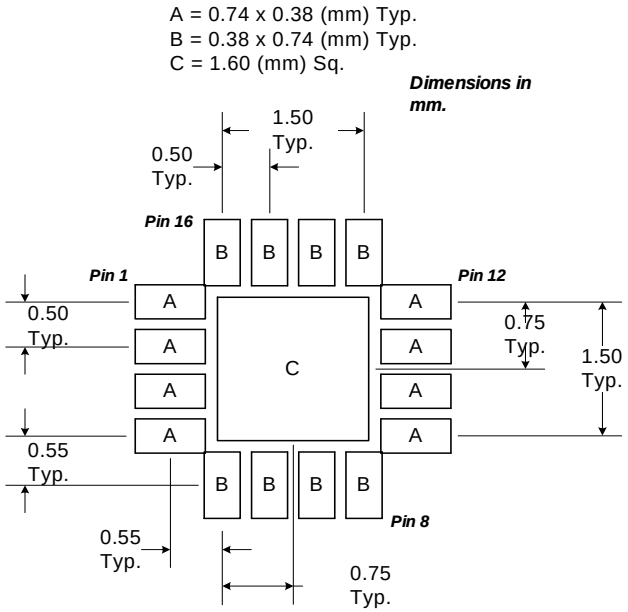

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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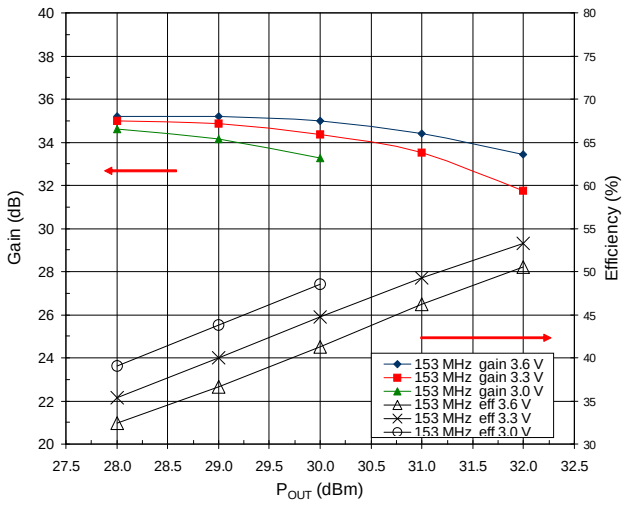
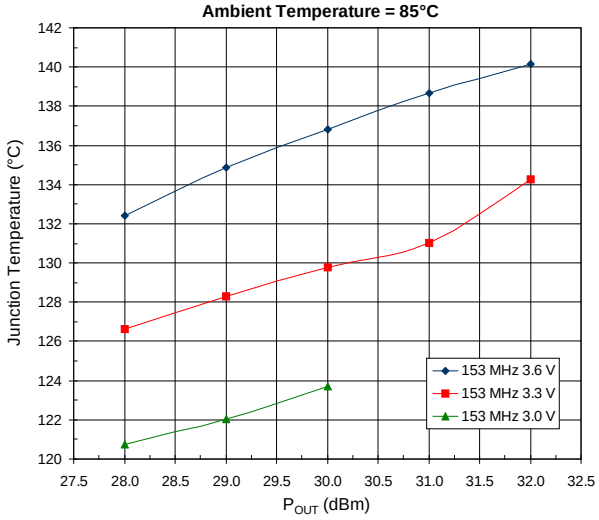
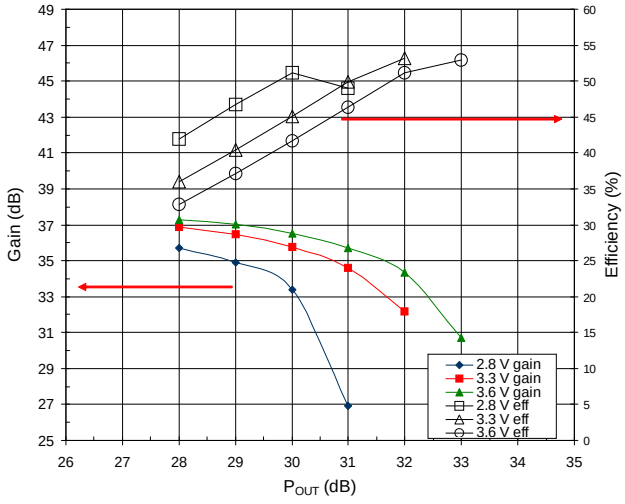
RF5110G 153 MHz Gain and Efficiency Versus P_{OUT}/V_{CC}



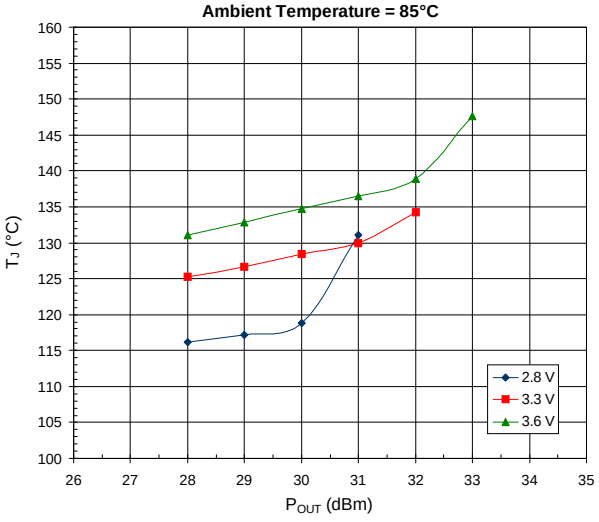
RF5110G 153 MHz Junction Temperature Versus P_{OUT}/V_{CC}
Ambient Temperature = 85°C



RF5110G 220 MHz Gain and Efficiency Versus P_{OUT}/V_{CC}



RF5110G 220 MHz Junction Temperature Versus P_{OUT}/V_{CC}
Ambient Temperature = 85°C



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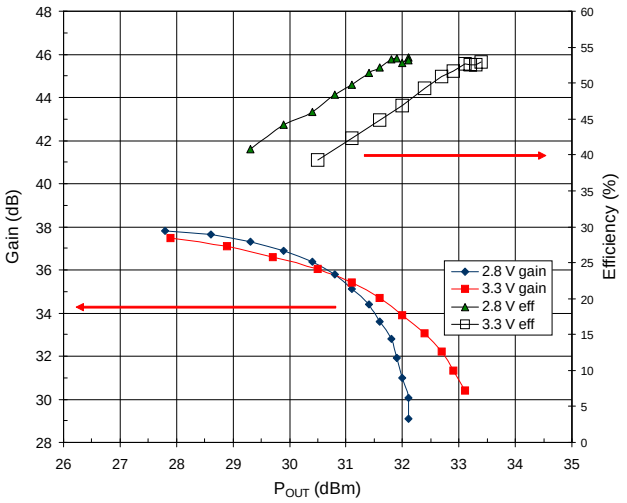
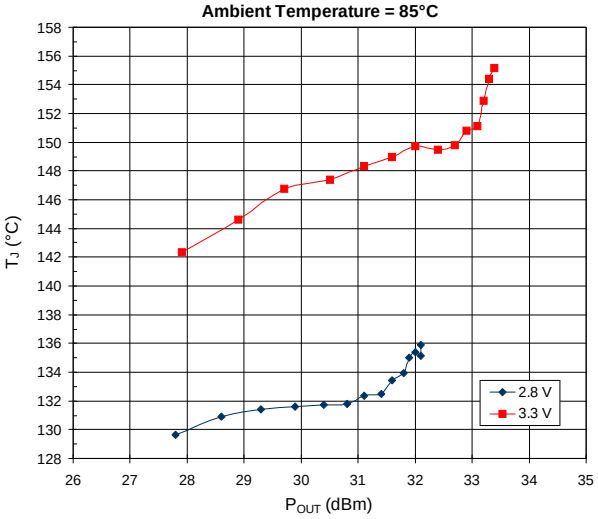
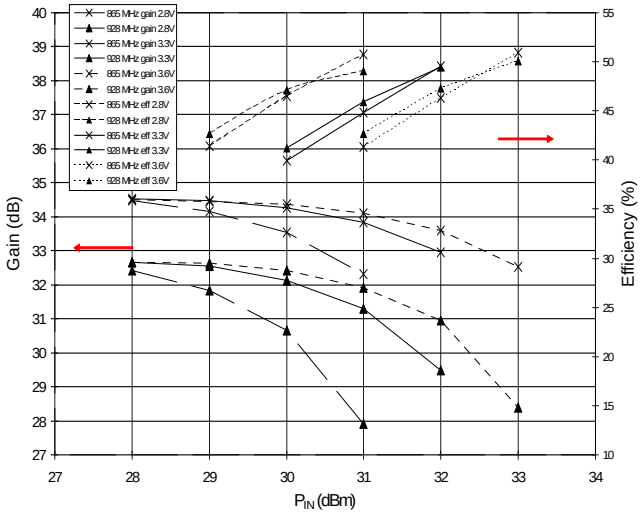
RF5110G 450 MHz Gain and Efficiency Versus P_{OUT}/V_{CC}



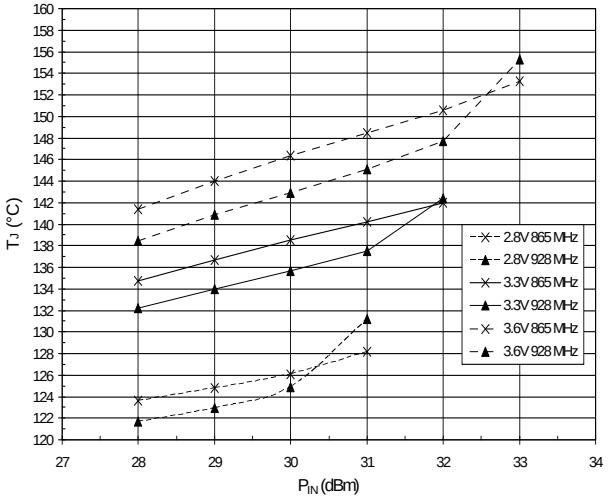
RF5110G 450 MHz Junction Temperature Versus P_{OUT}/V_{CC}
Ambient Temperature = 85°C



RF5110G 865 MHz to 928 MHz Gain and Efficiency Versus P_{OUT}/V_{CC}



RF5110G 865 MHz to 928 MHz Junction Temperature Versus P_{OUT}/V_{CC}
Ambient Temperature = 85°C



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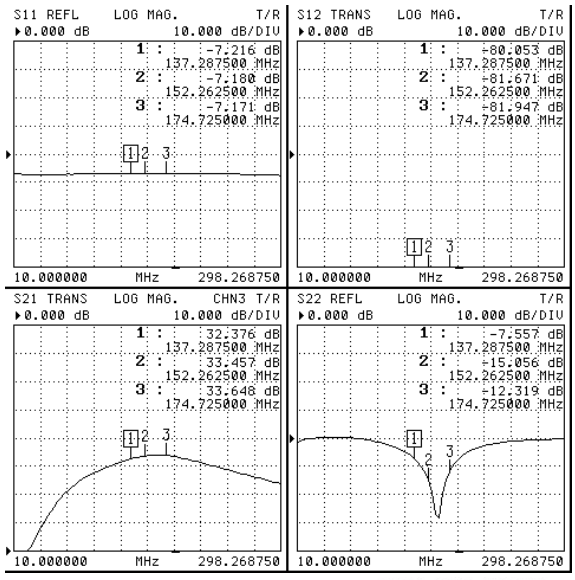
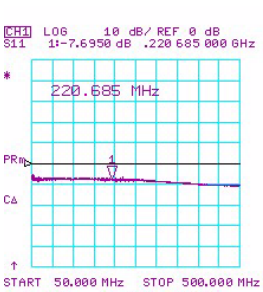
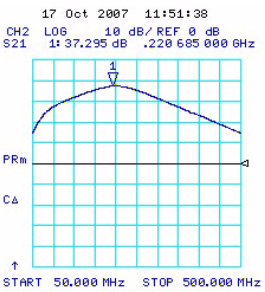
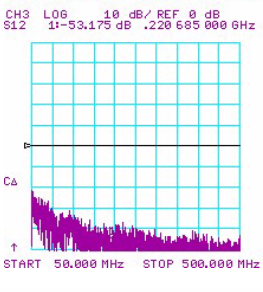
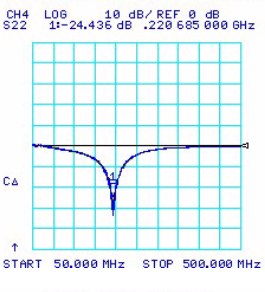
Application Schematic Small Signal Response

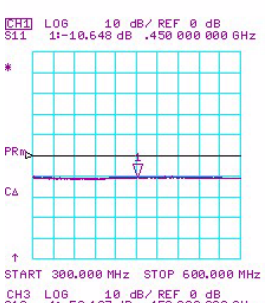


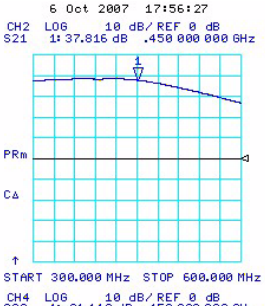


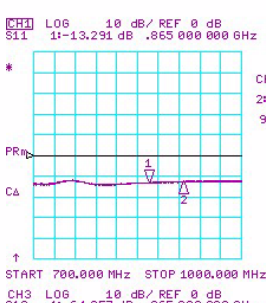


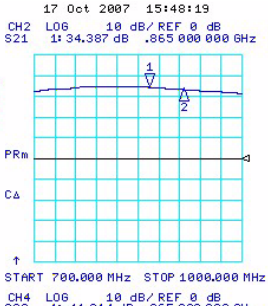


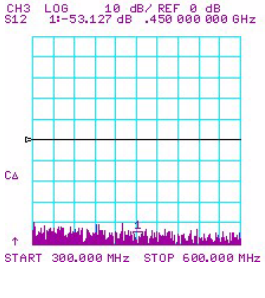


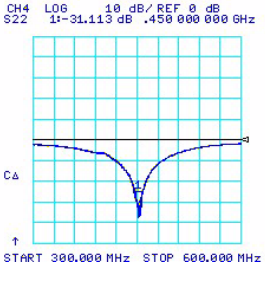


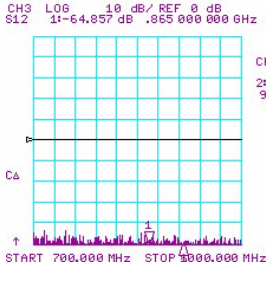


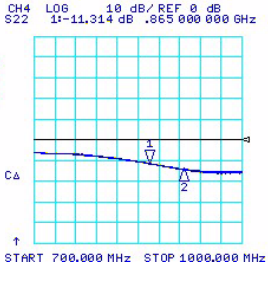












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Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

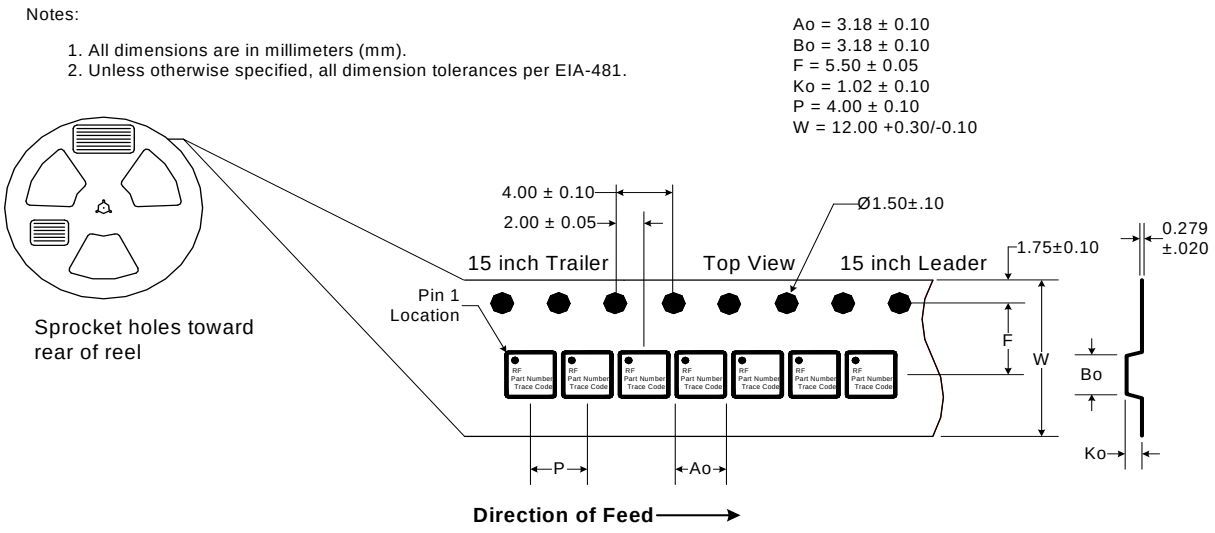
Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF5110GTR7	7 (178)	2.4 (61)	12	4	Single	2500

QFN (Carrier Tape Drawing with Part Orientation)



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