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DESCRIPTION

The PT8146 is an 8-bit D/A converter with 12 built-in channels. Each of the 12 analog outputs have a built-in OP amplifier with large current drive capability. The data input/output format is chip select (/CS) with serial bus connection available while a built-in 12-bit I/O expander enables serial-parallel conversion (8 of the 12 bits can also be used for analog output).

FEATURES

- Ultra compact package
- Ultra low power consumption (1.2mW/chl: typical)
- Built-in 12-channel R-2R type 8-bit D/A converter
- Built-in 12-bit I/O expander (8 bits also function as analog output)
- Built-in analog output amplifier (sink current 1.0mA maximum, source current 1.0mA maximum)
- Built-in power-on detection circuit (initialized at detection of VccD power-on)
- MCU interface compatible with 3V to 5V systems
- Power divided into MCU interface power supply (VccD) and OP amplifier power supply (VccA), D/A converter power supply (VccD)
- Analog output capability from 0 V to VccA
- Serial data I/O operates to maximum of 2.5MHz (in cascade connection, up to 2.5MHz when VccD=5V, up to 1.5Mhz when VccD=3V)
- CMOS process
- Available in 24 pin, SSOP Package

APPLICATIONS

- Microcontroller port expansion
- Electronic level adjustment
- Replacement of semi-fixed resistance for tuning

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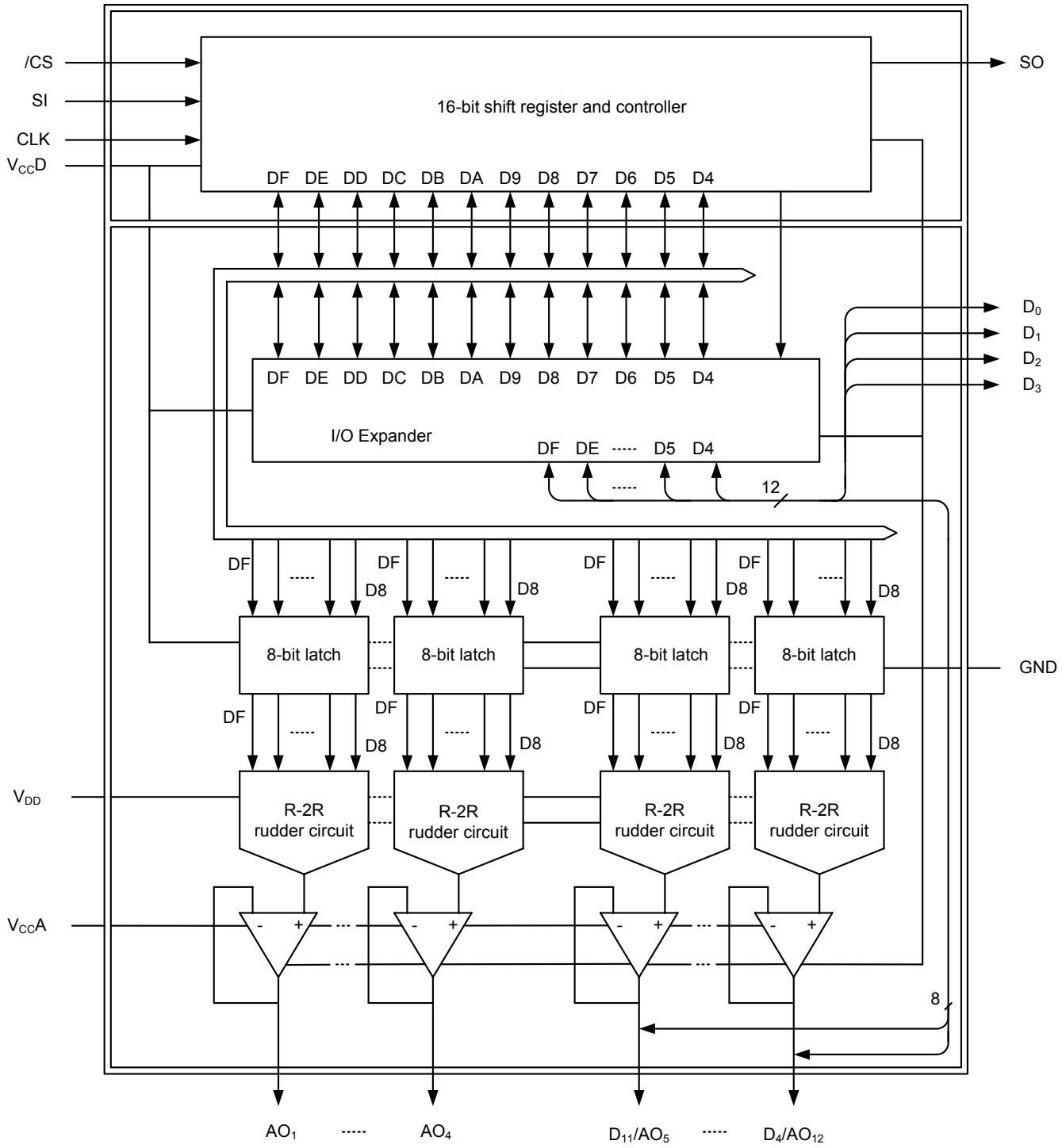
BLOCK DIAGRAM



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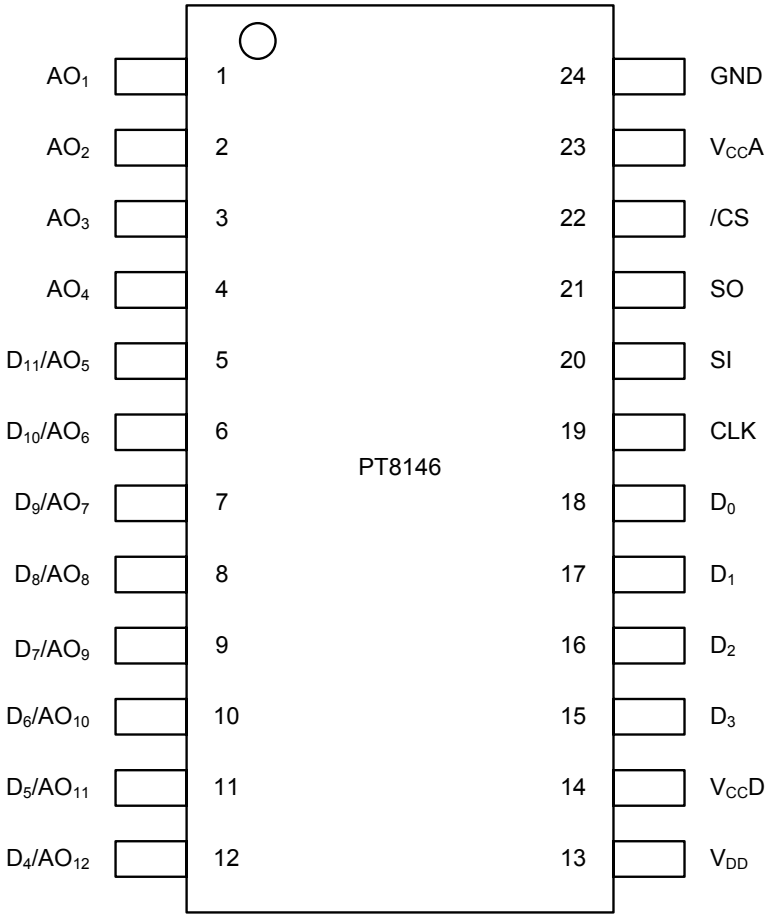
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	Description	Pin No.
AO1 to AO4	D/A converter analog output pins (VDD to GND output). (Default: output #00 setting level)	1 to 4
D11/AO5 to D4/AO12	These pins may be used as either I/O expander parallel input/output (VCCA/GND output 0.5 VCCA/0.2 VCCA input) or as D/A converter analog output (VDD to GND output). Pin status is controlled by input data. See “Data Configuration”. (Default: Input mode, Hi-Z state)	5 to 12
VDD*1	D/A converter reference power pin.	13
VCCD*1	MCU interface power supply pin (power supply for I/O expander)	14
D3 to D0	I/O expander parallel input/output pins. (VCCD/GND output: When VCCD ≥ 4.0 V, 0.5 VCCD/0.2 VCCD input, When VCCD < 4.0 V, 2 V/0.2 VCCD input) Pin status is controlled by input data See “Data Configuration.” (Default: Input mode, Hi-Z state)	15 to 18
CLK*2	Shift clock signal input pin. When CS = “L”, SI data is loaded into the shift register at the rising edge of the shift clock.	19
SI*2	Data input pin (serial input pin). Used for 16-bit serial data input.	20
SO	Data output pin (serial output pin). The first bit (LSB) data of the 16-bit shift register is output simultaneously with the falling edge of the shift clock. When /CS output = “H”, this pin goes to high impedance state.	21
/CS*2	Chip select signal input pin. Input to shift registers is enabled when the/ CS signal falling edges. Shift register contents can be executed when the /CS signal rising edges.	22
VCCA*1	Analog unit power supply pin (OP amplifier power supply).	23
GND	Common GND pin	24

*1: Be sure that VCCA ≥ VCCD, and that VCCA ≥ VDD.
*2: Do not leave this pin in floating state.

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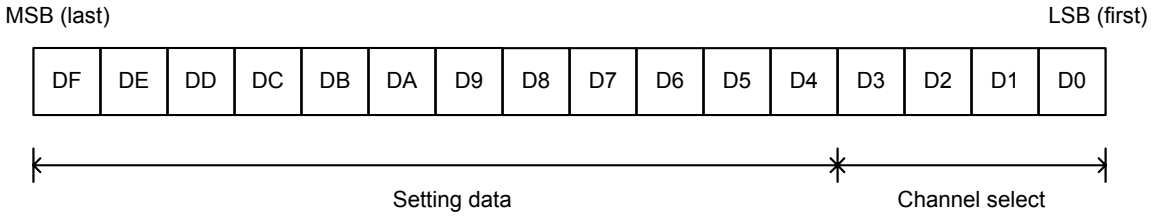
DATA CONFIGURATION

1. DATA CONFIGURATION



2. CHANNEL SELECT

D3	D2	D1	D0	Function
0	0	0	0	Don't care/special function
0	0	0	1	AO1 selected
0	0	1	0	AO2 selected
to	to	to	to	to
1	0	1	1	AO11 selected
1	1	0	0	AO12 selected
1	1	0	1	I/O expander (serial → parallel)
1	1	1	0	I/O expander (parallel → serial)
1	1	1	1	Expander Status Register (ESR)

3. SETTING DATA

DON'T CARE/SPECIAL FUNCTION (CHANNEL SELECT = "0000")

DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Function
x	x	x	x	x	x	x	x	0	0	0	0	Don't care
to	to	to	to	to	to	to	to	to	to	to	to	Don't care
x	x	x	x	x	x	x	x	1	0	1	1	Don't care
0	0	0	0	0	0	0	0	1	1	0	0	GND (all channels)
0	0	0	0	0	0	0	1	1	1	0	0	VDD/256 x 1 (all channels)
0	0	0	0	0	0	1	0	1	1	0	0	VDD/256 x 2 (all channels)
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	1	0	1	1	0	0	VDD/256 x 254 (all channels)
1	1	1	1	1	1	1	1	1	1	0	0	VDD/256 x 255 (all channels)
x	x	x	x	x	x	x	x	1	1	0	1	Hi-Z (I/O expander state)*
x	x	x	x	x	x	x	x	1	1	1	0	Reset (state when power is ON)
x	x	x	x	x	x	x	x	1	1	1	1	Don't care

x: Don't care
*: Hi-Z output on all channels of AO5 through AO12

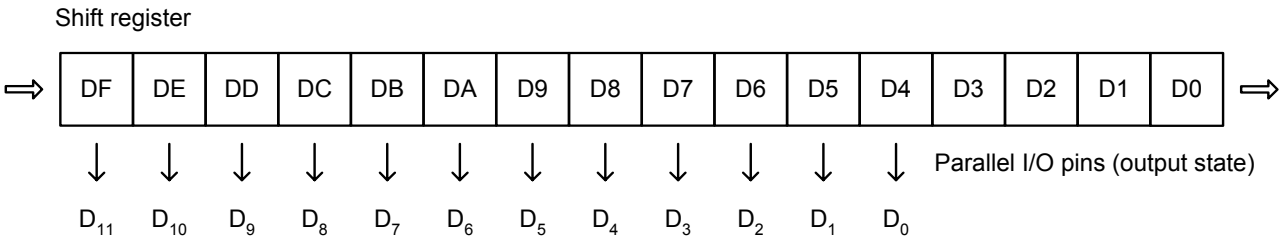
D/A CONVERTER (CHANNEL SELECT = "0001" TO "1100")

DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Function
0	0	0	0	0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	0	0	0	0	VDD/256 x 1
0	0	0	0	0	0	1	0	0	0	0	0	VDD/256 x 2
0	0	0	0	0	0	1	1	0	0	0	0	VDD/256 x 3
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	0	1	0	0	0	0	VDD/256 x 253
1	1	1	1	1	1	1	0	0	0	0	0	VDD/256 x 254
1	1	1	1	1	1	1	1	0	0	0	0	VDD/256 x 254
x	x	x	x	x	x	x	x	0	0	0	1	Hi-Z (I/O expander state)*
x	x	x	x	x	x	x	x	0	0	1	0	Don't care
to	to	to	to	to	to	to	to	to	to	to	to	Don't care
x	x	x	x	x	x	x	x	1	1	1	1	Don't care

x: Don't care
*: Only AO5 through AO12 output is valid

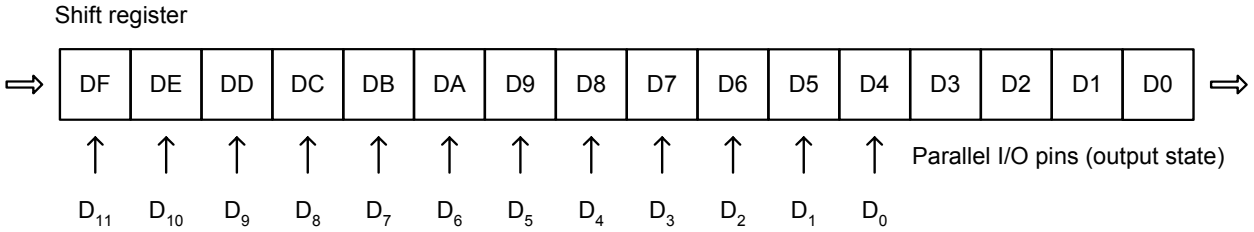
I/O EXPANDER (CHANNEL SELECT = "1101"): SERIAL → PARALLEL CONVERSION

Performs parallel conversion of data bits D4 to DF for output on pins D0 to D11.
Note that only those pins designated for output in the ESR (expander status register) are output.

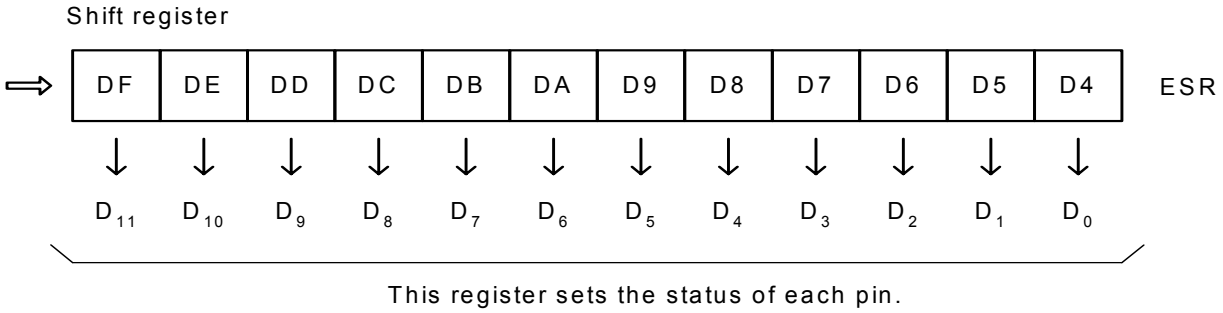


I/O EXPANDER (CHANNEL SELECT = "1110"): PARALLEL → SERIAL CONVERSION

Writes data from D0 to D11 pins to bits D4 to DF in the shift register.
Data is output to the SO pin on the shift clock (CLK) signal. (The first 4 bits output data D0 to D3, so the converted output should be read as data bits 5 through 16.)
Note that the data value is "0" for pins designated for output in the ESR (expander status register) as well as analog output pins.



EXPANDER STATUS REGISTER (CHANNEL SELECT = "1111")



Setting	Pin Status
"0"	Input standby status (Hi-Z output) D11 to D4 pins for analog output should be set to "0".
"1"	Output state

Note: After power VCCD is turned on, the state of pins and registers is as follows:

Pin	State
AO1 to AO4	"L" output
D11/AO5 to D4/AO12	Hi-Z state (input state)
D3 to D0	Hi-Z state (input state)

Pin	State
Shift register	Bits DF to D8 are "0", and D7 to D0 are not defined (retain prior status)
D/A register	All reset to "0"
Parallel output register	Not defined (retain prior state)
Expander Status Register (ESR)	All reset to "0"

ESR settings have priority in determining pin states. Switching between input standby state and analog output state is enabled even when the ESR value is "1". When the ESR value returns to "0", the pin returns to its previously defined state.
In input standby state with AO set for Hi-Z output, the AO output setting can be used for transitions to AO output state.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings		Unit
			Min.	Max.	
Power supply voltage	VCCA	Based on GND (TA=+25℃)	-0.3	+7.0	V
	VCCD		-0.3	VCCA*	V
	VDD		-0.3	VCCA*	V
Input voltage 1	VIN1	SI, CLK, /CS, SO, D1 to D3	-0.3	VCCD + 0.3	V
Output voltage 1	VOUT1		-0.3	VCCD + 0.3	V
Input voltage 2	VIN2	D4 to D11	-0.3	VCCA + 0.3	V
Output voltage 2	VOUT2		-0.3	VCCA + 0.3	V
Power consumption	PD	-	-	250	mW
Operating temperature	Topr	-	-40	+85	℃
Storage temperature	Tstg	-	-65	+150	℃

* : $V_{CC}A \geq V_{CC}D$, $V_{CC}A \geq V_{DD}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Power supply voltage	VCCA	-	4.5	5.0	5.5	V
	VCCD	VCCA ≥ VCCD	2.7	-	VCCA	V
	VDD	VCCA ≥ VCCD	2.0	-	VCCA	V
	GND	-	-	0	-	V
Analog output current	IAL	Source current	-	-	1.0	mA
	IAH	Sink current	-	-	1.0	mA
Oscillation limit output capacity	COL	-	-		1.0	μF
Operation temperature	Topr	-	-40	-	+85	℃

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

DIGITAL SECTION

($V_{CC}D \leq V_{CC}A$, Ta=-20 to +85℃)

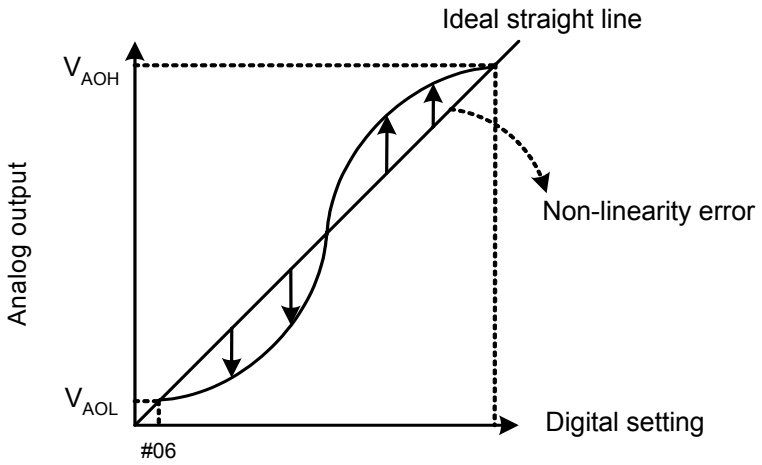
Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Power supply voltage	VCCD	VCCD	-	2.7	5.0	5.5	V
Power supply current	ICCD		CLK=1MHz, (Unloaded)	-	0.2	0.5	mA
Standby current	ICCS		CLK, SI, /CS Stop Vin=VCCD or GND	-10	-	+10	μA
Input leak current	IILK1	CLK, SI, /CS, D0 to D3	Vin=0 to VCCD	-10	-	+10	μA
"H" level input voltage	VIH1		VCCD ≥ 4.0 V	0.5 x VCCD	-	-	V
			VCCD < 4.0 V	2.0	-	-	V
"L" level input voltage	VIL1		-	-	-	0.2 x VCCD	V
High-impedance leak current	IOLK	SO	Vin=0 to VCCD	-10	-	+10	μA
"H" level output voltage	VOH1	SO, D0 to D3	IOH=-0.4mA	VCCD – 0.4	-	-	V
"L" level output voltage	VOL1		IOL=2.5mA	-	-	0.4	V

D/A CONVERTER SECTION

($V_{CC}A$=5V±10%, Ta=-20 to +85℃)

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Power supply voltage	VDD	VDD	VDD ≤ VCCA	2.0	5.0	5.5	V
Power supply current	IDD		VDD ≤ VCCA	-	1.2	2.5	mA
Resolution	Res	AO1 to AO12	Unload VDD=VCCA – 0.1 V Digital value: #06 to #FF	-	8	-	bits
Monotonic increase	Rem			-	8	-	bits
Nonlinearity error	LE			-1.5	-	+1.5	LSB
Differential linearity error	DLE			-1.0	-	+1.0	LSB

Nonlinearity error:	Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at “06” and output voltage at “FF”.
Differential linearity error:	Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note: The value of VAOH and VDD, and the value of VAOL and GND are not necessarily equivalent.

OPERATIONAL AMPLIFIER / ANALOG OUTPUT SECTION

(V_{DD}=V_{CC}A, Ta=-20 to +85℃)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	VCCA	VCCA	-	4.5	5.0	5.5	V
Power supply current	ICCA		#80 setting (Unloaded)	-	1.0	3.7	mA
Input leak current	IILK2	D4 to D11	Vin = 0 to VCCA	-10	-	+10	µA
"H" level digital input voltage	VIH2		-	0.5 x VCCA	-	-	V
"L" level digital input voltage	VIL2		-	-	-	0.2 x VCCA	V
"H" level digital output voltage	VOH2		IOH = -0.4 mA	VCCA – 0.4	-	-	V
"L" level digital output voltage	VOL2		IOL = 2.5 mA	-	-	0.4	V
Analog output minimum voltage 1	VAOL1	AO1 to AO12	IAL = 0 mA #00 setting	GND	-	0.1	V
Analog output minimum voltage 2	VAOL2		IAL = 0.5 mA #00 setting	-0.2	GND	0.2	V
Analog output minimum voltage 3	VAOL3		IAH = 0.5 mA #00 setting	GND	-	0.2	V
Analog output minimum voltage 4	VAOL4		IAL = 1.0 mA #00 setting	-0.3	GND	0.3	V
Analog output minimum voltage 5	VAOL5		IAH = 1.0 mA #00 setting	GND	-	0.3	V
Analog output maximum voltage 1	VAOH1	AO1 to AO12	IAL = 0 mA #FF setting	VCCA – 0.1	-	VCCA	V
Analog output maximum voltage 2	VAOH2		IAL = 0.5 mA #FF setting	VCCA – 0.2	-	VCCA	V
Analog output maximum voltage 3	VAOH3	AO1 to AO12	IAH = 0.5 mA #FF setting	VCCA – 0.2	VCCA	VCCA + 0.2	V
Analog output maximum voltage 4	VAOH4		IAL = 1.0 mA #FF setting	VCCA – 0.3	-	VCCA	V
Analog output maximum voltage 5	VAOH5		IAH = 1.0 mA #FF setting	VCCA – 0.3	VCCA	VCCA + 0.3	V

Note: IAH: Analog output sink current IAL: Analog output source current

AC CHARACTERISTICS

FOR OPERATION AT VCCD = 5.0 V

(V_{DD}=V_{CC}A=5.0V, Ta=-20 to +85℃)

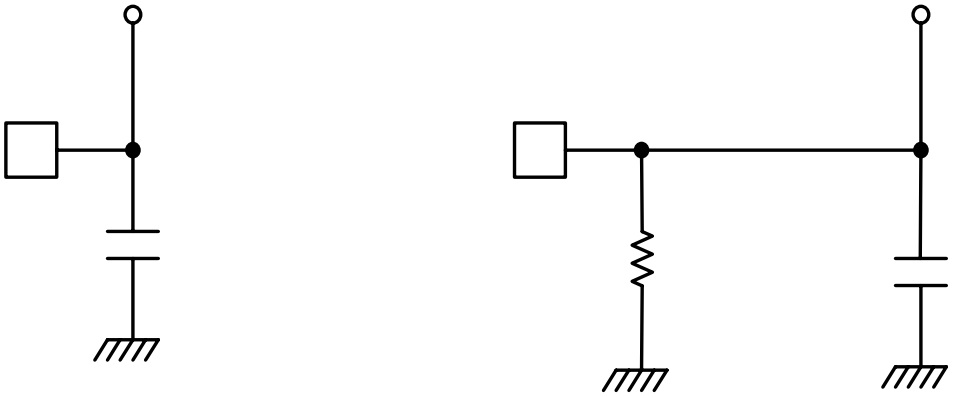
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Clock “L” level pulse width	tCKL	-	200	-	-	ns
Clock “H” level pulse width	tCKH	-	200	-	-	ns
Clock rise time	tCr	-	-	-	200	ns
Clock fall time	tCf	-	-	-	200	ns
Serial input setup time	tSSU	--	30	-	-	ns
Serial input hold time	tSHD	-	60	-	-	ns
Serial output delay time	tSOD	See “Load condition 1”	0	80	170	ns
CS input setup time	tCSU	-	100	-	-	ns
CS hold time	tCCH	-	200	-	-	ns
CS “H” level hold time	tCSH	-	100	-	-	ns
Data ouput enable time	tSO	-	-	-	200	ns
Data ouput float time	tSOZ	-	-	-	200	ns
Parallel input setup time	tPSU	-	30	-	-	ns
Parallel input hold time	tPHD	-	60	-	-	ns
Parallel ouput delay time	tPOD	See “Load condition 1”	-	100	170	ns
Analog output delay time	tAOD	See “Load condition 2”	-	30	100	μs
Power supply rise time	tR	-	-	-	50	ms
Power-on reset non-startup power supply variation	ΔVR	-	-10	-	10	V/μs

FOR OPERATION AT VCCD = 3.0 V *1

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Serial output delay time	tSOD	See “Load condition 1” *2	0	120	300	ns
Parallel output delay time	tPOD	See “Load condition 2” *3	-	120	300	ns

*1: Items not listed are identical to characteristics for VCCD = 5.0 V.
*2: Cascade connection enable at 1.5 MHz.
*3: Applied to D0 to D3 operation at VCCD

Load Conditions:



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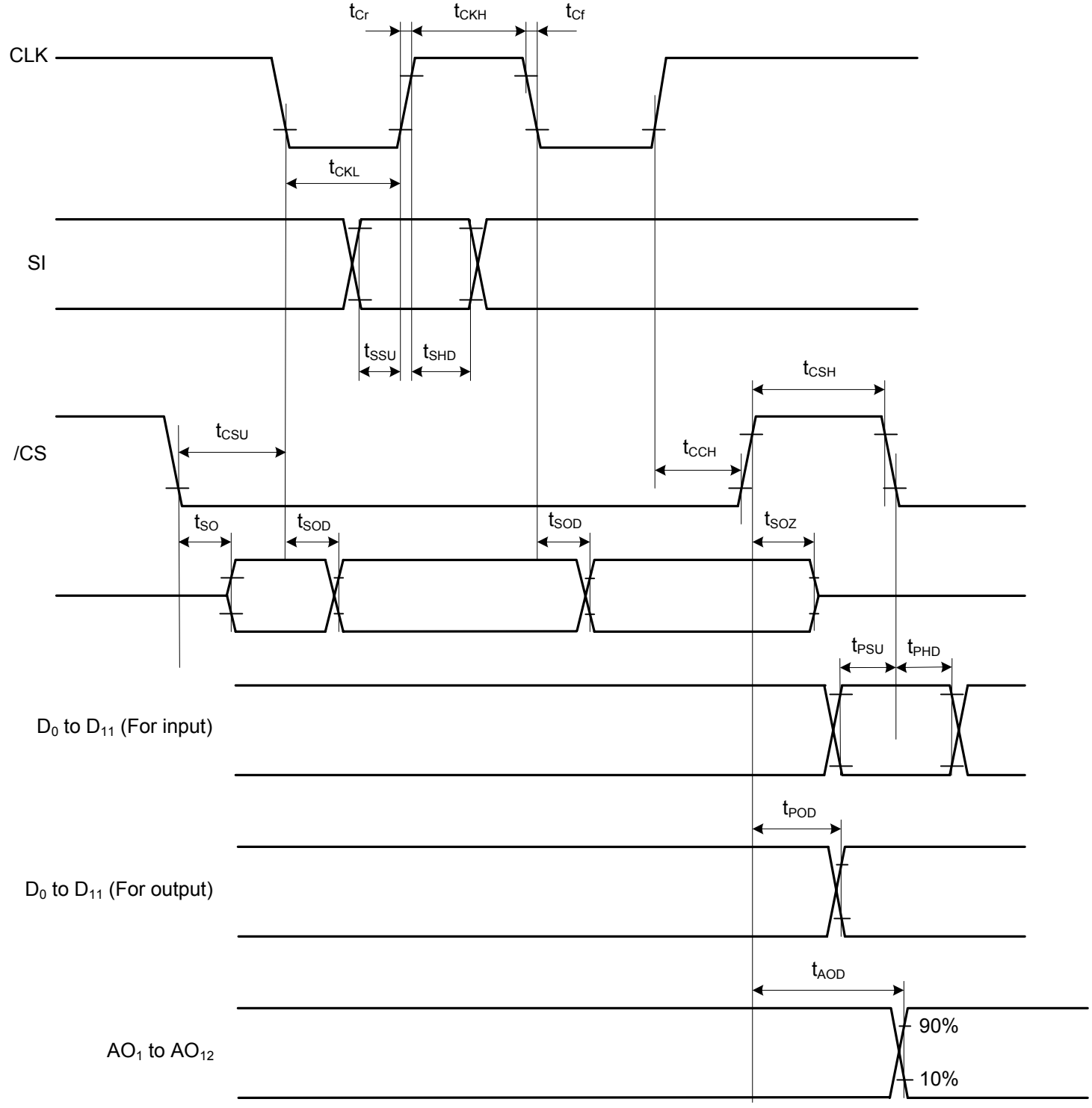
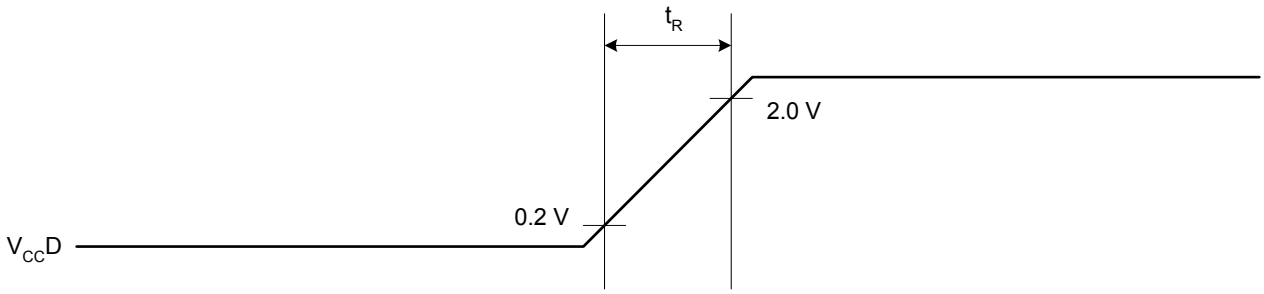
INPUT/OUTPUT TIMING (/CS METHOD)



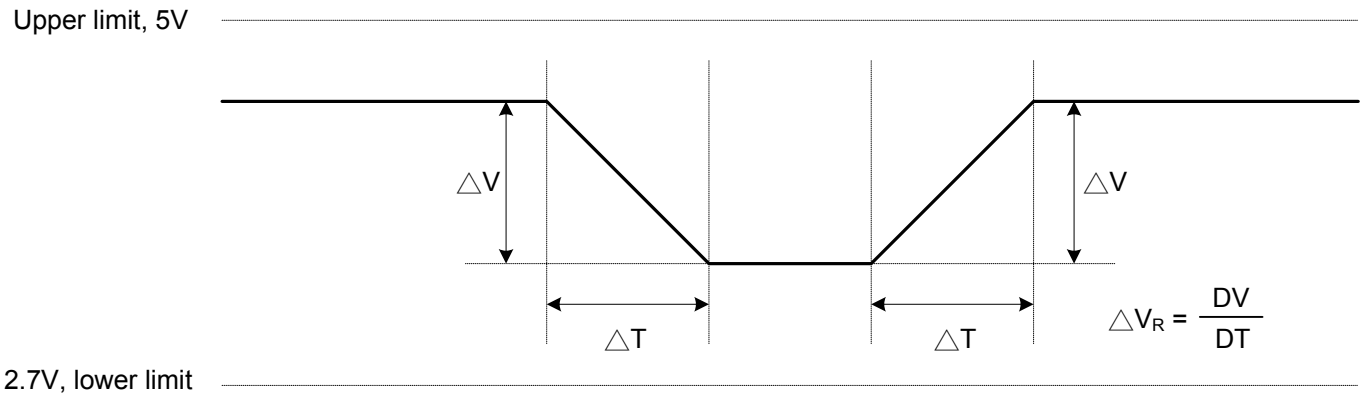
The decision level for CLK, SI, /CS, SO, and D0 to D3 is 80% and 20% of VCCD. The decision level for D4 to D11 is 80% and 20% of VCCA, and for AO1 to AO12 is 90% and 10% of VCCA.

POWER SUPPLY TIMING

Power-On Timing



Power-On Reset Non-Startup Supply Variation



ANALOG OUTPUT NOISE CHARACTERISTIC

(V_{DD}=V_{CC}D=V_{CC}A=5.0V, Ta=+25℃)

Parameter	Symbol	Conditions	Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
Digital supply noise reduction ratio	PSRD	fNOISE=1KHz	1	-	-	20	dB
Analog supply noise reduction ratio	PSRA	fNOISE=1KHz	1	-	-	20	dB
D/A supply noise reduction ratio	PSRDA	fNOISE=1KHz	1	-	-	0	dB
Operating noise	VN1	During serial transfer During analog operation During Hi-Z commands See “Operating Noise VN1”	2	-30	-	30	mV
I/O expander operating noise 1	VN2	Serial → parallel conversion See “I/O Expander Operating Noise 1 VN2” During digital-only pin operations During parallel → serial conversion ESR setting During digital input/digital output switching	2	-30	-	30	mV
I/O expander operating noise 2	VN3	During serial -> parallel conversion See “I/O Expander Operating Noise 2 VN3” During digital/analog capable pin operation ESR setting During digital output/digital output switching	2	-0.1	-	0.1	V

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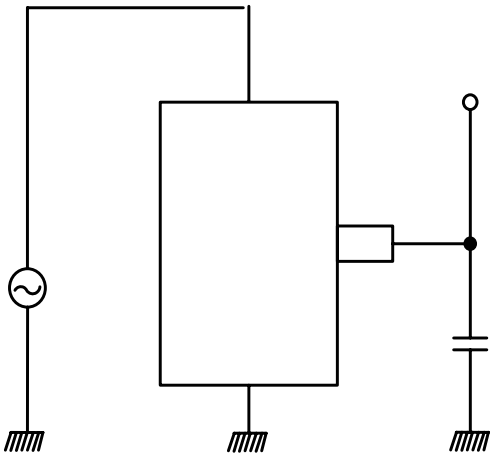
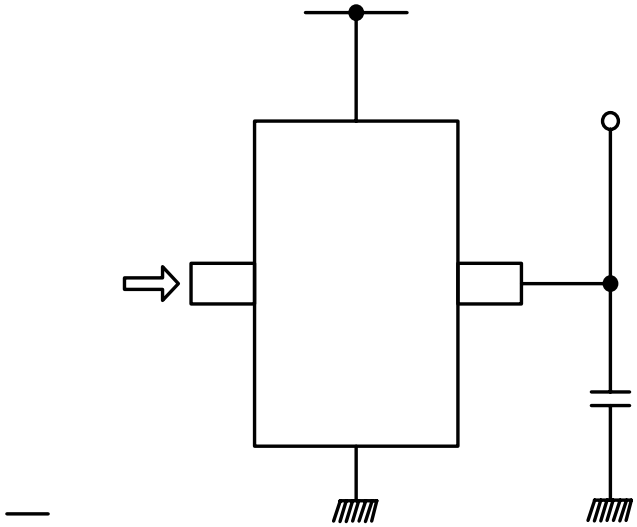
MEASUREMENT CONDITION 1



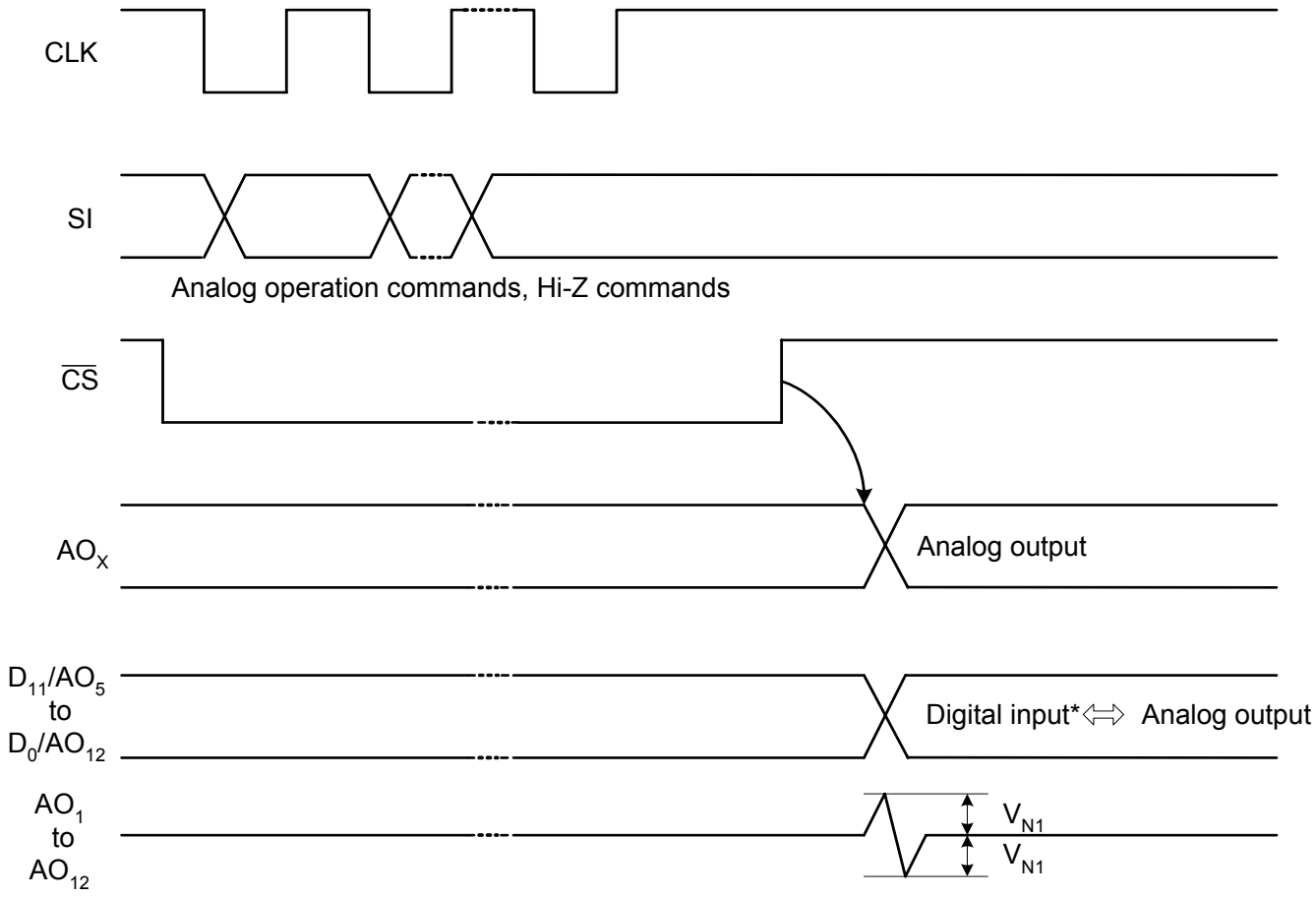
MEASUREMENT CONDITION 2



ANALOG OUTPUT NOISE DESCRIPTION

OUTPUT NOISE VN1

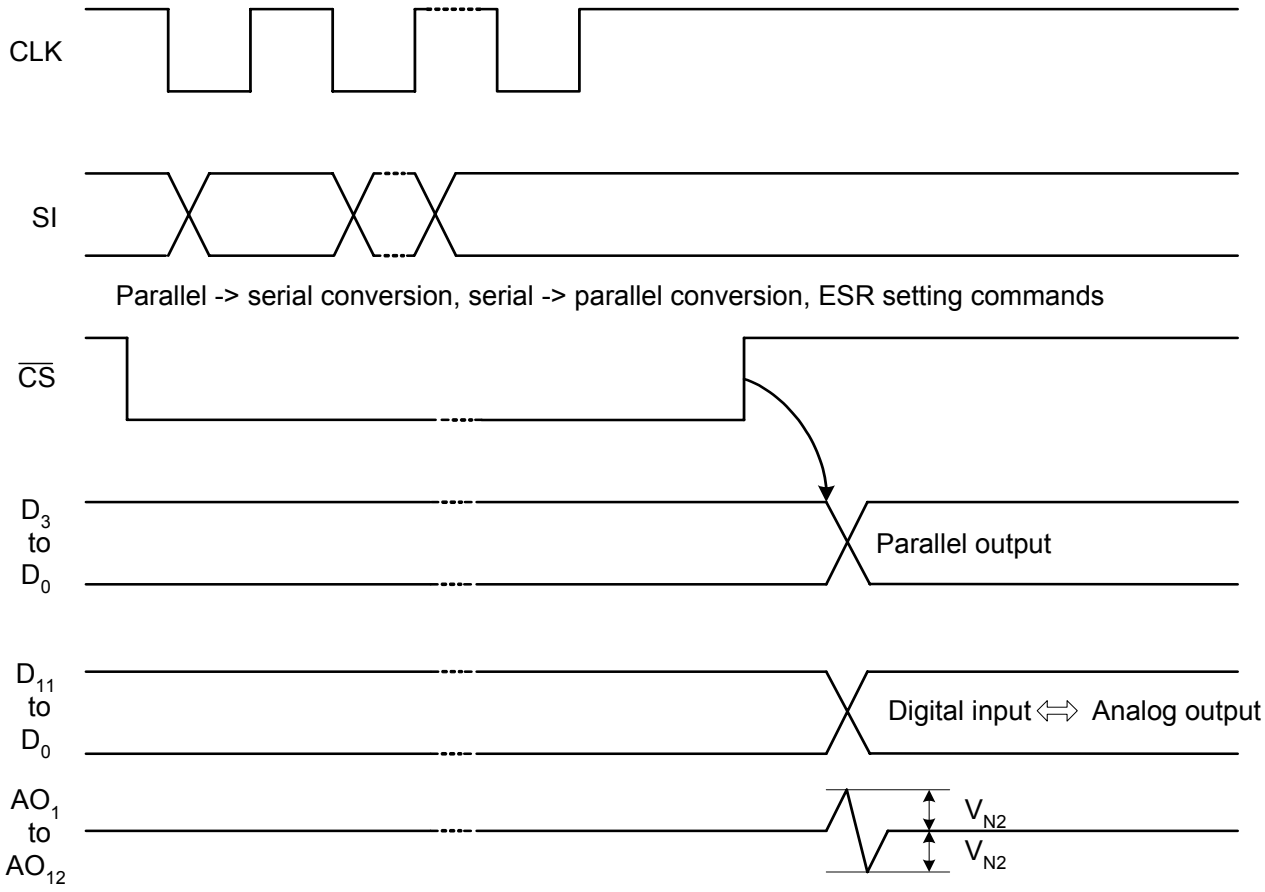
Noise to analog output during serial data transfer, analog operation, Hi-Z commands.



*: Hi-Z state = digital input state

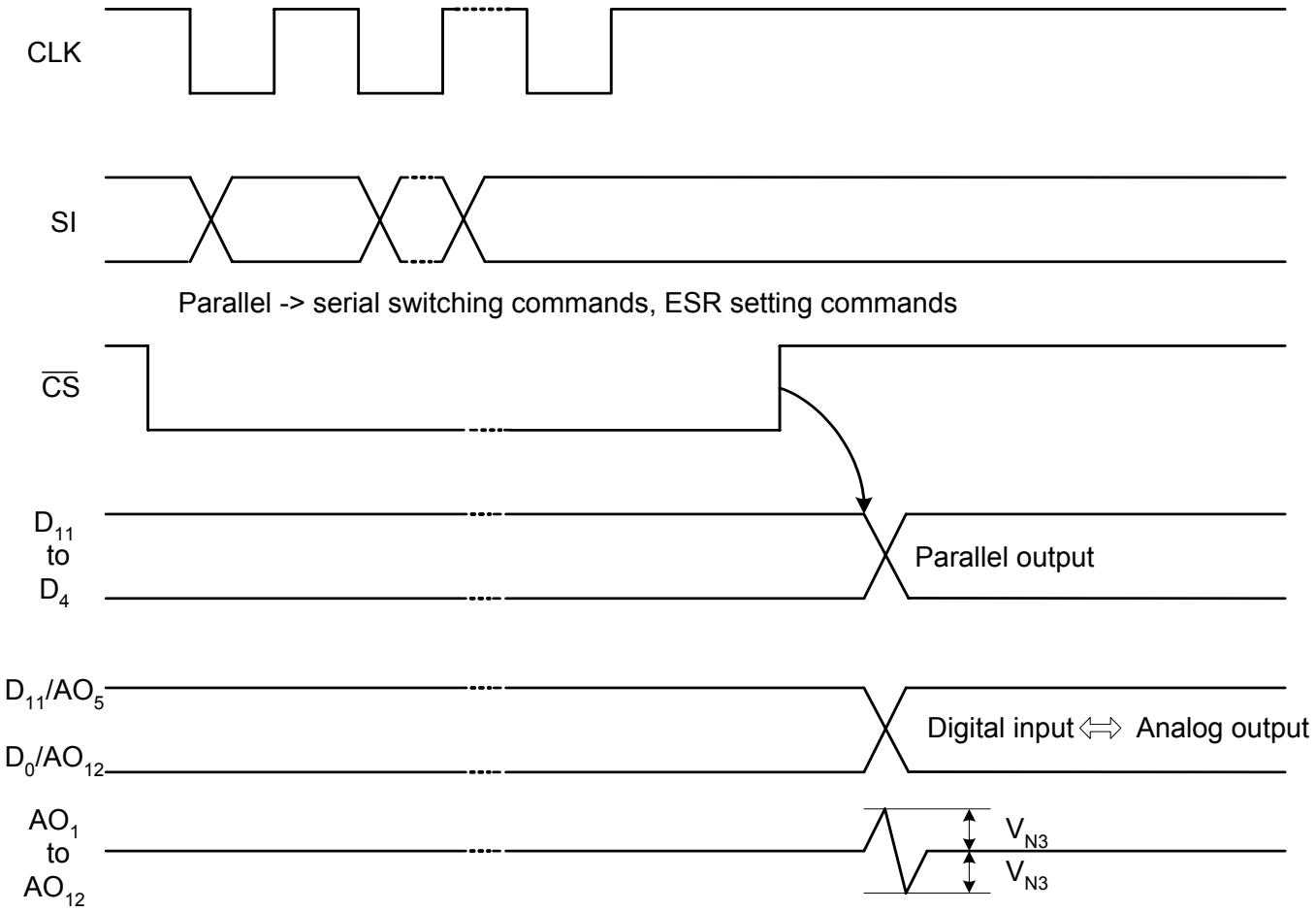
I/O EXPANDER OPERATION NOISE 1 VN2

Noise to analog during parallel → serial conversion commands, serial → parallel conversion command for digital-only pins, or ESR setting commands for switching between digital input and digital output.



I/O EXPANDER OPERATION NOISE 2 VN3

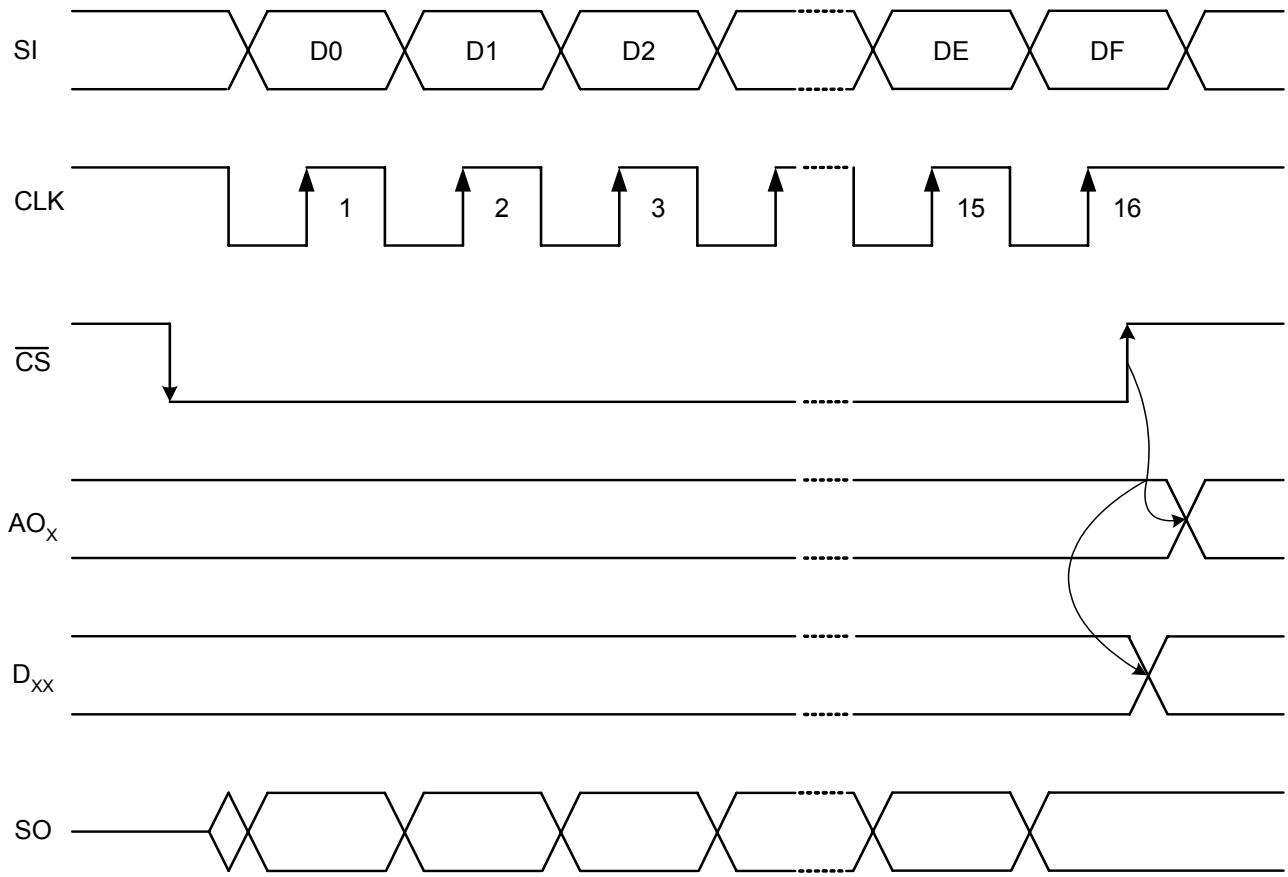
Noise to analog output during serial → parallel switching commands for digital-only pins, or ESR setting commands for switching between digital output and analog output.



DATA INPUT/OUPUT TIMING

PT8146 DATA INPUT/OUTPUT TIMING (SERIAL BUS FORMAT)

D/A Converter operation, and I/O expander (serial → parallel conversion) operation, and ESR writing operation



Data input is enabled at the falling edge of the /CS signal. 16-bit data is input, and the shift register command is executed at the rising edge of /CS.

In D/A converter operations, the analog output selected at the rising edge of /CS is the conversion result. In serial → parallel conversion, the digital output selected at the rising edge of /CS is the conversion result. In ESR write operation, ESR data is set and pin status determined at the rising edge of /CS.

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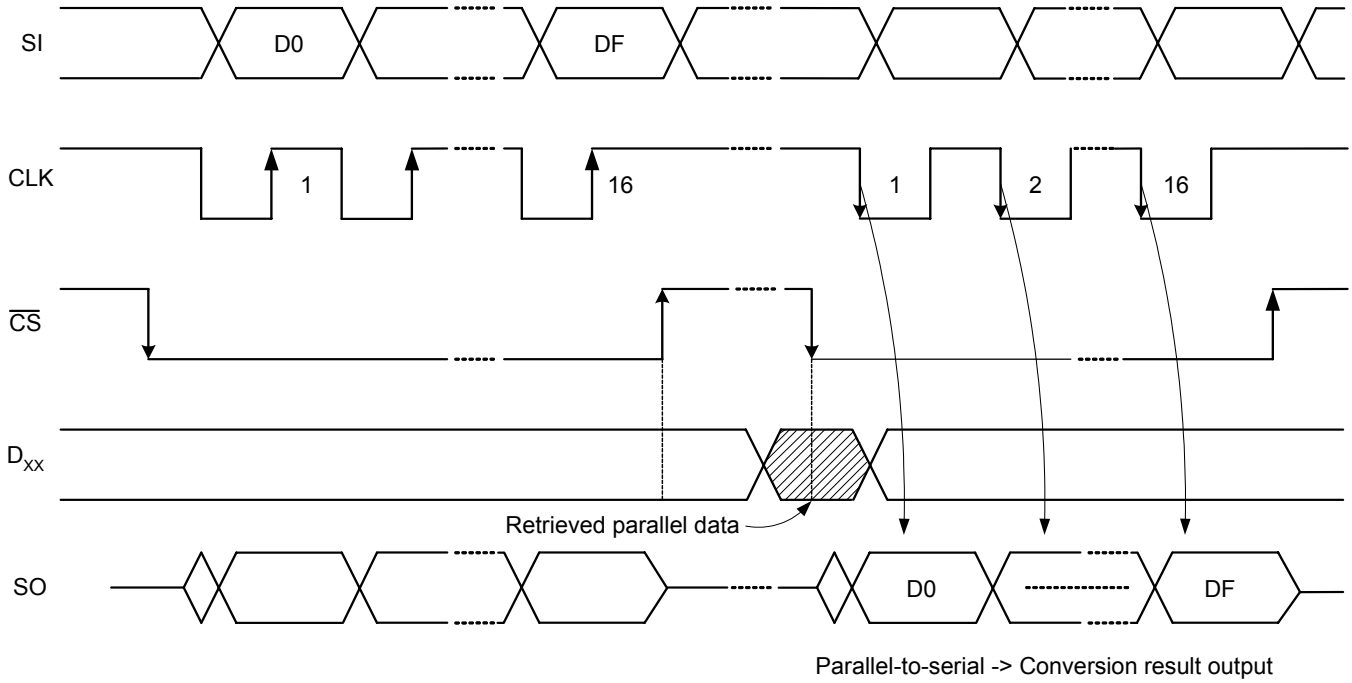
I/O expander (parallel -> serial conversion) operation



Parallel-to-serial -> Conversion result output

Data input is enabled at the falling edge of the /CS signal. 16-bit data (parallel → serial conversion commands) is input and commands accepted at the rising edge of /CS. AT the falling edge of /CS, data from the parallel input is loaded into bits D4 to DF of the shift register, and output from the SO pin timed to the falling edge of the CLK signal.

USAGE PRECAUTIONS

PREVENTING LATCH-UP

A condition known as “latch-up” may occur when the input or output pins of a CMOS IC device are exposed to voltages higher than VDD or VCCA or lower than GND voltage, or when voltages are applied to the device in excess of rated values for VCCD, VCCA, or VDD to GND voltages. Latch-up produces a rapid increase in power supply current, and may result in thermal destruction of elements. Users should take sufficient precautions to ensure that absolute maximum ratings are not exceeded at any time during use.

POWER SUPPLY PINS

The power supply should be connected to the VCCD, VCCA, VDD and GND terminals of the PT8146 with as low impedance as possible.

In addition, it is recommended that ceramic capacitors or approximately 0.1μF be connected as bypass capacitors between the VCCD, VCCA, and VDD terminals and the GND terminals.

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT8146	24 Pins, SSOP, 209mil	PT8146
PT8146 (L)	24 Pins, SSOP, 209mil	PT8146

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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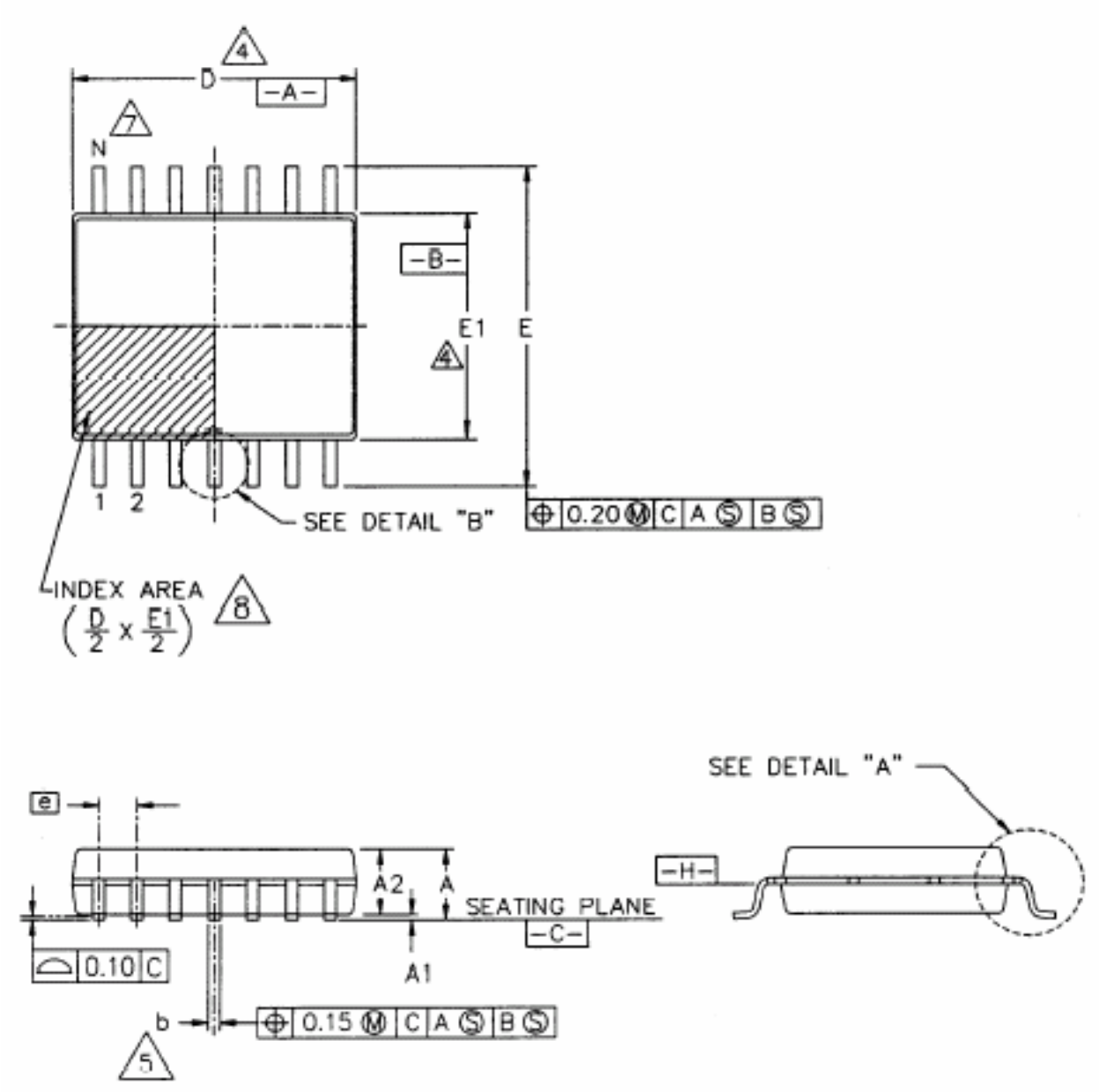
PACKAGE INFORMATION

24 PINS, SSOP, 209MIL



Symbol	Min.	Nom.	Max
A	-	-	2.0
A1	0.05	-	-
A2	1.65	1.75	1.85
*b	0.22	-	0.32
b1	0.22	0.30	0.33
c	0.09	-	0.25
c1	0.09	0.15	0.21
D	7.90	8.20	8.50
*E	7.60	7.80	8.00
E1	5.00	5.30	5.60
e	0.65 BASIC		
L	0.55	0.75	0.95
L1	1.25 REF		
N	24		
R1	0.09	-	-
θ	0°	4°	8°

Notes:
1. All dimensions are in millimeters.
2. Dimension and tolerancing per ANSI Y14.5M-1982.
3. D and E1 dimension do not include mold flash or protrusions, but do include mold mismatch and are measured at datum plane H, mold parting line. Mold flash or protrusion shall not exceed 0.20mm per side.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
5. To be determined at the seating plane – datum “C”.
6. “N” is the number of terminal positions.
7. A visual index feature must be located within the crosshatched area.
8. These dimensions apply to the flat section to the lead between 0.10 and 0.25mm from the lead tip.
9. Refer to JEDEC MO-150 variations AG
10. Dimensions marked with “*” are not complying with JEDEC product outlines.

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