TOSHIBA Power MOS FET Module Silicon N Channel MOS Type (Four L^2-π-MOSV in One)

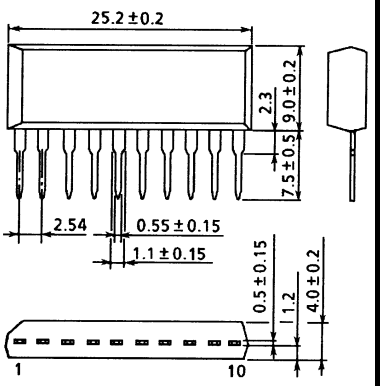
MP4209

Industrial Applications

High Power, High Speed Switching Applications
For Printer Head Pin Driver and Pulse Motor Driver
For Solenoid Driver

- 4-V gate drivability
- Small package by full molding (SIP 10 pins)
- High drain power dissipation (4-device operation)
  : P_T = 4 W (Ta = 25°C)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 0.28 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 3.5 S (typ.)
- Low leakage current: I_{GSS} = ±10 μA (max) (V_{GS} = ±16 V)
  I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement-mode: V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



1, 10 SOURCE
2, 4, 6, 8 GATE
3, 5, 7, 9 DRAIN
(PIN 1 AND PIN 10 IS DISCONNECTED INTERNALLY)

JEDEC	—
JEITA	—
TOSHIBA	2-25A1C

Weight: 2.1 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	3	A
	Pulse	I_{DP}	12	
Drain power dissipation (1-device operation, Ta = 25°C)		P_D	2.0	W
Drain power dissipation (4device operation, Ta = 25°C)		P_{DT}	4.0	W
Single pulse avalanche energy (Note 1)		E_{AS}	140	mJ
Avalanche current		I_{AR}	3	A
Repetitive avalanche energy (Note 2)	- device operation	E_{AR}	0.2	mJ
	4device operation	E_{ART}	0.4	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

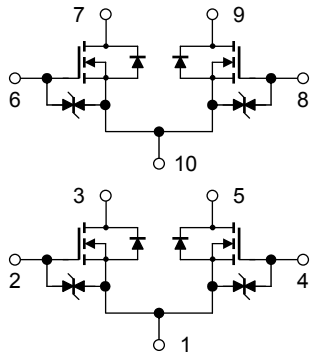
Note 1: Condition for avalanche energy (single pulse) measurement
V_{DD} = 50 V, starting T_{ch} = 25°C, L = 20 mH, R_G = 25 Ω, I_{AR} = 3 A

Note 2: Repetitive rating; pulse width limited by maximum channel temperature

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

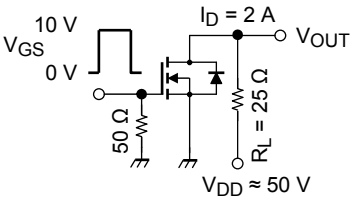
Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance from channel to ambient (4-device operation, Ta = 25°C)	$\Sigma R_{th\ (ch\text{-}a)}$	31.2	°C/W
Maximum lead temperature for soldering purposes (3.2 mm from case for t = 10 s)	T_L	260	°C

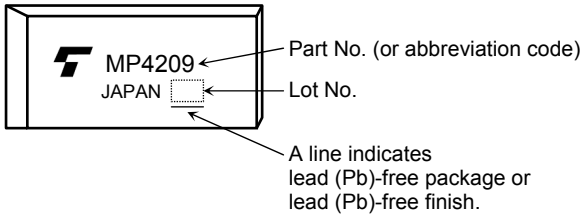
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 2 A	—	0.36	0.45	Ω
			V_{GS} = 10 V, I_D = 2 A	—	0.28	0.35	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2 A	1.5	3.5	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	—	280	—	pF
Reverse transfer capacitance		C_{rss}		—	50	—	pF
Output capacitance		C_{oss}		—	105	—	pF
Switching time	Rise time	t_r		—	20	—	ns
	Turn-on time	t_{on}		—	50	—	
	Fall time	t_f		—	40	—	
	Turn-off time	t_{off}	V_{IN}: t_r, t_f < 5 ns, duty ≤ 1%, t_w = 10 μs	—	170	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V I_D = 3 A	—	13.5	—	nC
Gate-source charge		Q_{gs}		—	8.5	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	5	—	nC

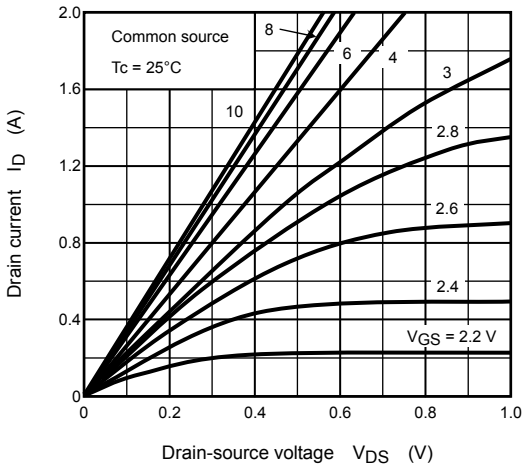
Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	3	A
Pulse drain reverse current	I_{DRP}	—	—	—	12	A
Diode forward voltage	V_{DSF}	I_{DR} = 3 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	I_{DR} = 3 A, V_{GS} = 0 V	—	100	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	0.2	—	μC

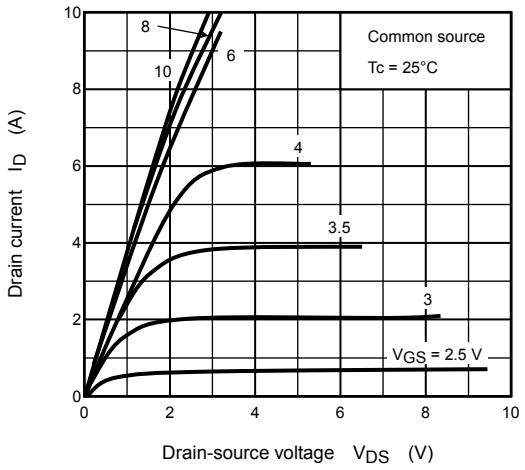
Marking



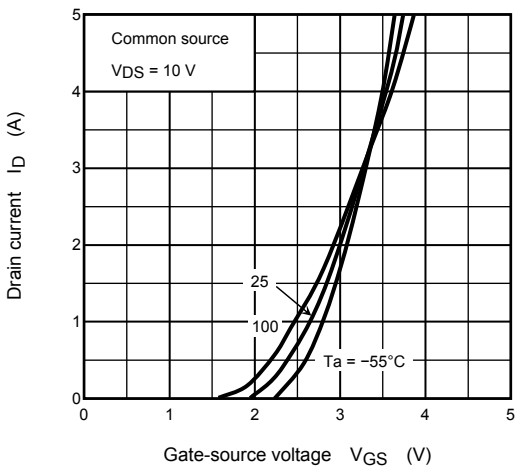
$I_D - V_{DS}$



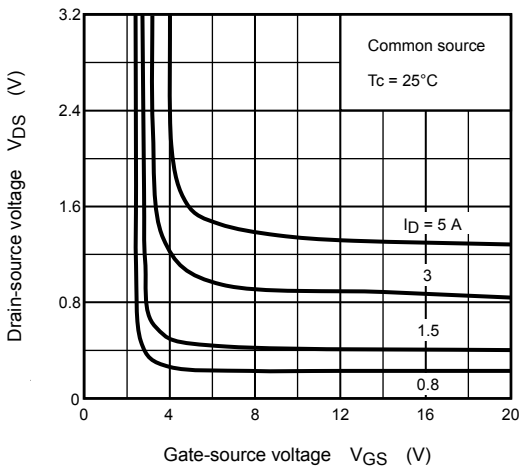
$I_D - V_{DS}$



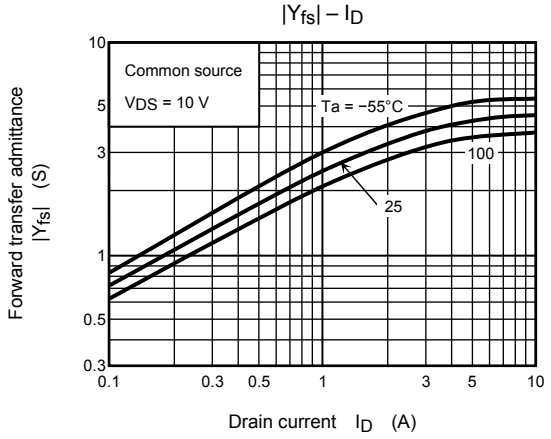
$I_D - V_{GS}$



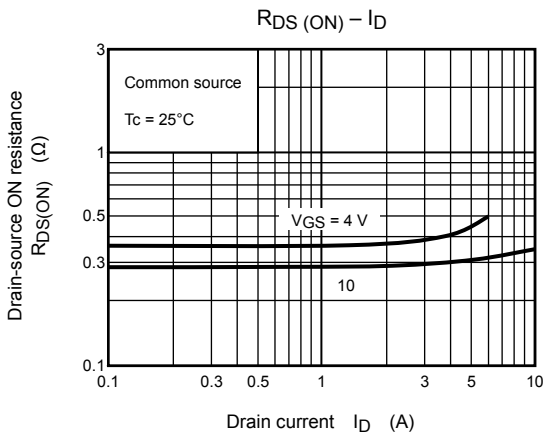
$V_{DS} - V_{GS}$



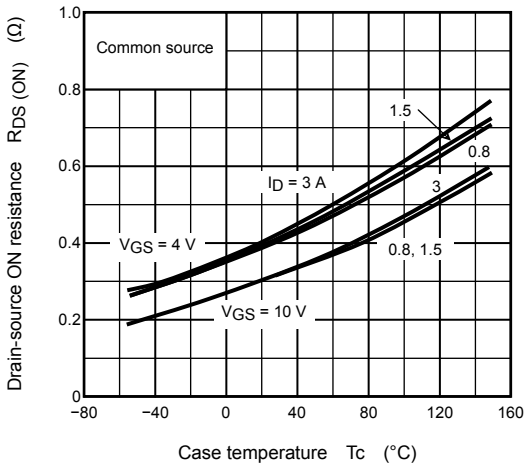
$|Y_{fs}| - I_D$



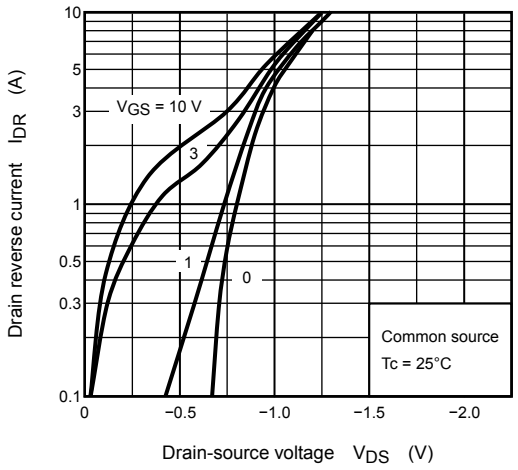
$R_{DS\ (ON)} - I_D$



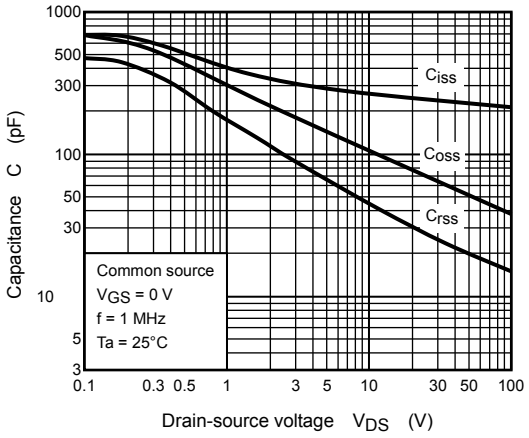
$R_{DS\ (ON)}$ – Tc



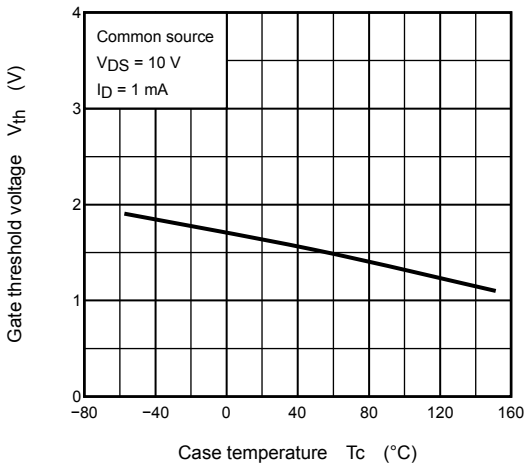
I_{DR} – V_{DS}



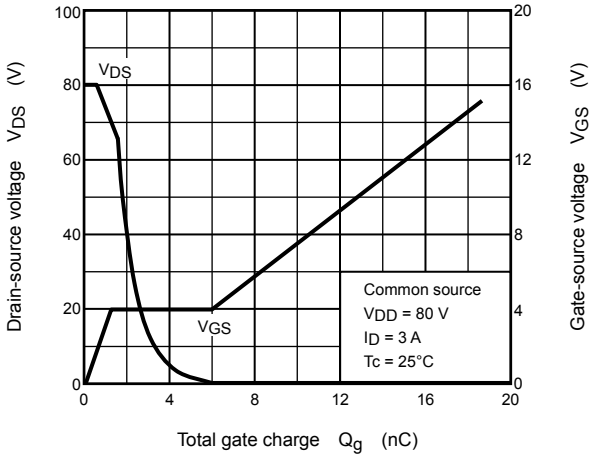
Capacitance – V_{DS}



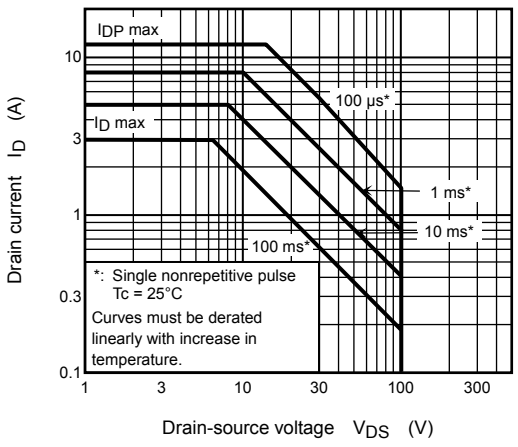
V_{th} – Tc



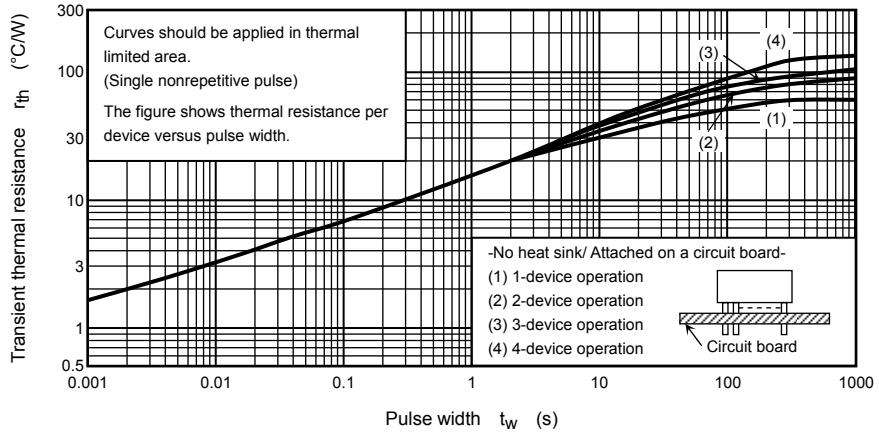
Dynamic Input/Output Characteristics



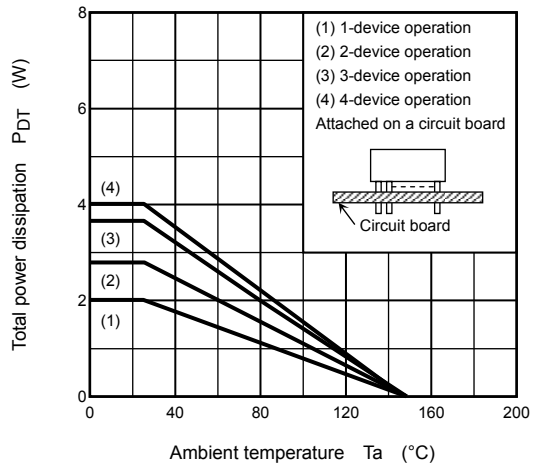
Safe Operating Area



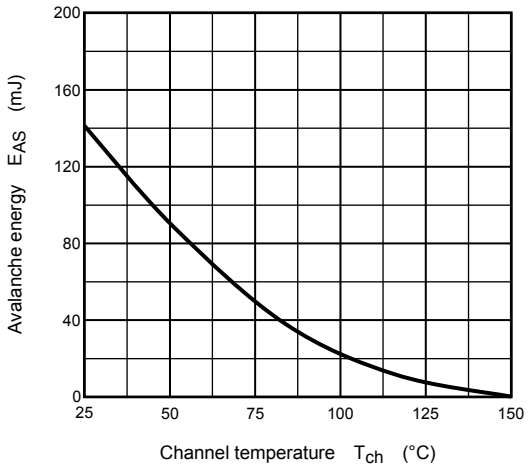
$r_{th} - t_w$



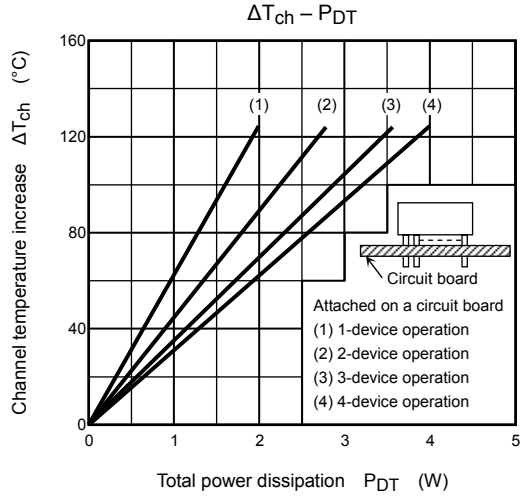
$P_{DT} - Ta$

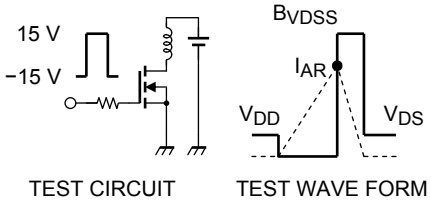


$E_{AS} - T_{ch}$



$\Delta T_{ch} - P_{DT}$





TEST CIRCUIT TEST WAVE FORM

Peak I_{AR} = 3 A, R_G = 25 Ω
V_{DD} = 50 V, L = 20 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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