LX1705

8+8W Stereo Filterless Class-D Amplifier

PRODUCTION DATA SHEET

DESCRIPTION

The LX1705 is a fully integrated stereo class-D CMOS audio amplifier. optimized for highly efficient operation and minimum system cost. The stereo BTL (Bridge-tied-load) configuration uses 3-level PWM modulation. This allows eliminating the LC filter to reduce the system cost and simplify the system design. The LX1705 outputs 8W into each of two channels with better than 90% efficiency. The entire signal path from input to output is differential to reject any sources of common-mode noise or distortion.

The part features on–board H-bridge output stages with low R_{DSON}. External bootstrap capacitors are all that is required to provide the gate drive to the all-NFET output stage since on-board bootstrap diodes are provided.

The LX1705 also features Mute and Standby modes, POP-free turn-on and turn-off, under-voltage lockout for both input supplies, and multi-level over-temperature protection.

The LX1705 is offered in a small thermally efficient footprint, low profile surface mountable 32-pin Micro Lead Quad Package (MLPQ) in 5mm x 5 mm.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

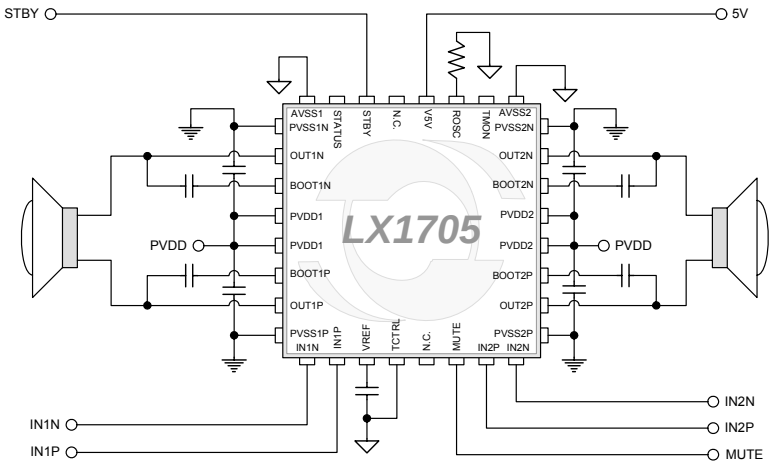
KEY FEATURES

- Filter Free Operation
- 6W +6W Output Power @ 8Ω load: THD+N < 1%
- High Efficiency > 90%
- Full Audio Bandwidth: 20Hz to 20kHz
- Low Distortion < 0.25% @ 30% Max Power, 1kHz
- High Signal-to-Noise Ratio: 90dB
- Wide Supply Voltage Range 5.0V ~ 15V
- 5mA Per Channel Typical Quiescent Current
- Turn ON/OFF POP Free
- Standby / Mute Feature
- Built-in Under Voltage Lockout
- Thermal Protection

APPLICATIONS

- LCD TV
- Car Navigation
- MP3 Docking Stations
- Portable Sound System

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	LQ Plastic MLPQ 32-Pin 5mm x 5mm RoHS Compliant / Pb-free
-40 to 85	**LX1705ILQ**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1705ILQ-TR)

Rev. 1.2, 2007-03-20

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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (PVDD) ..... -0.3V to 16.5V
BOOTP/N - PVDD ..... -0.3 to 16.5V
Bias Supply Voltage (V5V) ..... -0.3 to 6V
Input Pins (IN1P/N, IN2P/N ,TCTRL, STBY, MUTE) .....-0.3V to V5V + 0.3V
Output Pins (VREF, STATUS, ROSC, TMON).....-0.3V to V5V + 0.3V
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range.....-65°C to 150°C
Package Peak Temp. for Solder Reflow (40 seconds maximum exposure) ... 260°C (+0 -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to AVSS, except as noted. Currents are positive into, negative out of specified terminal.

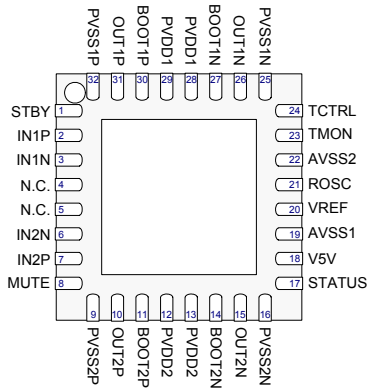
THERMAL DATA

LQ **Plastic MLPQ 32-Pin 5mm x 5mm**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	21.6°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

Pb-free 100% Matte Tin Pin Finish

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FUNCTIONAL PIN DESCRIPTION

Name	Function	Pin Number(s)	Description
PVSS1P PVSS1N PVSS2P PVSS2N	Power Ground	32 25 16 9	Power Ground for the two H-bridge output drivers, connect to power ground plane
PVDD1 PVDD2	Power Supply	28,29 12,13	Power Supply for the two H-bridge output drivers. Current draw will be up to 1.6A at 2 x 8W into 8Ω. These are peak currents when the part is run at maximum rated power on both channels.
V5V	Power Supply	18	Analog Power Supply for the analog signal processing section.
AVSS1 AVSS2	Analog Ground	19 22	Analog Ground for the analog signal processing section. Must be at the same potential as PVSS, connect at one point to the power ground plane.
IN1N IN1P IN2N IN2P	Analog Input	3 2 6 7	Differential analog audio inputs for each channel. The common mode voltage will be set by the LX1705 to around 2.25V.
OUT1N OUT1P OUT2N OUT2P	Digital Output	26 31 15 10	Differential high power audio outputs for each channel. Each output will swing between PVDD and PVSS. These outputs are driven by an on-chip H-bridge output driver which uses low R_{DSON} NFETs.
BOOT1N BOOT1P BOOT2N BOOT2P	Bootstrap	27 30 14 11	Bootstrap voltage pins which provide the high voltage needed to drive the upper NFET. A bootstrap capacitor should be placed between the respective output and these pins.
VREF	Analog Output	20	Typical 2.25V reference voltage which serves as an internal reference. An external compensation capacitor of at least 1uF should be connected between this pin and AVSS.
MUTE	CMOS Input	8	Logic level control which mutes the audio signal when high.
STBY	CMOS Input	1	Logic level control which places the chip into sleep mode when high.
STATUS	CMOS Output	17	Digital monitoring pin which is used to flag internal fault states. This pin will be synchronized with the internal clock to prevent glitches. See the STATUS flag list (below) for a summary of which conditions will force this pin to go high.
ROSC	Analog Input	21	Frequency control pin. A resistor between this pin and AVSS will set the oscillation frequency for the Class-D modulator.
TCTRL	Test Pin	24	Test purpose only, Connect to AVSS1
TMON	Test Pin	23	Test purpose only, left open.
N.C.	No connect	4,5	No Connect, pin is open

The STATUS pin will go high under any of the following conditions:

- STBY is high. This indicates that the chip is in “stand-by” mode.
- V5V is below the V5V UVLO threshold.
- PVDD is below the PVDD UVLO threshold.
- The die temperature is above about 140°C. This indicates that the part has gone in to gain foldback.
- A short circuit across the speaker has caused the output devices to shut off due to excessive temperature.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: P_{VDD} = 12V, P_{VSS} = A_{VSS} = 0V, V5V = 5V, R_{ROSC} = 24.9kΩ

Parameter	Symbol	Test Conditions	LX1705			Units
			Min	Typ	Max	
OSCILLATOR						
Oscillator Frequency	F_{OSC}	Varies with ROSC resistor value, value shown is for default conditions.	250	300	350	kHz
Temperature Stability		T_A = -40°C to 85°C		2		%
POWER SUPPLY						
Supply Voltage	PVDD		5	12	15	V
UVLO	PVDD	Start-up Voltage, Rising		4.5	4.9	
UVLO Hysteresis	PVDD			500		mV
+5V Supply	V5V		4.5		5.5	V
UVLO	V5V	Start-up Voltage , Rising		4.25	4.50	
UVLO Hysteresis	V5V			250		mV
Stand-By Current	I_{QQ}	For PVDD, STBY high		10	50	µA
Operating Current	I_{QQ}	For PVDD, STBY low, Mute high		10	30	mA
Stand-By Current	I_{QQ}5V5	For 5V5, STBY high		10		µA
Operating Current	I_{QQ}5V5	For 5V5, STBY low, Mute high		7	15	mA
Power Supply Rejection Ratio	PSRR	For PVDD @ 1kHz	55			dB
Reference Voltage[1]	VREF	C bypass = 1µF		2.25		V
GAIN						
Stage Gain	G	f = 1kHz; V_{MUTE} = 0V		26		dB
Mute Gain	G_{MUTE}	V_{MUTE} = 5V		-40		
OFFSET						
Output DC Offset	V_{OFFSET}	Measured Differentially. Channel + to Channel -		40		mV
INPUT STAGE						
Input Resistance	R_{IN}			22		kΩ
Common Mode Voltage	V_{CM}			2.25		V
OUTPUT STAGE						
MOSFET On Resistance	R_{DSON}	I_{DS} = 200mA		220		mΩ
THERMAL						
Thermal Shut Down Junction Temperature	T_{SD}			150		°C
Thermal Gain Fold-back Temperature	T_{FB}			140		
Thermal Recovery Temperature	T_{REC}			110		
MUTE / STBY						
MUTE Threshold	$MUTE_{TH}$	Mute Mode		V5V/2		V
STBY Threshold	$STBY_{TH}$			V5V/2		
STBY To Output Enable				5		ms

Note 1: Not ATE Tested.

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TYPICAL SYSTEM APPLICATION CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ TA ≤ 85°C except where otherwise noted and the following conditions: P_{VDD} = 12V, P_{VSS} = A_{VSS} = 0V, V5V = 5V, R_{OSC} = 25kΩ, R_L = 8Ω.

Parameter		Symbol	Test Conditions	LX1705 Min	LX1705 Typ	LX1705 Max	Units
AUDIO CHARACTERISTICS							
Output Power Stereo		P_O	THD+N < 1%		6		W
			THD+N <10%		8		
Total Harmonic Distortion Stereo		THD+N	P_{OUT} = 50% of Maximum Power, F_{IN} = 1kHz with diodes		0.2		%
			P_{OUT} = 50% of Maximum Power, F_{IN} = 1kHz No diodes		0.5		
			P_{OUT} = 1W, F_{IN} = 20Hz~20kHz		0.4		
Power Efficiency			P_{OUT} = Max, THD+N < 1%		90		%
Channel Crosstalk		V_{XTALK}	P_{OUT} = 1W, F_{IN} = 1kHz		-60		dB
Audio Bandwidth		BW	P_{OUT} = 1W, F_{IN} = 20-20kHz			3	
Stage Gain Stereo	High		V_{IN} = 200mV_{RMS}, F = 20Hz~20kHz		26		
	Low		V_{IN} = 2V_{RMS}, F_{IN} = 20Hz~20khz		-40		
Signal to Noise Ratio		SNR	F_{IN} = 1kHz @ 20Hz-20kHz A-weighted		90		dB
Output Noise Floor		V_N	Input short, non A-weighted @ 20Hz-20kHz		200		μV_{RMS}

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SIMPLIFIED BLOCK DIAGRAM

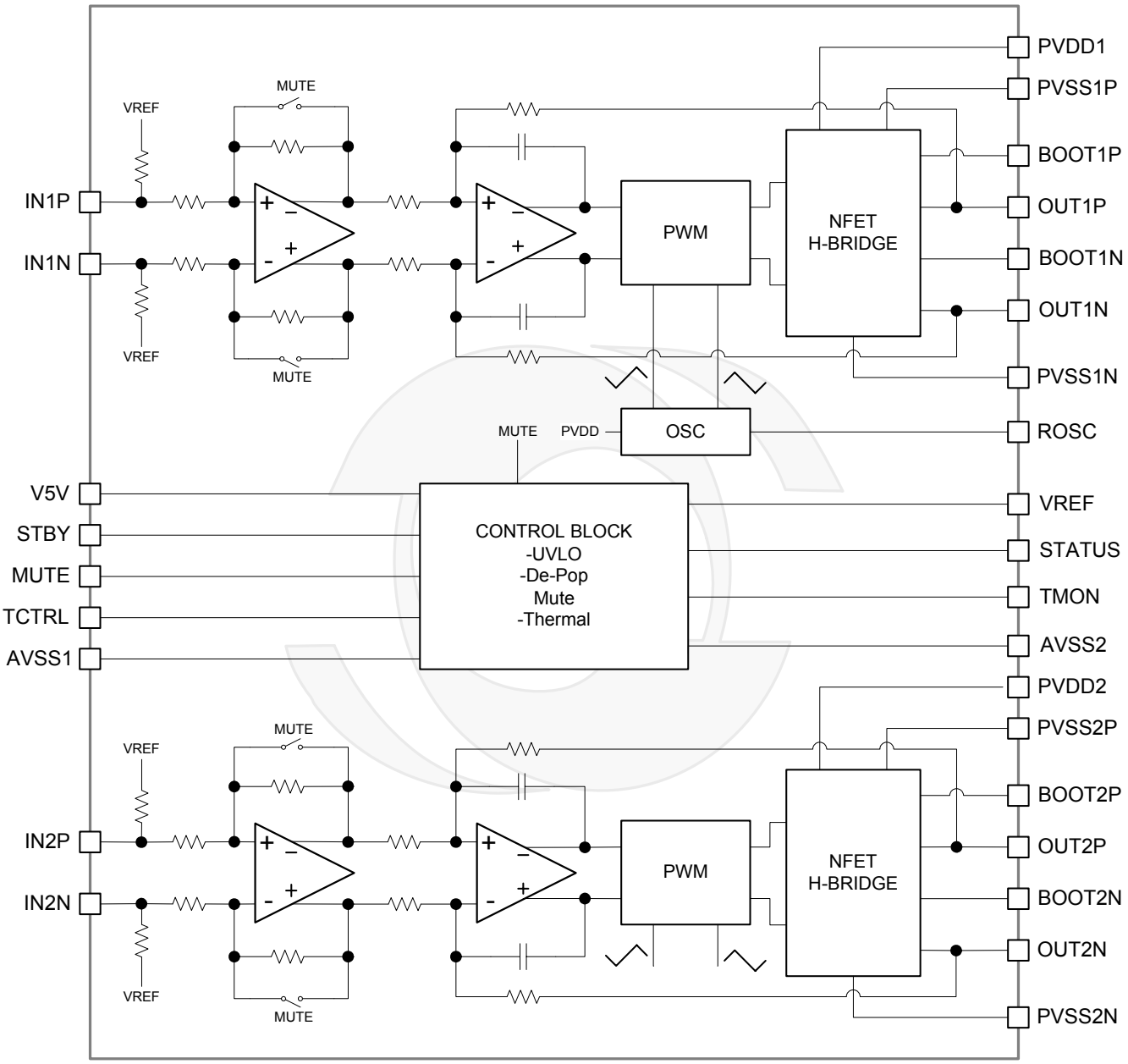

Figure 1 – Simplified Block Diagram

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TEST SYSTEM SET-UP

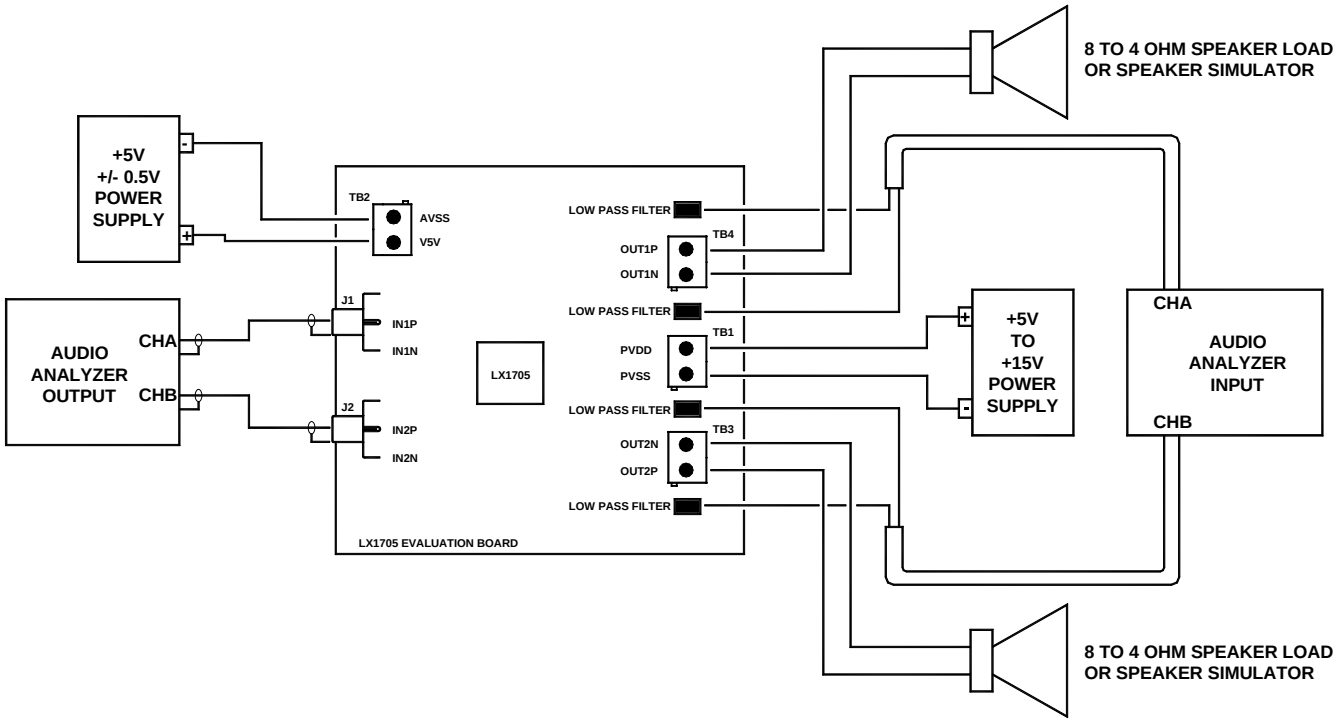

Figure 2 – System Test Set-up Diagram

Note: Speaker Load is simulated with 8Ω resistor in series with 66µH inductor for 8Ω speaker and 4Ω resistor in series with 33µH inductor for 4Ω speaker

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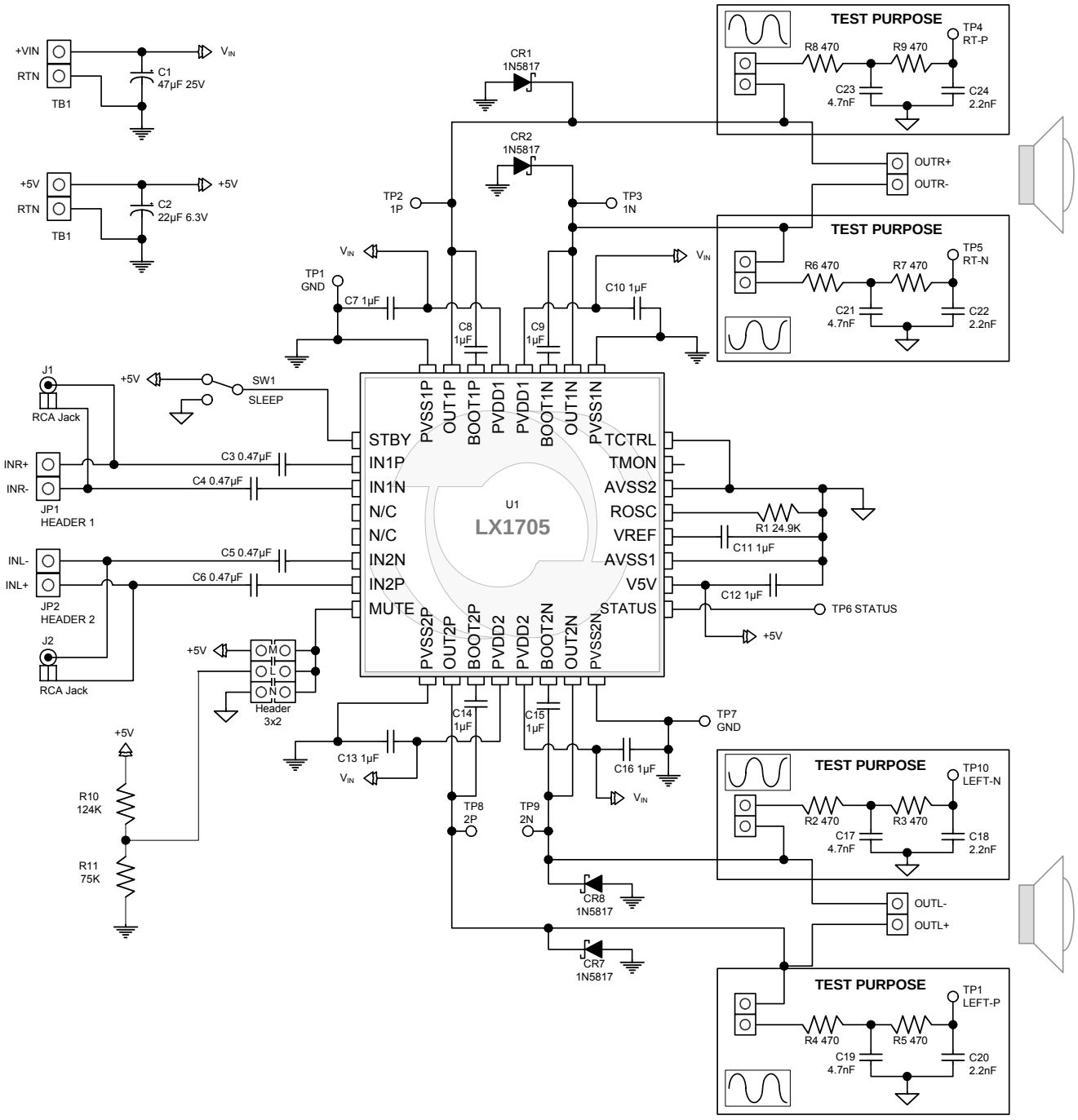
APPLICATION CIRCUITS



Note 1: CR1, CR2, CR7, CR8 can be used for lower distortion performance.

Figure 3 – Typical Application

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FUNCTIONAL DESCRIPTION

FILTERLESS CLASS-D MODULATION

The LX1705 drives each output between PVDD and PVSS using an all-NFET, bootstrapped, H-bridge driver for each channel. High efficiency is obtained by forcing all transistors to operate either completely on or completely off as required for a true class-D amplifier. The entire signal path from input to output is differential to reject any sources of common-mode noise or distortion. Even the triangle wave operates differentially. Filterless class-D modulation operates such that with no input signal, the outputs switch at the programmed clock frequency and are in-phase with each other. Because the two signals are identical, the differential signal to the speaker is zero. As a direct result, there is no requirement for a low-pass LC filter to present high impedance at the modulation frequency. This allows a cheaper and simpler audio amplifier to be designed. As the input signal goes positive, the duty cycle to the positive output increases while the duty cycle of the negative output decreases. This produces a net positive current flow into the load. A negative signal reduces the positive output duty cycles and increases the negative output duty cycle. The differential signal actually appears at twice the modulation frequency and alternates between +PVDD, 0, and –PVDD which allows the parasitic inductance of the load to effectively filter the switching signal so that only the audio band portion remains.

Because each speaker is driven by an in-phase signal, the common mode voltage to the speaker switches at the full PVDD amplitude at the clock frequency. This is a possible source of EMI radiation. Typically, a ferrite bead is placed with a small common-mode filter capacitor to reduce EMI generation by filtering the edges of the output signals.

NOISE-FREE TURN-ON AND OFF

Noise-free turn-on and off is accomplished by carefully sequencing the signal path when the amplifier is enabled or disabled. Prior to turn-on, the outputs are initially both at PVSS so there is no differential signal. The internal error amplifier is held in a reset condition so that the internal loop compensation components are “ready to go”. When the outputs begin to toggle, the audio signal path is muted for about 1.6ms. Following that time, the internal mute signal is de-asserted and the audio input signal is allowed to drive the pulse-width–modulator which then adjusts the output duty cycle as necessary to drive the speaker. At turn-off, the internal mute signal is asserted to silence the input audio signal. The outputs continue switching in this muted condition for about 0.6ms prior to being pulled low. Once the outputs are forced low, the error amplifier is reset so that the part is ready to begin a new power-up sequence. This scheme basically limits the pop noise at turn-on or off to be no larger than the differential offset voltage of the error amplifier.

AC-COUPLING AND BOOTSTRAP CAPACITORS

Input AC-coupling capacitors should be used to block any input DC and low frequency components below the desired low frequency corner. Since the input resistance to the LX1705 is 25kΩ, a 20Hz low frequency corner can be achieved with a 0.33µF AC-coupling capacitor. 1µF bootstrap capacitors are required at each output to supply the gate drive voltage for the upper level NFET in each half-bridge.

THERMAL OVERLOAD PROTECTION

The LX1705 protects itself by monitoring its operating temperature in two different ways. A general thermal protection scheme monitors the overall die temperature. Above 140°C, the amplifier gain is reduced by 6dB so that the audio signal is still amplified, but the on-chip power dissipation is halved. When the die temperature goes below 110°C, the amplifier gain is restored. Above 150°C, the LX1705 forces all outputs to PVSS so that no power is dissipated until the chip cools down to 110°C.

A dynamic thermal protection scheme operates by placing temperature sensors near each of the output devices. When a differential temperature rise of about 60°C occurs above the core die temperature, the outputs are disabled to protect the part. This provides short circuit protection for differential shorts across the output. Shorts to PVDD and ground (PVSS) are not protected.

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APPLICATION NOTE/PCB DESIGN GUIDELINE

OSCILLATOR

The value of ROSC selects the switching frequency, smaller values increase the switching frequency. See Figure 4, Typical Switching Frequency vs. ROSC. The recommended range of ROSC is between 17.5KΩ and 42.5KΩ

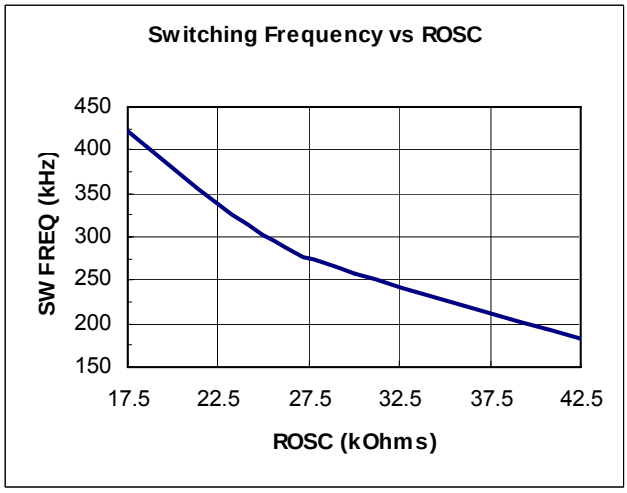

Figure 4 – Typical Switching Frequency vs. ROSC

BOOTSTRAP CAPACITORS

C8, C9, C14, and C15 are bootstrap capacitors for internal NMOSFETs gate drive voltage, they work together with internal diodes to provide sufficient gate drive voltage for upper MOSFETS. Those capacitors should be placed as close to the IC as possible.

BYPASSING CAPACITORS

C7, C10, C11, C12, C13, and C16 are bypassing capacitors for input supplies and internal reference voltage (VREF), nominal value is 1μF. These capacitors should be placed as close to the IC as possible, to guarantee low ripple and noise.

PCB DESIGN GUIDELINES

Component placement for the LX1705 should be done such that low-level inputs to the LX1705 are routed away from the high frequency switching outputs. Special care should be given to the bypass and bootstrap capacitors. Capacitors (C7, C10, C13, C16, C8, C9, C14, and C15 in the application schematic), should be placed as close to the IC as possible. If workable, they should be mounted on the same layer as the IC, with a direct connection to the IC on that layer. It is best not to use vias to establish the critical connection of these components to the LX1705. Bypass capacitors for V5V input, as well as VREF (C11 and C12 in the application schematic), should be mounted close to the IC as well.

One of the key efforts in implementing the MLP package on a pc board is the design of the land pattern. The MLP has a rectangular exposed thermal pad on the bottom surface of the package body. Electrical and mechanical connection between the component and the pc board is made by screen printing solder paste on the pc board and then reflowing the paste after placement. To guarantee reliable solder joints it is essential to properly design the land pattern to the MLP terminal pattern, exposed thermal pad, and thermal pad vias. There are two basic designs for PCB land pads for the MLP: Copper Defined style (also known as Non Solder Mask Defined (NSMD)) and the Solder Mask Defined style (SMD). The industry has had some debate on the merits of both styles and although Microsemi recommends the Copper Defined style land pad (NSMD). Both styles are acceptable for use with the MLP package. NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSMD by definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability. Due to the 0.5mm pitch of the LX1705's 5x5mm MLPQ package, it is recommended to design the solder mask around all pads on each side, rather than individual mask openings on each pad.

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APPLICATION NOTE/PCB DESIGN GUIDELINE (CONTINUED)

EXPOSED PAD PCB DESIGN

The construction of the Exposed Pad MLP enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder. The exposed pad is internally connected to the die substrate, so it is very important that the PCB substrate potential be connected to the same potential as AVSS.

The PCB thermal pad dimensions should be greater than the dimensions of the MLPQ thermal pad whenever possible; however adequate clearance must be met to prevent solder bridging to the outer pads. A minimum clearance of 0.2mm is recommended. If this clearance cannot be met, then the PCB thermal pad should be reduced in area.

THERMAL PAD VIA DESIGN

There are two types of on-board thermal pad designs: one using thermal vias to sink the heat to an inner layer utilizing a copper plane. Based on the JEDEC Specification (JESD 51-5) the thermal vias should be designed similar to Figure 5, with the following specifications:

Via Barrel diameter: 0.3mm
Min. Via Barrel plating: 0.025mm
Center to center spacing: 1.2mm

For the LX1705 5x5mm MLPQ package, there will be enough space for 9 vias. This method is recommended for use on a multilayer board, and will give the best thermal performance. Thermal vias may be used on a two layer board as well, with reduced performance.

Another method is the no via thermal pad, which uses only the copper pad as a heat sink, and relies on the PCB substrate material for thermal conduction. This type of thermal pad is good for a two layer board; however thermal performance will not be as good as the thermal via method on a multilayer board.

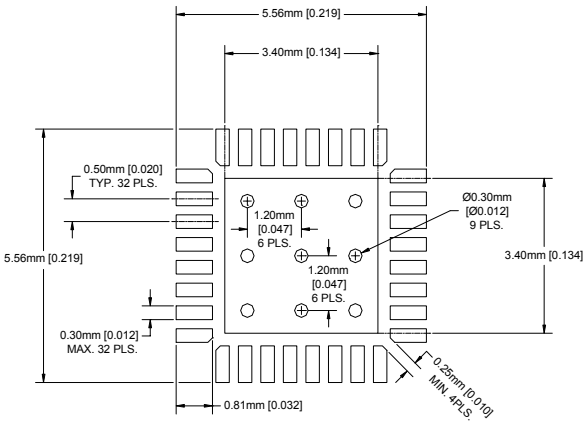

Figure 5 – Recommended Land Pad with Vias for 5x5mm LQ package

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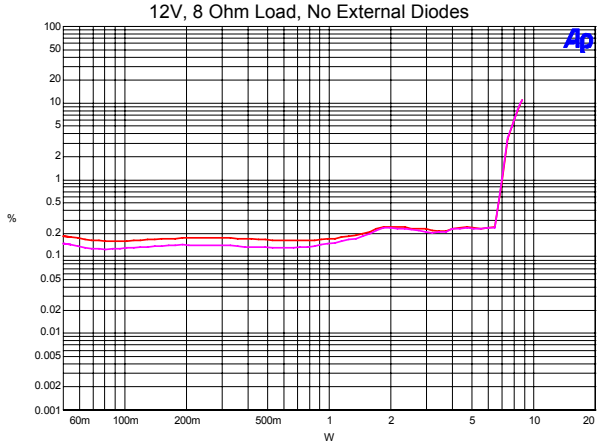
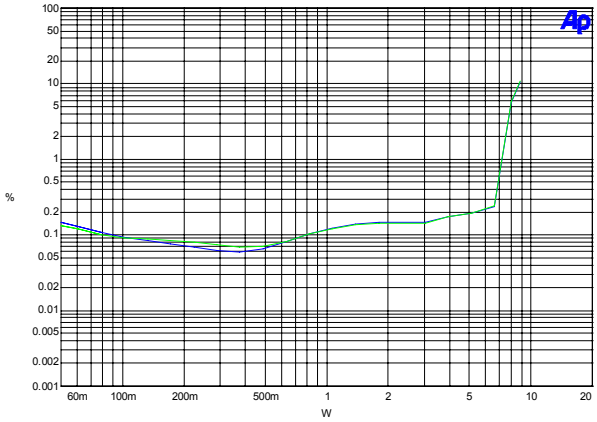
THD+N VS. OUTPUT POWER

12V, 8 Ohm Load, No External Diodes



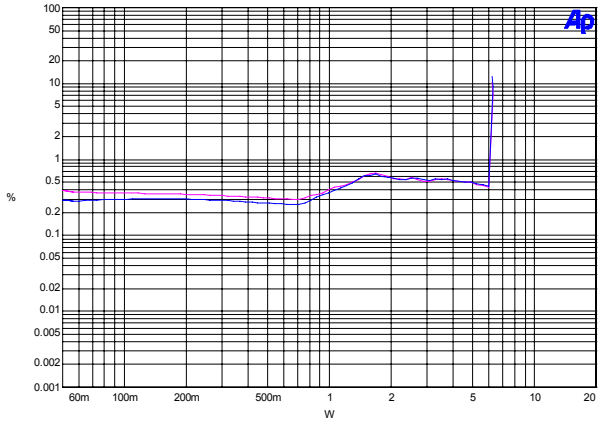
THD+N VS. OUTPUT POWER

12V, 8 Ohm Load with External Diodes



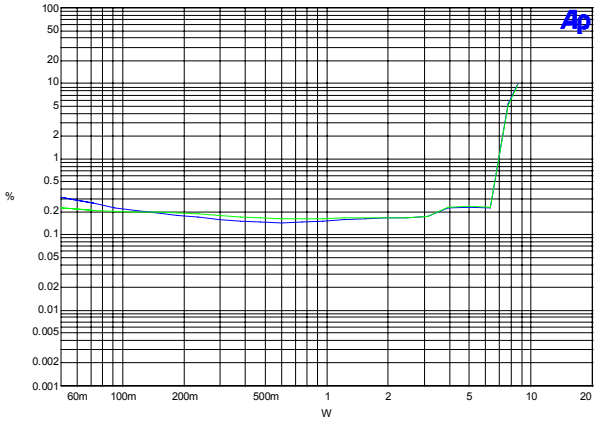
THD+N VS. OUTPUT POWER

9V, 4 Ohm Load No External Diodes



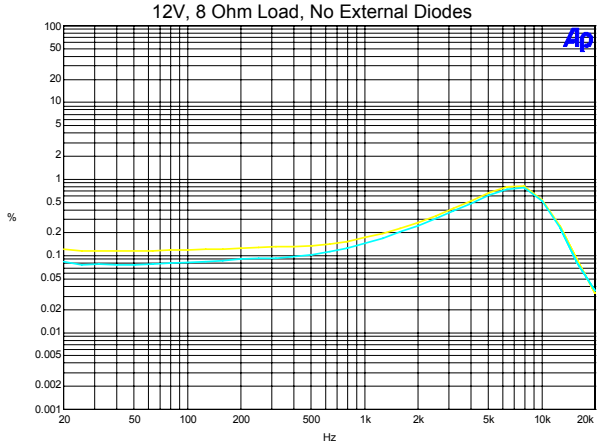
THD+N VS. OUTPUT POWER

9V, 4 Ohm Load, With External Diodes



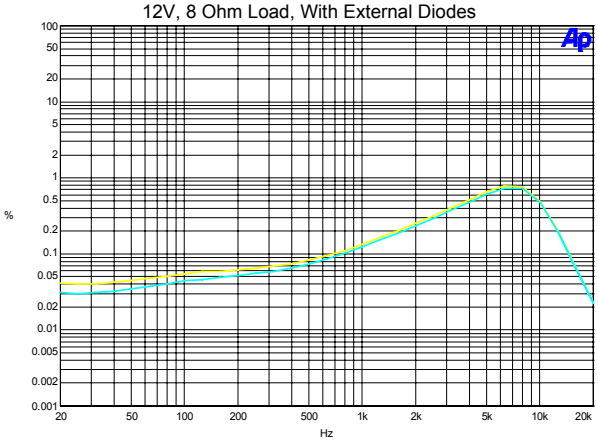
THD+N VS. FREQUENCY

12V, 8 Ohm Load, No External Diodes



THD+N VS. FREQUENCY

12V, 8 Ohm Load, With External Diodes



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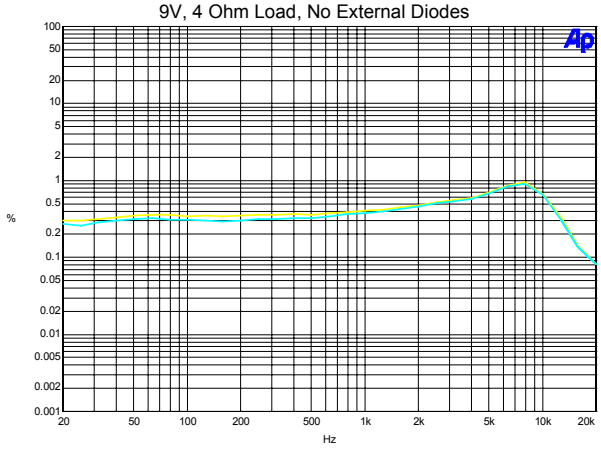
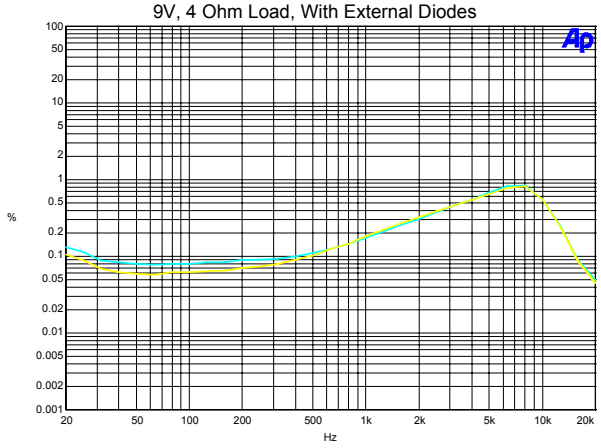
THD+N VS. FREQUENCY

9V, 4 Ohm Load, No External Diodes



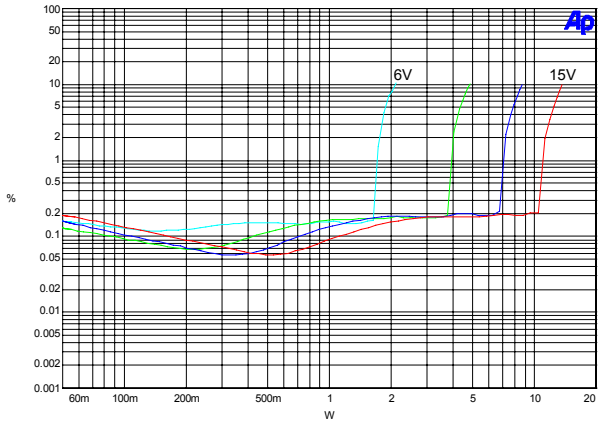
THD+N VS. FREQUENCY

9V, 4 Ohm Load, With External Diodes



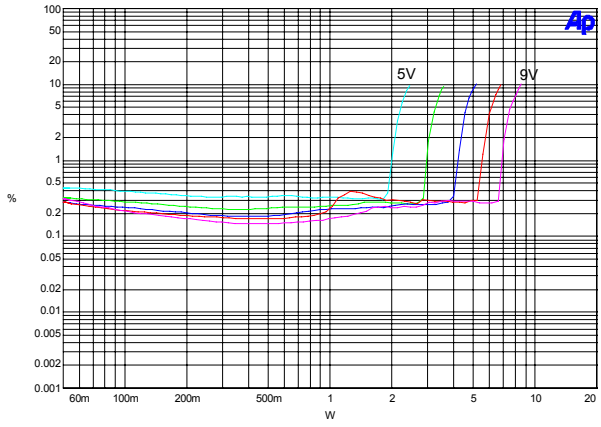
THD VS. POWER SUPPLY

8 Ohm Load, 6V, 9V, 12V, 15V



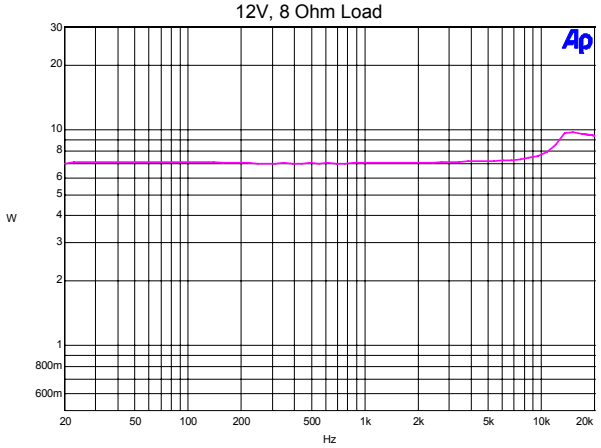
THD VS. POWER SUPPLY

4 Ohm Load, 5V, 6V, 7V, 8V, 9V



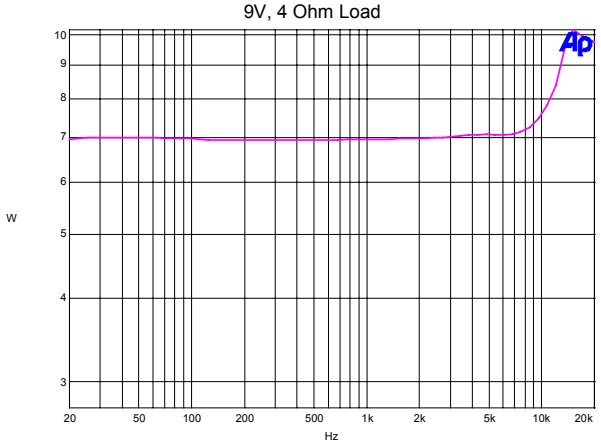
OUTPUT POWER BANDWIDTH @ 1% THD

12V, 8 Ohm Load



OUTPUT POWER BANDWIDTH @ 1% THD

9V, 4 Ohm Load



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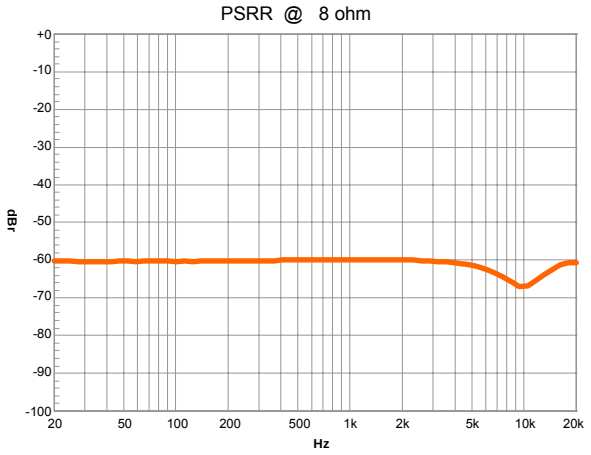
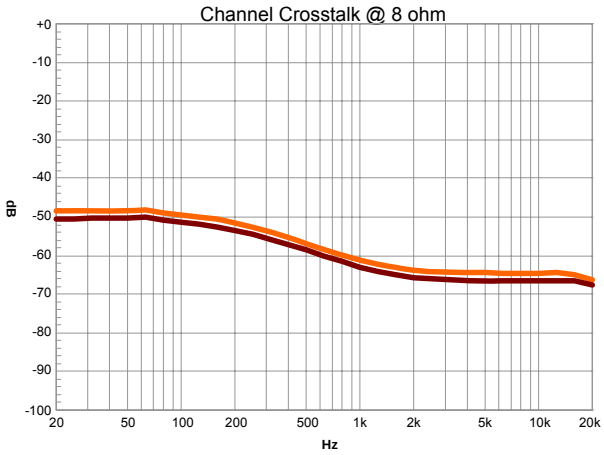
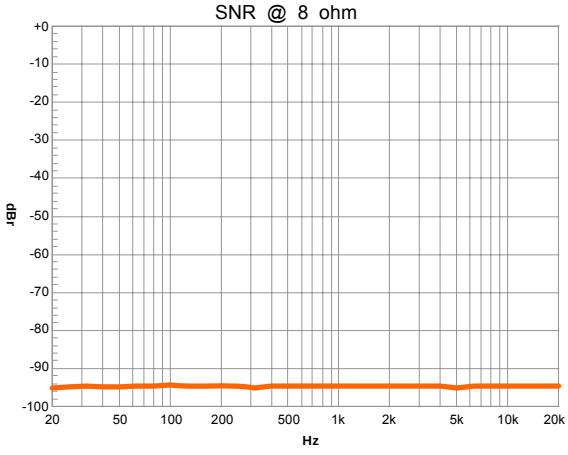
PSRR @ 8 OHM



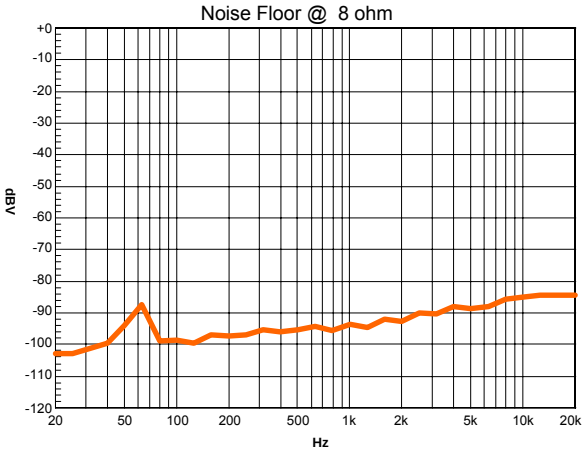
CHANNEL CROSSTALK @ 8 OHM



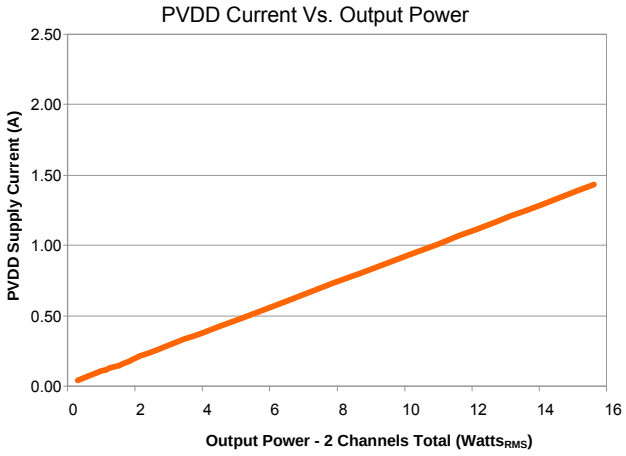
SIGNAL TO NOISE RATIO @ 8 OHM



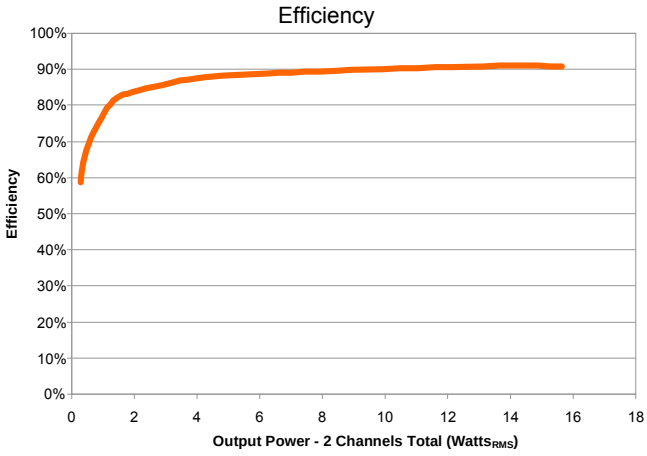
NOISE FLOOR @ 8 OHM



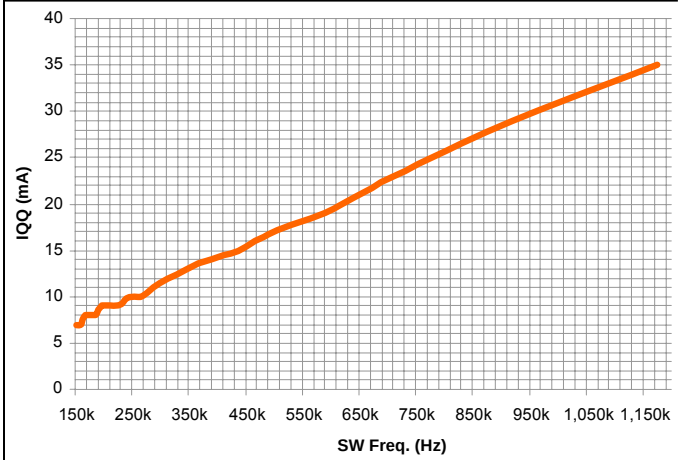
PVDD CURRENT VS. OUTPUT POWER



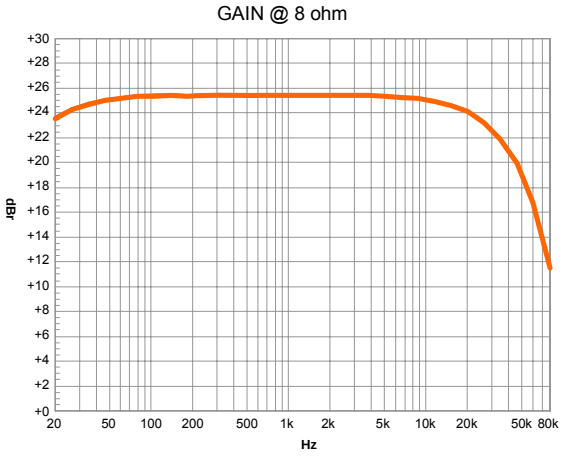
EFFICIENCY



IQQ VS. FREQUENCY



GAIN @ 8 OHM



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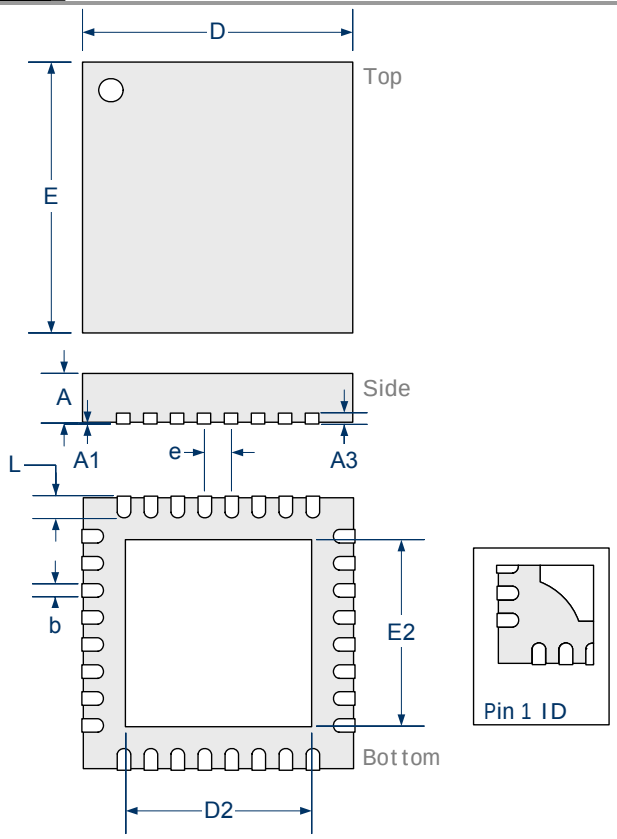
PACKAGE DIMENSIONS

LQ 32-Pin MLPQ Plastic (5x5mm EP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.30	3.55	0.130	0.140
E	5.00 BSC		0.197 BSC	
E2	3.30	3.55	0.130	0.140
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.020

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES