External Adjustable High Efficiency PFM Step-Down Converter

Features

- More than 90% efficiency and 100% duty cycle
- Wide input voltage range from 5V to 40V
- Integrated 1.6A on-chip P-channel MOS power switch
- 12µA typical shutdown current
- Less than 0.5V drop voltage at 500mA output current
- 0.2V to Vinput adjustable output range
- Controllable VOUT via an external Reference
- No control loop compensation required
- Improved current-limited PFM converter
- Maximum operating frequency > 300kHz
- Power good, reset or watchdog signal
- Under-voltage lockout and thermal shutdown
- -40°C to 125°C junction temperature
- Available in thermally enhanced TSSOP24 package

Applications

- Automotive electronics
- Minimum component step-down converter
- Sequenceable POL power supply systems
- Externally controllable LED power supply
- Externally controllable power amplifier

Brief Functional Description

The easy to use hysteretic step-down converter provides high efficiency over a wide load and input range with few external components.

An advanced PFM control scheme gives this device the benefits of a PWM converter with high efficiency at heavy loads, while using very low operating current at light loads to maintain an excellent behaviour over load variation.

Maximum switching frequency of 300kHz permits small external components and operation to 100% duty cycle allows the lowest possible dropout voltage. For optimal flexibility an external shunt resistor sets the maximum output current.

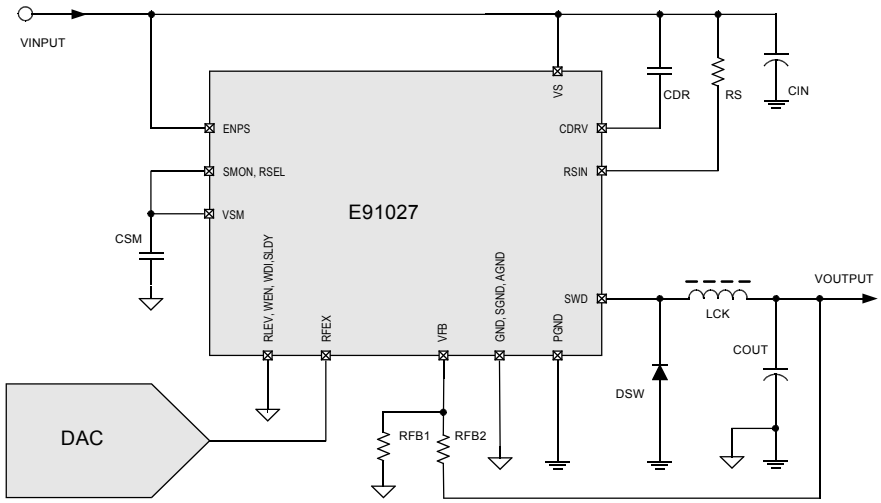
The converter contains a selectable internal reference with high or low voltage to regulate a wide range of output voltage or output current. The reference for output regulation can also be provided from an external source, like DAC.

A selectable power good, reset or watchdog signal is provided. An external capacitor sets the reset output pulse duration and / or watchdog trigger time.

An optional internal short delay timeout can greatly reduce the losses of the whole application in case of short or overload.

Very low shutdown and quiescent currents and the wide input voltage range makes the converter ideal for battery powered systems.

Typical Application



1 General

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2 Pinout

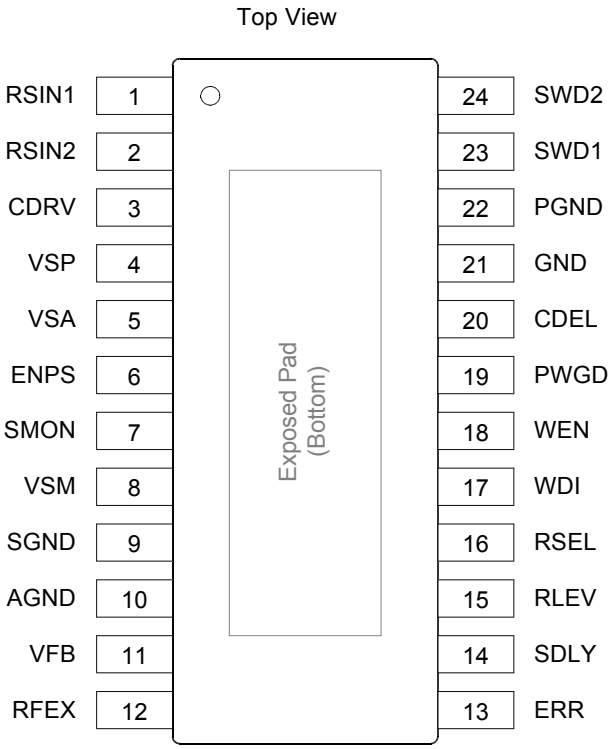
2.1 Pin Description

Name	Pin No.	Typ ①	Description
RSIN1	1	A, I, HV	PFM current sense comparator input and source terminal of internal P-MOSFET. Connect current-sense resistor between VS and RSIN. Internal power P-MOSFET is turned off when the voltage across this resistor is equal to or greater than the current limit trip level. External filter for extensive high frequency noise may be necessary.
RSIN2	2	A, I, HV	PFM current sense comparator input and source terminal of internal P-MOSFET. Connect current-sense resistor between VS and RSIN. Internal power P-MOSFET is turned off when the voltage across this resistor is equal to or greater than the current limit trip level. External filter for extensive high frequency noise may be necessary.
CDRV	3	A, O, HV	High side linear regulator output. CDRV provides a regulated output voltage that is VDRV below VS. The internal power P-MOSFET gate is driven between VS and CDRV. Bypass CDRV to VS with a high quality ceramic capacitor. There must be always a capacitor connected between VS and CDRV. In rare circuit configurations an external schottky diode must be connected between this pad and PGND to avoid malfunction through exessive substrat currents.
VSP	4	S, HV	Positive power stage supply input. Also acts as a voltage sense point for the internal current sense comparator. Bypass VSP to PGND with a ceramic capacitor in parallel with a low-ESR electrolytic capacitor.
VSA	5	S, HV	Positive analog power supply input. Bypass VSA to AGND with a ceramic capacitor.
ENPS	6	D, I, HV	Shutdown input. Connect ENPS to VS for normal operation. Drive ENPS to false to shut the part in shutdown. In shutdown mode most internal circuits are turned off. The thresholds are CMOS level compatible and a small pull-down current is drawn.
SMON	7	D, I, HV	Active-high SMON control input. When SMON is false the internal linear regulator is already working and can supply current to an external load. But the rest of the internal circuits are turned off. Thermal shutdown is already working. The thresholds are CMOS level compatible and a small pull-down current is drawn. Use this input for sequencing.
VSM	8	A, O	Internal linear regulator output. VSM provides power to the internal circuity and can supply a specified amount of current to an external load. Bypass VSM to AGND with a high quality ceramic and parallel low-ESR tantal or equivalent, capacitors. All electrical specifications are valid until VSM is settled only.
SGND	9	S	Signal ground. SGND requires a short low noise connection to ensure good load regulation. The internal reference is referred to this ground, so errors at this pin are multiplied by the error comparator.
AGND	10	S	Analog ground. AGND requires a short low noise connection to ensure good VSM regulation. The low drop preregulator powers most of internal circuits.
VFB	11	A, I	Feedback input is the error comparator inverting input, and controls output voltage by adjusting switch duty cycle. VFB also aids power good detection circuit. Connect a resistor divider between VOUTPUT, VFB and SGND for the desired output voltage. In case of outer loop current regulation connect VFB to an external sense resistor.
RFEX	12	A, I	If enabled, external reference input is the error comparator noninverting input reference and controls the voltage VOUTPUT. In this case power good, reset and watchdog functions are disabled.
ERR	13	D, O	Open drain logic true output for indicating an internal fault. Errors are VSM under voltage lockout, driver voltage low and ASIC over temperature.
SDLY	14	D, I	When true, the PFM inserts an additional delay after an overcurrent pulse. The switching frequency decreases due to the larger duty cycle. This function reduces greatly the power consumption in case of a fault. The thresholds are CMOS level compatible.
RLEV	15	D, I	When false selects internal high-reference voltage and when true internal low-reference voltage. The thresholds are CMOS level compatible.
RSEL	16	D, I	When false selects internal reference generator and when true external reference voltage input at port RFEX. The thresholds are CMOS level compatible.
WDI	17	D, I	Watchdog trigger input. The rising edge of an input pulse resets the watchdog. This function is with internal references available only. The thresholds are CMOS level compatible.

Name	Pin No.	Typ ①	Description
WEN	18	D, I	Watchdog enable input. When true watchdog function is enabled. This function is with internal references available only.The thresholds are CMOS level compatible.
PWGD	19	D, O	The PWGD open drain output stays low for undervoltage condition at VFB and in case of internal error. Use this output for sequencing or in combination with an external timing capacitor at CDLY for reset delay timer function and watchdog timeout. This function is with internal references available only.
CDLY	20	A, I	Delay timing capacitor input. Connect a timing capacitor between CDLY and GND to set the reset output duration and watchdog trigger time.
GND	21	S	ESD structure and substrat ground return for internal circuits. Make a short connection between this port and the other grounds. A low impedance circuit ground plane is highly recommended.
PGND	22	S	High current power ground return for internal circuits. Make a short connection between this port, the free-wheel diode, input and output capacitors. Due tue high frequency currents, a low impedance circuit ground plane is highly recommended.
SWD1	23	A, O, HV	Drain output of the internal power P-MOSFET. Connect the external choke and the free-wheel diode to this port.
SWD2	24	A, O, HV	Drain output of the internal power P-MOSFET. Connect the external choke and the free-wheel diode to this port.

① D = Digital, A = Analog, S = Supply, I = Input, O = Output, HV = High Voltage (max. 40V)

2.2 Package Pinout



Exposed Pad must be connected to GND

Figure 2.2-1: Pinout TSSOP24 ADT-1

3 Basic Blockdiagram

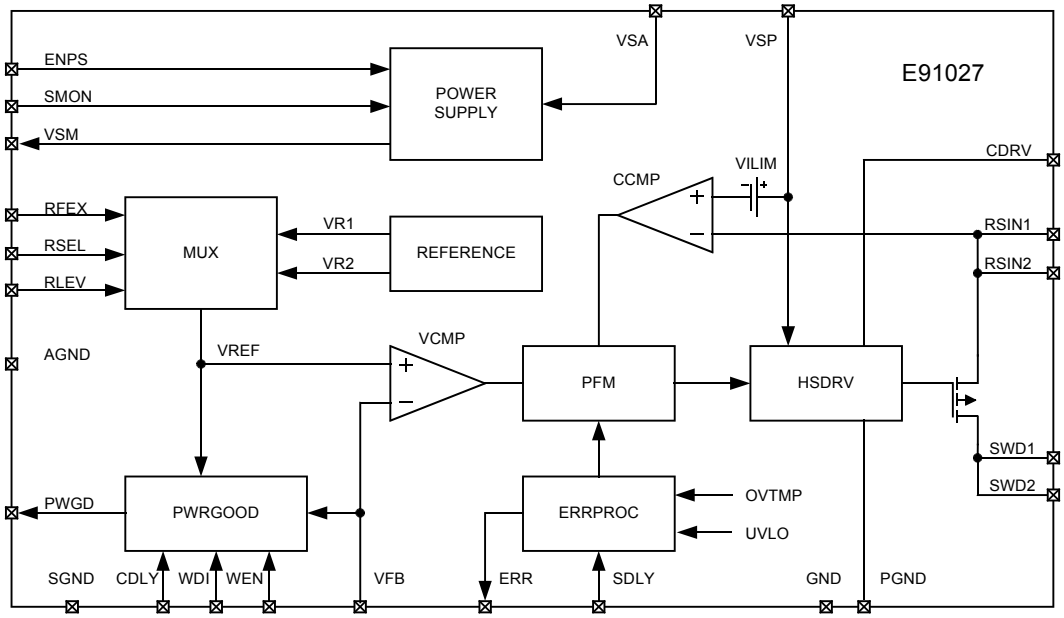


Figure 3-1: Blockdiagram

4 Operating Conditions

4.1 Absolute Maximum Ratings

Stresses beyond those listet under „absolute maximum ratings“ may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated above is not implied. Expose to absolute maximum rated conditions for extended periods may effect device reliability and are not permitted.

AGND, SGND, PGND and Exposed Pad must be soldered to GND and stand for future reference within text as GND.

VSA and VSP must be always external interconnected and stand for future reference within text as VS.

RSIN1 and RSIN2 must be always external interconnected and stand for future reference within text as RSIN.

SWD1 and SWD2 must be always external interconnected and stand for future reference within text as SWD.

Parameter	Condition	Symbol	Min.	Max.	Unit
Supply voltage input VS		VS	-0.3	40	V
Supply voltage input VS (Load dump)	tw<400ms	VSmax	-0.3	45	V
VSM to GND		VSM	-0.3	5.5	V
IVSM		IVSM	0	-20	mA
CDRV to GND		VCDRVG	-0.3	VS	V
CDRV to VS		VCDRV	VS-7.0	VS	V
RSIN to VS		VRSIN	VS-1.0	VS+0.3	V
IRSIN		IRSIN	0	2	A
SWD to GND		VSWD	-2.0	VS	V
ISWD		ISWD	0	-2	A
ENPS to GND		VENPS	-0.3	40	V
SMON to GND		VSMON	-0.3	40	V
RLEV to GND		VRLEV	-0.3	VSM	V
RSEL to GND		VSEL	-0.3	VSM	V
RFEX to GND		VRFEX	-0.3	VSM	V
SDLY to GND		VTOEN	-0.3	VSM	V
VFB to GND		VFB	-0.3	VSM	V
CDLY to GND		VCDLY	-0.3	VSM	V
PWGD to GND		VPWGD	-0.3	8	V
IPWGD		IPWGD	0	4	mA
WEN to GND		VWEN	-0.3	VSM	V
WDI to GND		VWDI	-0.3	VSM	V
ERR to GND		VERR	-0.3	8	V
IERR		IERR	0	4	mA
Maximum input current in protection circuitry on any pin		IPROT	-10	10	mA
ESD Protection	HBM; R=1.5K, C=100pF	VESD	-1.5	1.5	kV

Parameter	Condition	Symbol	Min.	Max.	Unit
Capacitor between VS and CDRV	ceramic (X7R) or better	CDR	150	-	nF
Continuous power dissipation Derate 7.5mW/°C above +20°C	@ TA = +20°C	PVTOT	-	1000	mW
Continuous power dissipation [1] Derate 25mW/°C above +105°C	@ TA = +105°C	PVTOT	-	800	mW
Thermal resistance junction to ambient		RTJA	-	160	K/W
Thermal resistance junction to ambient	[1] PCB heat sink area 500mm²	RTJACLD	-	40	K/W
Thermal resistance junction to case		RTJC	-	5	K/W
Operating temperature		TA	-40	125	°C
Junction temperature		TJ	-40	140	°C
Storage temperature		TSTG	-40	150	°C

1) Package mounted on FR4 50x50x1.5mm³; 70µ Cu, zero airflow

This integrated circuit can be damaged by ESD. ELMOS Semiconductor AG recommends that all integrated circuits must be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtile performance degradation to complete device failure.

4.2 Recommended Operating Conditions

Parameters are guaranteed within the range of operating conditions unless otherwise specified.

-40°C < TJ < 125°C

Parameter	Condition	Symbol	Min.	Max.	Unit
Supply voltage	100nF bypass, ceramic (X7R)	VS	5	40	V
Supply bypass capacitance	ceramic (X7R) or better	CIN	100	-	nF
Source impedance at VFB	RFB1//RFB2	RVFB	-	2	kOhm
External reference voltage at RFEX	Zi < 2kOhm	VRFEX	0	1.30	V
Linear regulator bypass capacitance	ceramic (X7R) or better	CSM	1	10	µF
Driver regulator bypass capacitance	ceramic (X7R) or better	CDR	330	1000	nF
ERR output current	VERRL < 0.50V	IERR	0.2	2	mA
PWGD output current	VPWGD < 0.50V	IPWGD	0.2	2	mA
POR and WD timing capacitance	ceramic (NPO / X7R)	CDLY	0	1	µF
DSW max. reverse recovery time	IF/ IR = 2A	TRR	-	30	ns
Operating temperature Range	PVTOT within limits	TOP	- 40	105	°C

All voltages are referred to GND, and currents are positive when flowing into the node unless otherwise specified.

5 Detailed Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical values represent the mean values at room temperature, which are related to production processes.

5.1 Supply Voltage and Currents

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Input voltage range		VS	5	-	40	V
2	Shutdown mode current into VS	ENPS=false SMON=false VS=>6V	ISHTD	-	12	18	µA
3	ENPS input high threshold	5V<VS<40V	VENPSH	-	2.2	-	V
4	ENPS linput low threshold	5V<VS<40V	VENPSL	-	0.8	-	V
5	ENPS input pull down current	5V<VS<40V, ENPS=5V	IENPS	-	2	-	µA

5.2 Low Drop Internal Voltage Regulator

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Output voltage	6V<VS<40V, IVSM<5mA	VSM	4.50	5	5.50	V
2	Dropout voltage	IVSM<5mA, VS=5V	DVSM	-	0.5	-	V
3	External available output current	PVTOT must be within limits	IVSM	10	-	15	mA
4	Output short current	6V<VS<40V, static value	IVSMST	20	-	120	mA
5	Idle quiescent supply current into VS (stand-by)	ENPS=true, SMON=false, VS=>6V, IVSM=0µA	IVSOFF	140	170	200	µA
6	SMON input high threshold	6V<VS<40V	VHSMON	-	2.2	-	V
7	SMON input low threshold	6V<VS<40V	VLSMON	-	0.8	-	V
8	SMON input pull down current	6V<VS<40V, SMON=5V	ISMON	-	2	-	µA
9	Device quiescent current	[3] not switching	IDQS	-	3	-	mA

[1] VS => 5V, VSM > 4V, ENPS = true, SMON = true, [2] Tj=25°C , [3] VS = 12V, ENPS = true, SMON = true; CDR = 220nF, VFB = VSM

5.3 Internal VSM Undervoltage Lockout Level

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	VSM level true	[1] SMON=true	VCLRL	-	3.90	-	V
2	VSM level false	[1] SMON=true	VCLRH	-	3.60	-	V

[1] Ensured by design. Not production tested.

5.4 MUX

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	RFEX input voltage range	1)	VRFEX	0	-	1.30	V
2	RFEX input current	1) 0V < VRFEX < 1.3V	IRFEX	-	-1	-3	µA
3	RFEX feedthrough loss	1) 2) Source Impedance < 2kOhm	VLRFEX	-	10	-	mV
4	RSEL level true	1) 2)	VRSELH	-	0.65xVSM	-	V
5	RSEL level false	1) 2)	VRSELL	-	0.26xVSM	-	V
6	RSEL input current	1)	IRSEL	-	1	-	µA
7	RLEV level true	1) 2)	VRLEVH	-	0.65xVSM	-	V
8	RLEV level false	1) 2)	VRLEVL	-	0.26xVSM	-	V
9	RLEV input current	1)	IRLEV	-	1	-	µA

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) Ensured by design. Not production tested.

5.5 Voltage Comparator

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Effective VFB offset voltage	1) 2)	VOFF	-10	0	10	mV
2	VFB input current	1)	IVFB	-	-1	-3	µA
3	VFB reference voltage H	1)	VR1	1.165	1.200	1.236	V
4	VFB reference voltage L	1)	VR2	194	200	206	mV
5	Static VFB hysteresis	1)	VCMPHYST		4		mV
6	VFB propagation time to SW output	2) VS=12V, VR1+/-100mV Tj=25°C, RSW=50Ohm	TRHFB	-	100	-	ns

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) Ensured by design. Not production tested.

5.6 Current Comparator

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Threshold level	1)	VCLIM	VS-170m	VS-200m	VS-230m	V
2	Propagation time to SWD output	2) VS=12V, Tj=25°C, RS=1.30Ohm, RSW=50Ohm	TRHCL	-	100	-	ns

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) Ensured by design. Not production tested.

5.7 Pulse Frequency Modulator

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Minimum SW off-time	1) SDLY = false	TOFFM	1.5	2	2.5	µs
2	Minimum SW off-time	1) SDLY = true and CCMP activeted	TOFFMS	14	20	26	µs
3	Minimum SW on-time	1)	TONM	0.5	1	1.5	µs
4	Blanking time	1) 2)	TBLK	-	300	-	ns
5	Duty cycle	1) 2)	DCYC	0	-	100	%

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) Ensured by design. Not production tested.

5.8 Power Stage

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	ON resistance	1) VS-CDRV = 5V	RDSON	-	0.50	0.80	Ohm
2	RSIN voltage range	1)	VRSR	VS-1000m	VS-200m	VS	V
3	SWD voltage range	1)	VSWR	-2.0	-	VS	V
4	Minimum sink current by internal regulator	1) 2) CDR = 220nF	IDRVS	5	8	-	mA
5	Driver lockout voltage	1) 2) CDR = 220nF	VDRVL	-	3.74	-	V
6	Driver voltage	1) 2) between VS and CDRV, CDR = 220nF	VDRV	4.5	5.20	6.5	V

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) static value

5.9 Error Output and Optional Short Detection Delay Input

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	SDLY level true	1) 2)	VSDLH	-	0.65xVSM	-	V
2	SDLY level false	1) 2)	VSDLL	-	0.26xVSM	-	V
3	ERR open drain voltage range	1) 2) ERR = false	VERRH	0	-	6	V
4	ERR low voltage	1) IERR<= 1mA	VERRL	-	0.50	0.80	V
5	ERR leakage current	1) VERR = 5V	IERRL	-	-	10	µA

1) VS => 5V, VSM > 4V, ENPS = true, SMON = true, 2) Ensured by design. Not production tested.

5.10 Power Good / Reset and Watchdog Stage

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	PWGD threshold	1)	VPWGDT	-	0.90xVFB	-	V
2	PWGD hysteresis	1)	VPWGDY	-	0.05xVFB	-	V
3	PWGD low voltage	PWGD = false IPWGD <= 2mA	VPWGDL	-	0.50	0.80	V
4	PWGD open drain voltage range	2) PWGD = true	VPWGDR	0	-	6	V
5	PWGD leakage current	VPWGD = 5V	IPWGDL	-	-	10	µA

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
6	Minimum required pulse duration at VFB for PWGD response	[1) 2)] VFB=1.200V overdrive=-250mV int. VREF=1.2V CDLY = 100nF	TREC	2	-	-	µs
7	PWGD delay without CDLY	[1) 2)] VFB=1.050V overdrive=+/-200mV int. VREF=1.2V CDLY = 0nF	TPWGD	-	40	-	µs
8	Upper reset timing threshold	[1) 2)] CDLY = 100nF	VRUD	0.75xVSM	0.8xVSM	0.85xVSM	V
9	Reset saturation voltage	[1) 2)] CDLY = 100nF	VRLD	0	-	0.5	V
10	Reset discharge resistance	[1) 2)]	RRDC	-	15	-	Ohm
11	Reset charge current	[1)] VSM = 5V VCDLY=2.5V	IRSTC	9	15	21	µA
12	Reset delay with CDLY	[1) 2)] VSM = 5V CDLY = 100nF 1%	TRST	15	25	35	ms
13	WEN level true	[1) 2)]	VWENH	-	0.65xVSM	-	V
14	WEN level false	[1) 2)]	VWENL	-	0.26xVSM	-	V
15	WDI level true	[1) 2)]	VWDIH	-	0.65xVSM	-	V
16	WDI level false	[1) 2)]	VWDIL	-	0.26xVSM	-	V
17	Watchdog trigger pulse duration	[1) 2)] Reaction on trailing edge only	TWDI	200	-	-	ns
18	Upper watchdog switching threshold	[1) 2)] CDLY = 100nF	VWUD	0.75xVSM	0.8xVSM	0.85xVSM	V
19	Lower watchdog switching threshold	[1) 2)] CDLY = 100nF	VWLD	0.15xVSM	0.2xVSM	0.25xVSM	V
20	Watchdog charge current	[1)] VSM = 5V VCDLY=2.5V	IWDC	9	15	21	µA
21	Watchdog discharge current	[1)] VSM = 5V VCDLY=2.5V	IWDD	1.68	2.80	3.90	µA
22	Watchdog period	[1) 2)] VSM = 5V CDLY = 100nF 1%	TWDP	75	125	175	ms
23	Watchdog trigger time	[1) 2)] VSM = 5V CDLY = 100nF 1%	TWDTR	63	105	147	ms

[1)] VS => 5V, VSM > 4V, ENPS = true, SMON = true, [2)] Ensured by design. Not production tested.

5.11 Thermal Shutdown

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Shutdown temperature	[1)] VS > 5V	KTMPS	-	160	-	°C
2	Hysteresis	[1)] VS > 5V	KTMPH	-	30	-	°C

[1)] Ensured by design. Not production tested.

6 Typical Performance Characteristics

Shutdown current vs. input volt. and temperature

Reference voltages over temperature

Idle current vs. input voltage and temperature

Current sense trip level vs. temperature

VSM Voltage over input voltage and temperature

Swtich ON-resistance vs. temperature

Minimum switch on-time vs. temperature

PWGD delay vs. capacitance and temperature

Minimum switch off-time vs. temperature

WD period vs. capacitance and temperature

Short case (SDLY=1) min. swtich off time vs. temp.

7 Functional Description

7.1 Operation

7.1.1 Typical Application Circuit

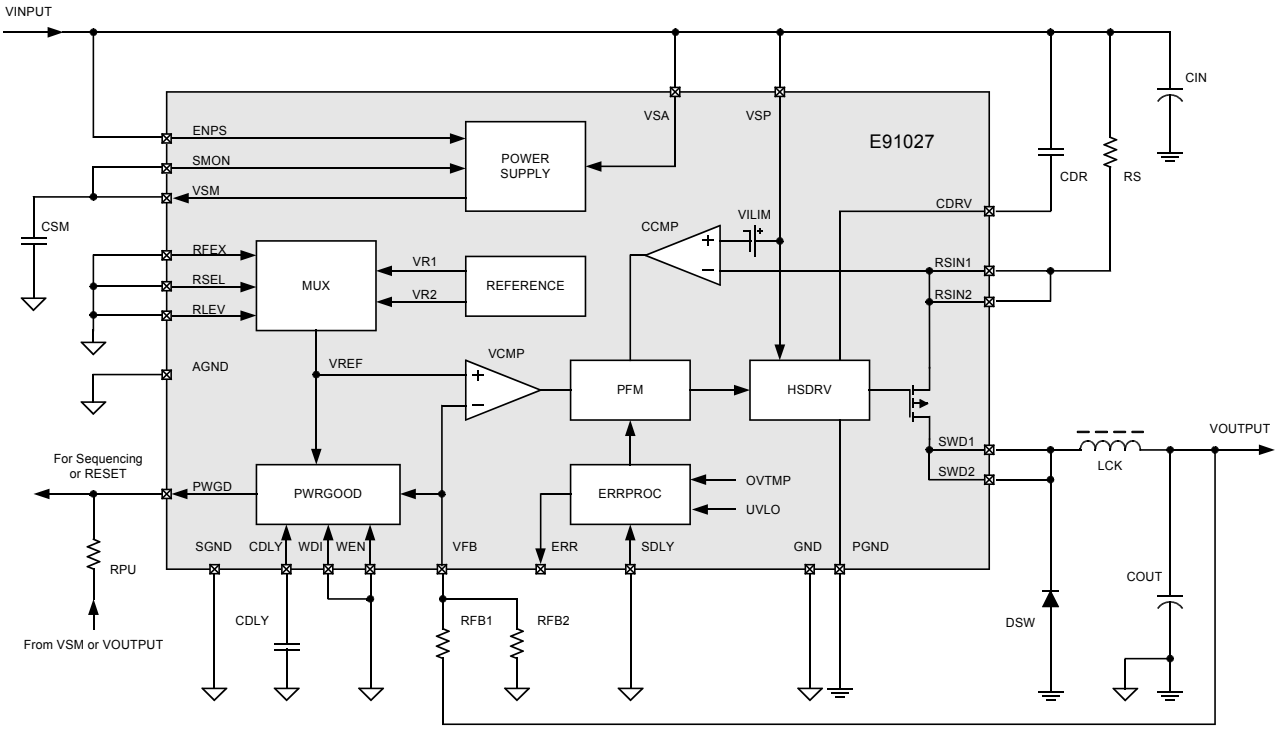


Figure 7.1.1-1: Typical Application Circuit

7.1.2 Introduction

The E910.27 is a user friendly high voltage CMOS step-down DC-DC converter that provides an external controllable output voltage. It features an internal 500mOhm (typically) P-channel MOS transistor switch for high efficiency over a wide range of input/output voltages and currents. Moreover the converter can be operated over a very wide input supply range from 5V to 40V with typically 12µA shutdown and typically 170µA stand by current, making them optimal for use in applications as automotive and industrial control.

Its sophisticated control scheme combines the advantages of pulse-skipping pulse-frequency modulation (low supply current) and pulse-width modulation (high efficiency with heavy loads), providing high efficiency over a wide input voltage and output current range. Operation up to 100% duty cycle allows the lowest possible dropout voltage, which allows a wider input voltage variation. Its small size, high switching frequency, and low external parts count minimise the required circuit board area and component cost.

A reset signal is generated for a voltage at VFB below a level of VREF-15%. The watchdog circuit monitors a connected controller. If there is no positive going edge at the watchdog input WDI within a fixed time, the PWGD output is set low. The delay for power on reset and the maximum permitted watchdog pulse period can be set externally with capacitor CDLY.

Figure 7.1.1-1 shows the E910.27 in a typical application circuit.

7.2 Linear Regulators

7.2.1 Internal Power Supply

The internal high PSRR power supply allows the E910.27 to operate from typically 4.5V up to 40V input voltage (VSA), while drawing a constant very low quiescent current (ISHTD). This allows the use in automotive K30 systems. It is always on and supports the internal regulators, thermal protection circuits, undervoltage lockout circuits and error logic's with stable reference voltages and currents.

7.2.2 VSM Regulator

The power supply block contains also a short and thermal protected low quiescent current 5V low drop linear regulator (VSM). It will be switched on via a high level at Pin ENPS. Output VSM can provide at minimum 10mA to an external load (e.g. stand by circuits).

Due to the very wide input level range from 0V to $VS_{MAX,}$ and CMOS compatible thresholds the ENPS input can be driven by controllers, bus transceivers (e.g. CAN), K15D applications and used for power sequencing.

In SMPS operating mode (SMON=true) the linear regulator powers the internal SMPS circuits. When the input voltage VSA goes below about 4V and therefore VSM drops down to the level VCLRH the E910.27 enters into undervoltage lockout state, the internal P-channel MOS transistor is switched off and the ERR output goes low. Bypass VSM with a good quality capacitor (CSM) to the small signal ground.

7.3 Device Quiscent Currents

Mode	ENPS	SMON	Device Quiescent current
Shutdown (Idle)	0	0	ISHTD
VSM ON (linear regulator on, not externally loaded)	1	0	IVSMST
SMPS ON (not switching)	1	1	IDQS

7.4 DRV Regulator

The E910.27 contains a high side hysteretic regulator (CDRV) that controls its output to a voltage of VDRV below the positive high side driver input voltage VSP. This regulator limits the internal P-channel MOS transistor gate swing, provides high gate charge / discharge currents, high switching frequency and allowing high input voltage operation without exceeding the internal P-channel MOS transistor gate source breakdown voltage. If VDRV drops due any case to its lookout voltage VDRVL the ERR output will be set and internal P-channel MOS transistor is switched off. Bypass CDRV always with a good quality temperature stable ceramic capacitor between VSP and CDRV, otherwise the chip may be damaged. To avoid substrate currents in case of very high temperatures and a fast falling edge of the input voltage a Schottky diode between CDRV and PGND may be necessary.

7.5 Error Output

Pin ERR indicates fault conditions of the E910.27. These conditions are:

- Under voltage lockout (VSM < VCRH)
- Driver voltage low (VDRV < VDRVL)
- Chip over temperature (Tj > KTMPS)

- SMON input pin low

One or more errors switch the ERR output into high impedance. If the ERR pin is not used, it should be connected to ground. The open drain output can be wired with other signals.

7.6 Reference Multiplexer

A high flexibel feature of the E910.27 is its internal reference multiplexer. Due to the externally selectable MUX the user can choose between two internal precise temperature compensated or an user provided external reference. Via an external reference voltage at pin RFEX the output voltage or output current of the SMPS circuit can be controlled (e.g. for LED dimming applications or synchronous output voltage ramp up).

Keep in mind that in case of disabling VSM (ENPS=false) the ESD input structures of pins RFEX, RSEL, and RLEV will clamp to ground. Input signals in this mode leads to malfunction of the E910.27 and are therefore not allowed. In any case floating of the three pins must be avoided. A save way to supply the logic levels for the multiplexer is for logically „false“ connect to ground and for logically „true“ connect to VSM. Use hard wired coding on the pc-board, because changing the mode during operating is not allowed.

VCMP connected to	RFEX	RLEV	RSEL
VR1 (internal)	-	0	0
VR2 (internal)	-	1	0
VREXT (external)	Ex. Ref Input	0	1

7.7 Power Good, Reset Generation and Watchdog Circuitry

7.7.1 PWRGOOD Block

Depending on external wiring the PWRGOOD circuit can provide *POWER-GOOD*, *RESET* or *WATCHDOG* behaviour. The PWGD pin open drain output can be wired „OR“ to other E910.27. If the PWGD pin is not used it should be connected to GND.

If the external reference input (RFEX) is selected via the MUX (RSEL=true), the whole PWRGOOD block is automaticly disabled and the PWGD output stays low. For correct behaviour of the PWGD pin, there must be a minimum input voltage at VSA of 4V.

7.7.2 Power Good and Reset Timing

If the switcher feedback voltage VFB decreases 15% out of nominal regulation value, the external capacitor CDLY at pin CDLY will be discharged fast by the reset generator and pin PWGD is set low. If feedback voltage VFB rises above the reset threshold, VREF-10%, CDLY will be charged with a constant current IWDC. After the power on reset time TRST the voltage on capacitor CDLY reaches VRUD and the PWGD output will be set high (high impedance) again. The value of the power on reset time TRST can be set within a wide range depending on the capacitance value of CDLY.

The delay time of power on reset is defined by the charging time of the external capacitor CDLY and can be calculated as follows:

$$TRST = \frac{(VRUD - VRLD)}{IWDC} \cdot CDLY$$

[1]

For power good behaviour of the circuit only, e.g. in case of ramp up sequencing of multiple power supplies, the delay capacitor CDLY is omitted. PWGD output than will react instantaneously (within TPWGD).

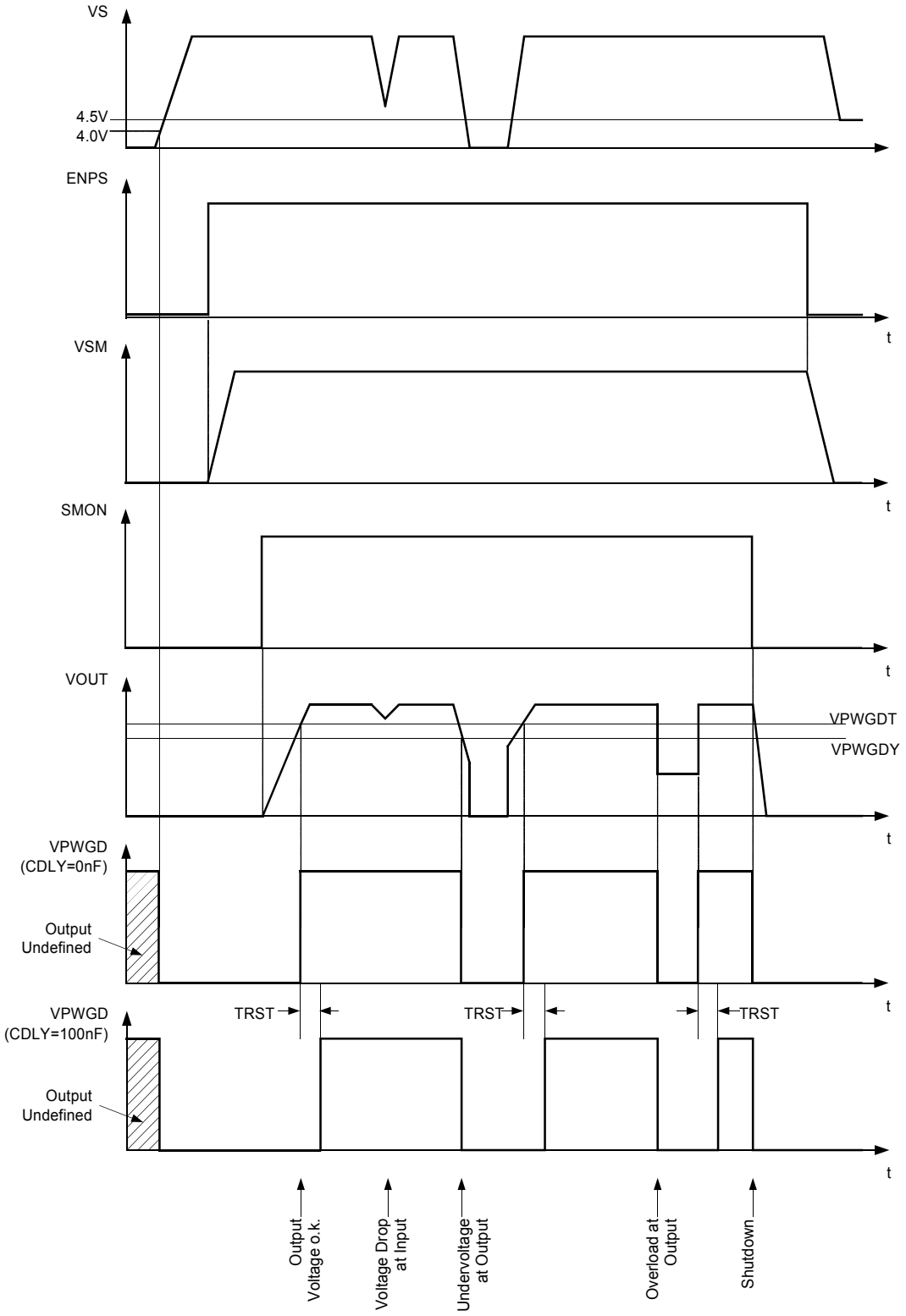


Figure 7.7.2-1: Time Response Power Good and Reset Generation

7.7.3 Watchdog Timing

When the voltage on the delay capacitor CDLY has reached VWUD and pin WEN was set high, the watchdog circuit is enabled and discharges CDLY with a constant current IWDD. If there is no rising edge detected at the watchdog input, CDLY will be discharge down to VWLD, then PWGD output will be set low and CDLY will be charged again with the current IWDC until VCDLY reaches VWUD and pin PWGD will be set high (high impedance) again.

If a watchdog pulse, rising edge at watchdog input WDI, occurs during the discharge period, CDLY is charged again and the PWGD output stays high. After VCDLY has reached VWUD, the periodical behaviour starts once more.

The watchdog timing is defined by the charging and discharging time of the external capacitor CDLY and can be calculated as follows:

$$TWDTR = \frac{(VWUD - VWLD)}{IWDD} \cdot CDLY$$

$$TWDP = \frac{(VWUD - VWLD) \cdot (IWDC + IWDD)}{IWDC \cdot IWDD} \cdot CDLY$$

$$TWDL = \frac{(VWUD - VWLD)}{IWDC} \cdot CDLY$$

[2]

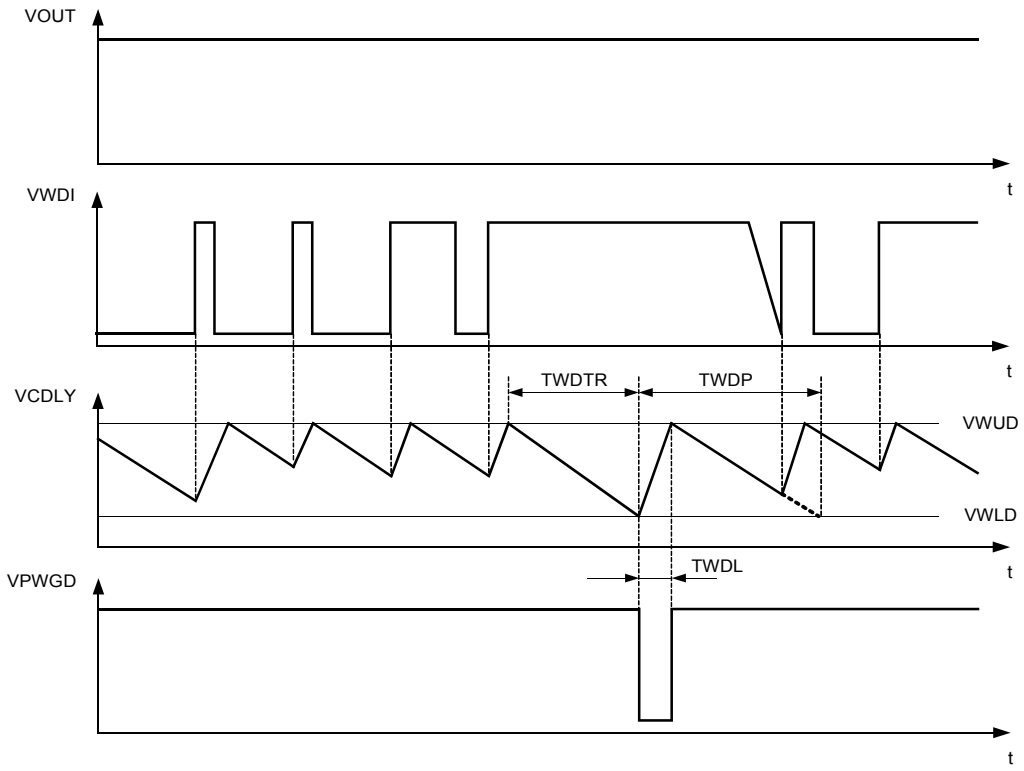


Figure 7.7.3-1: Watchdog Behaviour, Time Response

Use hard wired coding of WDE on the pc-board, because changing the mode during operating is not allowed.

7.8 Description of the SMPS Section

The E910.27 is a high input-voltage step down (buck) DC-DC converter including an internal robust P-channel MOS transistor with a typical resistance of 0.50 Ohm. This low on resistance and the possibility of 100% duty cycle assures high efficiency and a minimal dropout even at high output current level and a wide input voltage variation. By means of an on board shunt resistor current in fault conditions is limited. Together with the internal temperature supervisor the device is protected against accidental output short circuit, to avoids dangerous load damage. If the chip temperature rises higher than a fixed internal threshold (150°C with 40° C hysteresis), the power stage is turned off.

The E910.27 automatically switches from PWM operation at medium and heavy loads to pulse skipping operation at light loads to improve light-load efficiency without an increase in output ripple. The small size, high switching frequency, integrated P-channel MOS transistor, and the low parts count minimise the required circuit board area and component costs. The hysteretic control architecture provides for simple design without any control loop stability concerns using a wide variety of external components.

The SMPS part will be switched on by a high level at Pin SMON. Due to the very wide input voltage range from 0V to $VS_{MAX,}$ and its CMOS compatible thresholds the SMON input can be driven by micro-controllers, bus transceivers (e.g. CAN), K15D applications and can be used for power up sequencing .

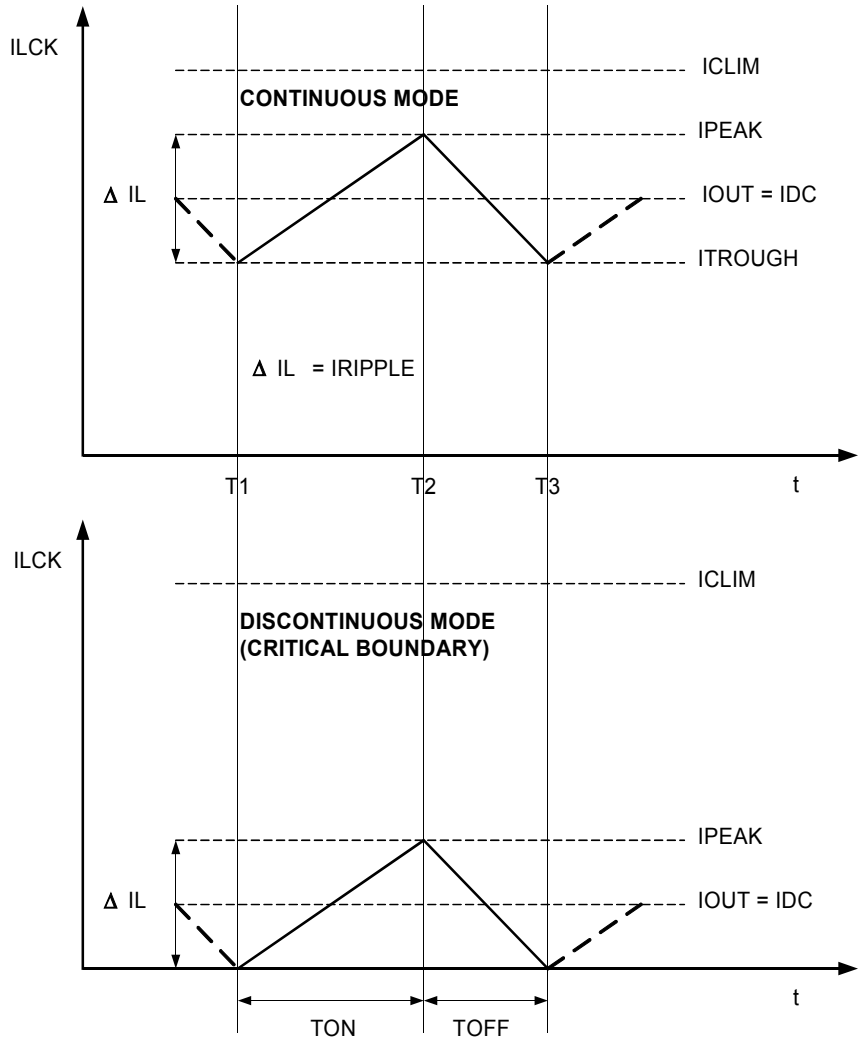


Figure 7.8-1: Choke Current Waveform

7.8.1 Operating Modes

Hysteretic control does not require an internal oscillator. Switching frequency depends on external components and operating modes. Operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

When delivering low output currents, the E910.27 operates in discontinuous conduction mode (DCM).

In case of delivering medium to high output currents, the E910.27 operates in PWM continuous conducted mode (CCM). In this mode, current always flows through the choke and never ramps to zero. The pulse frequency modulator (PFM) adjusts the internal P-channel MOS transistor duty cycle to maintain regulation without exceeding the peak switching current set by the external current sense resistor (RS).

7.8.2 100% Duty Cycle and Dropout

The E910.27 operates with a duty cycle up to 100%. This feature extends the input voltage range by turning the internal P-channel MOS transistor on continuously when the supply voltage (VS) approaches the output voltage. This services the load when conventional switching regulators with less than 100% duty cycle would fail. Dropout voltage is defined as the difference between the input (VINPUT) and output (VOUTPUT) voltages when the input is low enough for the output to drop out of regulation. Dropout voltage depends on the internal P-channel MOS drain to source on resistance, current sense resistor (RS), and choke (LCK) series resistance and is proportional to the load current:

$$V_{DROP} = I_{OUT} \cdot \left(R_{RDSON} + R_{RS} + R_{LCK}\right)$$

[3]

7.8.3 Discontinuous Conduction Mode

The E910.27 operates in discontinuous conduction mode (DCM) at light load current. In discontinuous conduction mode, current through the choke (LCK) starts at zero and ramps up to the peak as high as the voltage comparator (VCMP) limit , then ramps down to zero. Next cycle starts when the VFB voltage reaches the reference voltage. Until then, the choke current remains zero. Switching frequency is lower and switching losses reduce. The switching frequency depends on input voltage, output capacitor and output load. The switch waveform (Pin SWD) can exhibit ringing, which occurs at resonant frequency of the choke and stray capacitance, due to residual energy stored in the core when the commutation diode (DSW) turns off.

7.8.4 Continuous Mode PFM Control Behaviour

The E910.27 PFM controller has an unique regulation scheme that allows PWM operation at medium and high output current with automatic switching to pulse skipping mode at lower currents to improve light load efficiency.

Under medium and heavy load operation, the choke (LCK) current is continuos and the SMPS part operates in PWM mode. Current always flows through the choke and never ramps down to zero. In this condition, the switching frequency is set by either the minimum on-time (TONM), or the minimum off-time (TOFFM), depending on the duty cycle. The duty cycle is:

$$Duty \approx \frac{V_{OUTPUT} + Vd_{DSW} + IOUT_{MAX} \cdot RDC_{CHOKE}}{V_{INPUT} + Vd_{DSW} - IOUT_{MAX} \cdot \left(RS + RDS_{ON} + RDC_{CHOKE}\right)}$$

[4]

If the duty cycle is less than 33%, the minimum on-time (TONM) controls the switching frequency. The operating frequency is approximately:

$$Fop \approx \frac{Duty}{TONM} \cong 1000kHz \cdot Duty$$

[5]

If the duty cycle is greater than 33%, the off-time (TOFFM) sets the switching frequency. The operating frequency is approximately:

$$Fop \approx \frac{(1 - Duty)}{TOFFM} \cong 500kHz \cdot (1 - Duty)$$

[6]

In both cases the voltage is regulated by the voltage comparator (VCMP). For low duty cycles (<33%) the internal P-channel MOS transistor is turned on for the minimum on-time (TONM), causing fixed on-time operation. During the internal P-channel MOS transistor's on-time the output voltage rises. Once the internal P-channel MOS transistor is turned off, the voltage drops to the regulation threshold set by the external voltage divider (RFB1 and RFB2), and another cycle is initiated. For high duty cycles (>33%) the internal P-channel MOS transistor remains off for the minimum off-time (TOFFM) causing fixed off-time operation. In this case the internal P-channel MOS transistor remains on, until the output voltage rises to the regulation threshold set by the external voltage divider (RFB1 and RFB2). Then the internal P-channel MOS transistor turns off for the minimum off-time (TOFFM) and the next cycle starts.

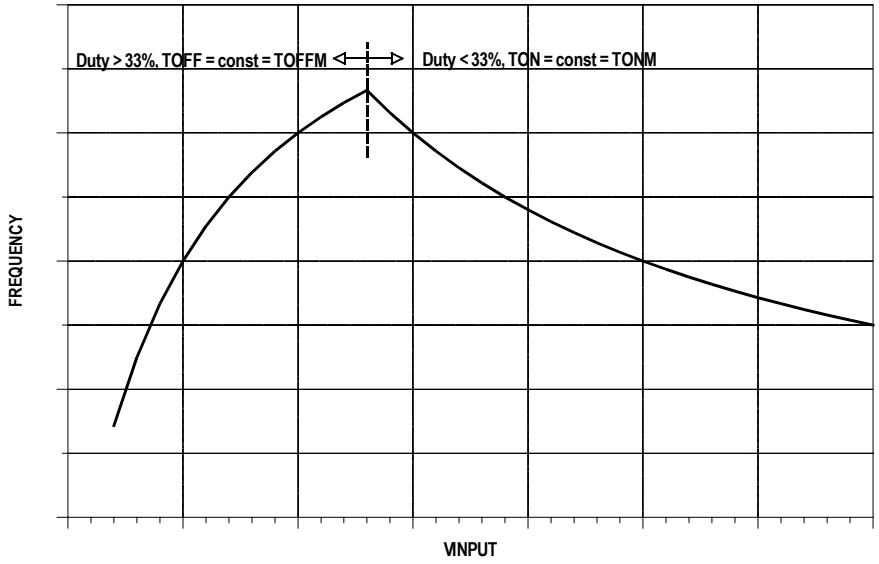


Figure 7.8.4-1: Relative Switching Frequency in Continuous Conduction Mode

An unique regulation feature of the PFM controller is its automaticly selection of fixed on-time or fixed off-ime mode. By switching between fixed on-time and fixed off-time operation the E910.27 can operate at high input to output ratios, yet still operate up to 100% duty cycle for low dropout. When transitioning from fixed on-time to fixed off-time mode, the output voltage drops slightly due to the output ripple voltage. In fixed on-time operation the minimum output voltage is regulated, while in fixed off-time operation the maximum output voltage is regulated. Thus, as the input voltage drops below approximately three times of the output voltage, a decrease in line regulation can be expected. The output voltage drop is about:

$$V_{DROP\_OP} \approx \frac{V_{RIPPLE}}{2}$$

[7]

At light output loads, the choke current is discontinuous, takes the E910.27 to switch at lower frequencies and decreasing the internal P-channel MOS transistor's gate drive and switching losses. Under most circumstances in discontinuous mode the on-time will be fixed to the minimum on-time of TONM. If the choke (LCK) inductance value is small or the current sense resistor (RS) is large the current limit will be reached before the minimum on-time (TONM), terminating the on-time and overwrite it.

If the impedance of the feedback divider is too high, or the choke (LCK) inductance is too large, or the output capacitance (COUT) is too high and equivalent series resistance (ESR) is too low, then the internal P-channel MOS transistor remains on longer than the minimum on-time (TONM) until the output capacitor charges beyond the voltage comparators (VCMP) hysteresis of about VHYST and causing the controller to operate in hysteretic mode. Operating in hysteretic mode results in lower switching frequency operation.

$$VHYST \approx 4mV \cdot \left(1 + \frac{RFB1}{RFB2}\right)$$

[8]

The E910.27 requires a certain ESR value for proper operation. The transition to hysteretic mode occurs at the critical output capacitor ESR:

$$C\_ESR_{CRITICAL} \approx \frac{VHYST}{I_{RIPPLE}}$$

[9]

In the above equation IRIPPLE is the choke ripple current and can be approached, for duty cycle less than 33%, by:

$$I_{RIPPLE} \approx \frac{\left(V_{INPUT} - V_{OUTPUT} - IOUT_{MAX} \cdot (RS + RDS_{ON})\right)}{LCK} \cdot TONM$$

[10]

Where TONM is the minimum on-time for minimum on-time control, or in case of duty cycle greater than 33%:

$$I_{RIPPLE} \approx \frac{(V_{OUTPUT} + Vd_{DSW})}{LCK} \cdot TOFFM$$

[11]

Where TOFFM is the minimum off-time for minimum off-time mode.

7.8.5 Leading Edge Blanking

A leading edge blanking timer (TBLK) avoids an erratic operation through spikes at RSIN input while switching on the internal P-channel MOS transistor. The same timer suppresses also a quasi-analogue operation of the internal P-channel MOS transistor by means of too small gate drive pulses. Too small gate pulses lead to internal overheating and the complete SMPS is switched off.

7.8.6 Run Away at Start-up and Output Short

Under start-up or output short condition, the PFM will switch the internal P-channel MOS transistor always on to bring the output voltage in tolerance. When the voltage across RS caused by the high switch current reaches the threshold level (VCLIM) of the comparator CCMP, it resets the PFM and therefore the internal P-channel MOS transistor is immediately switched off. After the fixed off-time (TOFFM) the internal P-channel MOS transistor starts to conduct again. The required duty cycle in this short circuit situation is:

$$Duty_{Short} \approx \frac{Vd_{DSW} + V_{RLCK}}{V_{INPUT} - Von_{PMOS} - V_{RS} + Vd_{DSW}}$$

[12]

Depending on input voltage VS (especially at high input voltages), inductance values for the choke, internal P-channel MOS transistor´s on resistance and impedance of the rest of external components it is not always possible to keep the duty to the required small value. When this happens the current through the circuit is rising from period to period, until the output voltage reaches a value for the duty cycle that the E910.27 can handle, or reaches a maximum current, limited by the cumulated resistances in the buck path only. In this inrush current situation, the external components may be over stressed and / or the internal thermo protection switches off the whole SMPS. Normally this start-up time period is very short and the effect takes no matter.

To handle this current run away, the user can select with pin SDLY=true, a longer off-time option (TOFFMS), that takes place the minimum off-time (TOFFM) in case of triggering the current comparator CCMP only. Due to the reduced stored energy per switching cycle, ramp up duration of the whole supply takes somewhat longer. However, be careful there may be combinations of external component values (especially too low or too high inductance values for the choke), which prevents successful start-up of the supply.

8 Design Information

8.1 Design Guidelines

External component selection is driven by output to input voltage ratio (duty cycle), ripple current and maximum output load. The circuit design is an iterative process and must be carefully proved by testing of your prototype. First calculate the appropriate duty cycle range for your circuit, then proceed as follows.

8.1.1 Output Voltage Setting

The step down converter´s output voltage is set using the following equation, where RFB2 is connected between the VFB pin and SGND, and RFB1 is connected between VOUTPUT and the VFB pin.

$$RFB1 = \left(\frac{V_{OUTPUT}}{VREF} - 1 \right) \cdot RFB2$$

[13]

Where VREF is 200mV, 1.2V or externally by user provided in the range of 0V to 1.3V.

Output voltage ripple causes the output voltage to be higher or lower than set by the resistor divider at the feedback pin VFB. If the application runs with minimum on-time, the ripple (half of the peak to peak value) adds to the output voltage. In the case of working with minimum off-time, the output voltage is lower by the amount of ripple (half of the peak to peak value) at the output.

The input bias current at VFB loads the divider, therefore RFB2 should not be set too high-valued resistor to obtain high accuracy. A divider current of 120µA or higher is recommend. The feedback voltage line can be sensitive to noise. Avoid inductive coupling to the choke or the switching node, by keeping the VFB trace away from these areas.

In some applications, depending on board layout, the capacitance may be too high from pin VFB to GND. In this case, the internal comparator may not switch fast enough to operate with the minimum on-time or the minimum off-time given in this data sheet. For such applications a small feedforward capacitor (CFF) should be added in parallel with RFB1 to speed up the internal voltage comparator. On the other hand in some applications, depending on board layout, a small capacitor (some pF) in parallel to RFB2 might be necessary for stable operation. But this changes the operating frequency range too.

8.1.2 Current Sense Resistor Selection

In case of SMPS ramping up, heavy output load, or shorted output, the current sense comparator CCMP limits the peak switching current to VCLIM/RS, where RS is the value of the current sense resistor and VCLIM is the current sense threshold. Minimising the peak switching current will increase efficiency and reduce the size and cost of external components. But, since available output current is a function of the peak switching current the peak limit must not be set too low.

A good value is setting the peak current limit to 1.20 times the maximum load current by calculating the current sense resistor to:

.

$$RS \le \frac{VCLIM_{MIN}}{1.20 \cdot \left(IOUT_{MAX} + \frac{I_{RIPPLE}}{2} \right)}$$

[14]

This takes the normal coke's inductance value tolerance into account. The maximum RMS current in continuous operating mode is (take “r” from the calculations below):

$$IRS_{RMS} = IOUT_{MAX} \cdot \sqrt{D_{MAX} \cdot \left(1 + \frac{r^2}{12}\right)}$$

[15]

For 100% duty cycle we get:

$$IRS_{RMS} = IOUT_{MAX}$$

[16]

The current sense resistor's power rating should be:

$$P\_RS = \frac{VCLIM_{MAX}{}^2}{RS}$$

[17]

8.1.3 Choosing the Choke Value

The E910.27 operates with a wide range of inductance values. The inductance mainly determines the choke current ripple. Lower values are chosen to reduce physical size of the choke. Higher values allow more output current because they reduce peak current seen by the internal P-channel MOS transistor. Higher values also reduce output ripple voltage, and core loss.

When choosing a choke you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the choke, saturation, and of course, cost.

Since the choke value determines the output ripple current, you have to decide the ratio of the ripple current to the output current. The ripple current is depending on the duty cycle. Take the worst case ripple current value of your application.

$$r = \frac{\Delta I_L}{IOUT_{MAX}} = \frac{I_{RIPPLE}}{IOUT_{MAX}}$$

[18]

The core-material losses (magnetic hysteresis loss, eddy-current loss), skin-effect and proximity-effect losses in the conductor and radiation losses increases substantially with increasing “r”. Calculations show, the most optimum choice happens when this ratio “r” is set between 0.2 and 0.4 at the maximum output current. Often r=0.3 is used. Note that this is just a guideline for an economic design.

$$I_{RIPPLE} \approx 0.3 \cdot IOUT_{MAX}$$

[19]

If the converter should work in continous mode, even with the lowest output current, than the ripple ratio must yet be lower:

$$I_{RIPPLE} \leq 2 \cdot IOUT_{MIN}$$

[20]

The first step in choke design is to determine the appropriate operating mode of the E910.27. Calculate the minimum inductance value of the choke in continuous mode as follows.

Equation A:

$$LCK \geq \frac{\left(V_{OUTPUT} + Vd_{DSW} + IOUT_{MAX} \cdot RDC_{CHOKE}\right)}{I_{RIPPLE}} \cdot TOFFM$$

[21]

Equation B:

$$LCK \geq \frac{\left(V_{INPUT} - V_{OUTPUT} - IOUT_{MAX} \cdot (RS + RDS_{ON} + RDC_{CHOKE}\right)}{I_{RIPPLE}} \cdot TONM$$

[22]

With RDC_{CHOKE} = choke resistance and RDS_{ON} = P-channel MOS transistor “ON” resistance.

Case A, minimum input voltage

Determine the duty cycle for minimum input voltage VS. If the duty cycle is greater than 33% take equation A. If the duty cycle is lower than 33% take equation B.

Case B, maximum input voltage

Determine the duty cycle for maximum input votage VS. If the duty cycle is greater than 33% take equation A. If the duty cycle is lower than 33% take equation B.

Compare the calculation results from case A and case B and take the highest inductance value. Use the next greater standard inductance value. For optimum efficiency, the choke winding's resistance should be not larger than the current sense resistance (RS).

Calculate peak choke current at worst case to ensure that the choke will not saturate over temperature. Ferrite cores saturate abruptly. Peak current can be significantly higher than output current.

$$IChoke_{SAT} \geq 1.25 \cdot \frac{VCLIM_{MAX}}{RS_{MIN}}$$

[23]

Decide if your circuit can tolerate an magnetic open core geometry like a rod or barrel (drum), which have high magnetic field radiation, or whether it needs a closed core like an U-, E- or toroid to prevent EMI problems.

8.1.4 Choosing the Input and the Output Capacitor

Choose the input capacitor CIN and the output capacitor COUT to manage the input and output peak currents with acceptable voltage ripple. The value of the output capacitor depends on the output voltage ripple requirements as well as the maximum voltage deviation during load transients. ESR of the output capacitor and the value of the choke are the major source of output voltage ripple, so low ESR capacitors are recommended. Keep in mind that specifically standard aluminium electrolytic capacitors have a large ESR variation over temperature and lifetime. For good EMI behaviour, the ESL of the output capacitor should also be low. Output voltage ripple is the sum of contributions from ESL, ESR and capacitance value:

$$VOUT_{RIPPLE} = V_{RIPPLE}\,ESL + V_{RIPPLE}\,ESR + V_{RIPPLE}\,CVAL$$

[24]

The output voltage ripple in continuous mode due to the ESR is approximately:

$$V_{RIPPLE}\,ESR \approx R_{ESR} \cdot I_{RIPPLE}$$

[25]

The output capacitance typically increases with load transient requirements. During the time between the load transient and turn-on of the internal P-channel MOS transistor, the output capacitor must supply all the current required by the load. This current supplied by the output capacitor results in a voltage drop across the ESR that is substracted from the output voltage.

For a load step from near zero output current (discontinuous conduction mode) to its maximum (continuous conduction mode), the following equation can be used to calculate the required output capacitance.

$$COUT \geq \frac{LCK \cdot \left(IOUT_{MAX} + \frac{I_{RIPPLE}}{2} \right)^2}{2 \cdot V_{OUTPUT} \cdot V_{RIPPLE} CVAL} \cdot \left(\frac{V_{INPUT}}{V_{INPUT} - V_{OUTPUT}} \right)$$

[26]

If the worst case load step is not so extremely large and the E910.27 stays always in continuous conduction mode, a much smaller capacitance value for COUT is possible.

$$COUT \geq \frac{LCK \cdot {I_{\Delta L}}^2}{V_{OUTPUT} \cdot V_{RIPPLE} CVAL} \cdot \left(\frac{V_{INPUT}}{V_{INPUT} - V_{OUTPUT}} \right)$$

[27]

Where $I_{\Delta L}$ is the change in choke current, therefore minimum I_{RIPPLE}.

Obtain an output ripple voltage lower than the system hysteresis (VHYST) is not practical, since the E910.27 will switch at slower frequencies and increases choke ripple current.

The output capacitor COUT also needs therefore to be at least big enough to handle the worst case RMS current through it.

$$ICOUT_{RMS} = IOUT_{MAX} \cdot \frac{r}{\sqrt{12}}$$

[28]

Estimate the input capacitor capacitance value for a given maximum voltage ripple in continuous mode as follows:

$$CIN \geq \frac{LCK \cdot \left(IOUT_{MAX} + \frac{I_{RIPPLE}}{2} \right)^2}{2 \cdot V_{INPUT} \cdot V_{RIPPLE} CIN}$$

[29]

In a buck converter the input capacitor CIN must carry a high RMS current because of the currents pulsating nature. The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple at VINPUT. Use a low ESR capacitor type. For good EMI behaviour, the ESL of the input capacitor should be also very low. Two or more smaller value low ESR capacitors connected in parallel work often better than a single larger one. Place ceramic capacitors very close from VSA and VSP to GND. In continuous conduction mode, the input capacitor must be able to handle the whole RMS current of the converter with the worst case duty cycle of your application.

$$ICIN_{RMS} = IOUT_{MAX} \cdot \sqrt{Duty \cdot \left(1 - Duty + \frac{r^2}{12} \right)}$$

[30]

These equations are suitable for initial capacitor selection. Final values should be set by testing of your prototype circuit.

8.1.5 Catch Diode Selection

The catch diode DSW carries load current during the internal P-channel MOS transistors off-time. Therefore the average diode current is depending on the duty cycle. At high input to output voltage ratios the diode conducts most of the time. The most stressful condition for the diode is when the output is shorted. Under this condition the diode must safely handle a peak current of:

$$IDSW_{PEAK} \geq 2 \cdot \frac{VCLIM_{MAX}}{RS_{MIN}}$$

[31]

The catch diode maximum forward loss in continuous conduction mode is:

$$PDSW_{MAX} \approx IDSW_{AVG} \cdot Vd_{DSW}$$

[32]

Where Vd_{DSW} is the maximum forward drop from the diode data sheet and $IDSW_{AVG}$ is the average current at the minimum duty cycle:

$$IDSW_{AVG} = IOUT_{MAX} \cdot (1 - Duty)$$

[33]

The reverse (blocking) voltage VRRM of the catch diode must be at minimum $VINPUT_{MAX}$.

The E910.27 high switching frequency requires a high speed rectifier DSW. The catch diode is the biggest EMI source in the circuit. Take therefore care of diode selection. Surface mount low reverse leakage Schottky diodes are recommended for low output voltages. Ultra high speed soft recovery rectifiers with reverse recovery times < 30ns should be used for moderate or high output voltages, where the increased forward drop causes less efficiency degradation.

8.1.6 Snubber Network Design

For low output current, in discontinuous conduction mode, the internal P-channel MOS transistor turns off, and the energy stored in the inductance would cause oscillations with the parasitic capacitances without a snubber network. Typically there are little losses in parasitic resonant circuits so many cycles of ringing normally occur. This oscillation may be an EMI issue. If required an RC snubber will easily damp the ringing.

If the snubber resistance is equal to the characteristic impedance of the resonant circuit then the resonant circuit will be critically damped. Once the circuit has been build and is operating, the values of the snubber components may be evaluated experimentally.

Start with a small value of capacitor CSN and place it in the circuit directly across the catch diode DSW, and observe the voltage waveform with and without the capacitor in the circuit. Increase the value of the capacitor until the frequency of the ringing to be damped has been halved. This is a near optimum value for the capacitor CSN since it allows damping very near Q=1. Add a resistor in series with the snubber capacitor and choose its value for optimum, so that the ringing will be aperiodic damped.

$$RSN \approx 2 \cdot \pi \cdot fres \cdot LCK$$

[34]

Where fres = initially measured resonant frequency, and LCK = choke inductance.

The amount of power dissipation is independent of the value of the resistor RSN. If the time constant of the snubber network is short compared to the switching period of the converter but is long compared to the voltage rise time, than the loss can be estimated by:

$$P\_RSN \approx Fop \cdot CSN \cdot V_{INPUT}{}^{2}$$

[35]

With Fop = switching frequency of the converter and V_{INPUT} = maximum input voltage.

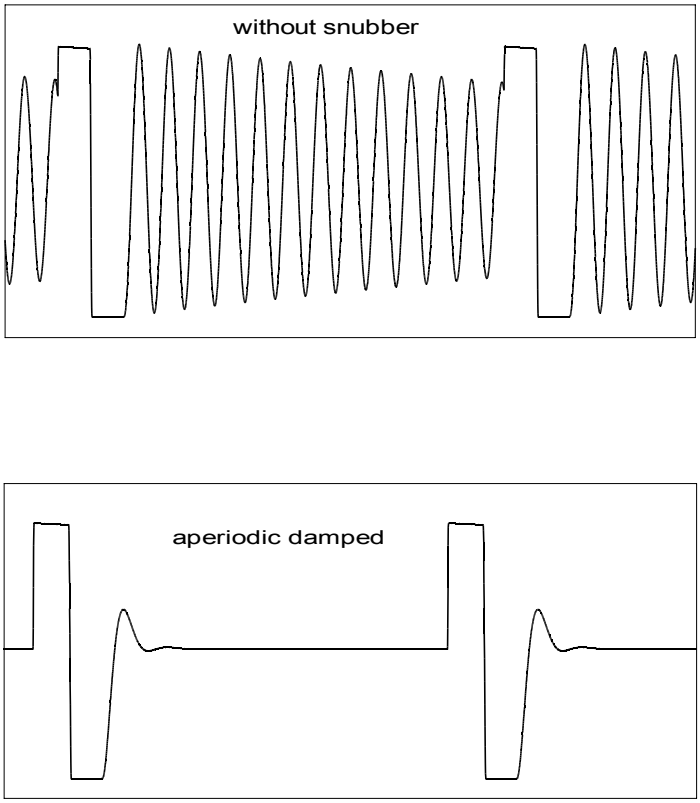


Figure 8.1.6-1: Discontinuous Mode Switch Drain Voltage without and with Snubber

8.1.7 Maximum available Output Current versus Internal Losses and Operating Temperature

The internal E910.27 DC-DC converter losses are a combination of quiescent device power, dynamic gate driver power and P-channel MOS transistors switching losses.

In any case the maximum allowed peak drain current of the internal P-channel MOS transistor must not exceed ISWD. With the maximum continuous output current of the buck converter and the specified maximum operating temperature, the chip temperature must be well lower than the thermal shutdown limit. The maximum available output current of the converter depends on maximum duty cycle, switching frequency (dynamic losses) and the thermal transfer of the package provided by the external heat sinking (e.g. printed circuit board).

The crossover losses are lowest at minimum input voltage. But they are usually a small fraction of the conduction losses, they can be sometimes ignored. For 100% duty cycle we get the worst case RMS current through the internal P-channel MOS transistor.The maximum RMS current through the switch in continuous conduction mode over duty cycle can be calculated by:

$$IPMOS_{RMS} = IOUT_{MAX} \cdot \sqrt{Duty\left(1+\frac{r^2}{12}\right)}$$

[36]

The effective ON-resistance of the E910.27 over junction temperature can be approximated by:

$$RDSON \approx (470m + 1.41m \cdot T_J + 2.85\mu \cdot T_J{}^2) \cdot \Omega$$

[37]

In continuous conduction mode the total device power loss can be approximated using the following equation:

$$PDEV_{TOT} \approx V_{INPUT} \cdot IDQS + IPMOS_{RMS}{}^2 \cdot RDSON + V_{INPUT} \cdot Fop \cdot \left(0.5 \cdot IOUT_{MAX} \cdot \left(t_{ON} + t_{OFF}\right) + Q_{DS}\right)$$

[38]

Where:

t_{ON} = P-channel MOS transistor turn on time

t_{OFF} = P-channel MOS transistor turn off time

Q_{DS} = P-channel MOS transistor gate driver charge

Typically values for the E910.27 are:

t_{ON} ~ 20ns

t_{OFF} ~ 30ns

Q_{DS} ~ 10nQ

When maximum junction temperature and maximum operating temperature are known, their difference indicates the permissible junction temperature rise for the given application. The thermal resistance path must ensure that the product PDEV x RTAJ is lower than this difference. The maximum possible device power loss can by calculated by:

$$PDEV_{MAX} \approx \frac{TJ_{MAX} - TA_{MAX}}{RTAJ}$$

[39]

Where:

TAMAX = maximum operating temperature

TJMAX = maximum save junction temperature, about 135°C

RTAJ = thermal resistance junction to ambient.

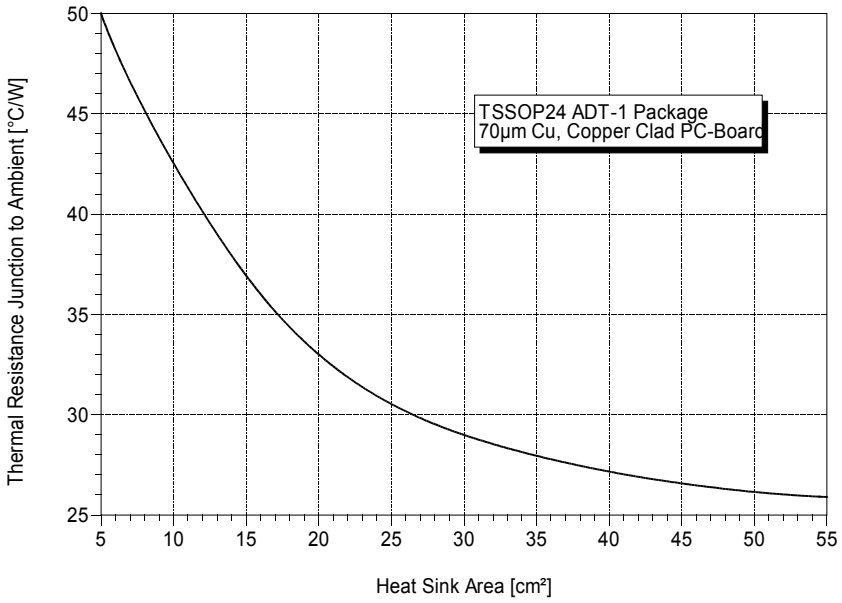


Figure 8.1.7-1: Typical Thermal Resistance (RTAJ) versus PC-Board Area

Always use a ground plane under the step-down converter to minimise interplane coupling and provide the required heat sinking. The typically thermal resistance for a given PC-board area can be read in the above diagram. By further reducing of the thermal resistance due to an additional external heat sinking (e.g. case) a maximum power loss of about 1.6W is possible.

9 PCB Layout Considerations

The PC board layout is very important in all high-frequency switching converter designs. Poor layout can cause switching noise into the feedback signal and may degrade performance and is general the source of heavy EMI problems.

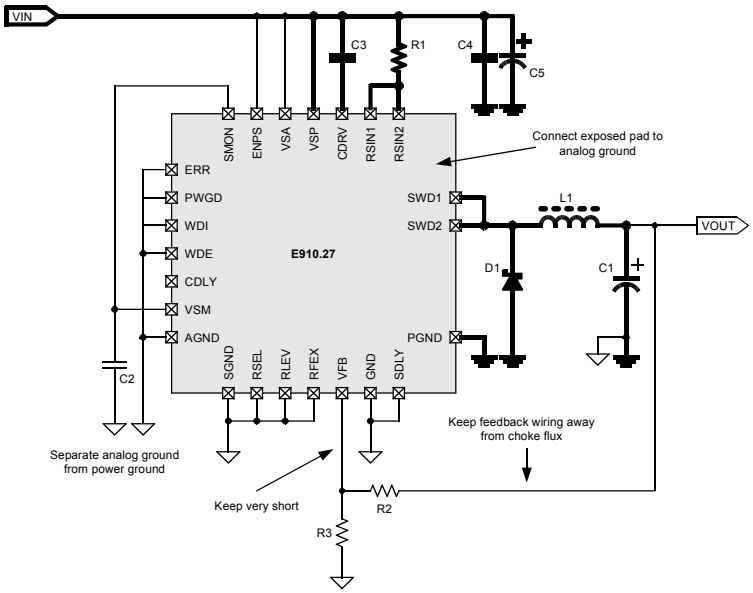


Figure 9-1: Typical Converter Schematic for PCB Layout

For minimal inductance, the wires indicated by heavy lines should be as wide and short as possible. Keep the ground pin of the input capacitor (C5) as close as possible to the anode of the catch diode (D1), snubber network (if there is any) and output capacitor (C1). This path carries a large AC current. The switching node, the node with the catch diode cathode, choke, and internal P-channel MOS transistor drain (SWD1 & SWD2), should be kept short. This node is one of the main sources for radiated EMI since it is an AC voltage with switching frequency. It is always a good practice to use a ground plane in the design of the PC board, particularly at high frequency currents.

The three ground pins, AGND, SGND and GND, should be connected by as short a trace as possible. The ground pins should be tied to the ground plane, or to a large ground trace in close proximity to both the VFB divider and then should be connected to PGND pin and the output capacitor (C1) grounds.

The VFB pin is a high impedance node and care should be taken to make the VFB trace short to avoid noise pickup, inaccurate regulation and erratic function of the PWGD output. The feedback resistors should be placed as close as possible to the E910.27, with the ground of R3 placed as close as possible to the SGND of the E910.27. Avoid inductive coupling to the choke or the switching node, by keeping the VFB trace away from these areas. Radiated noise can be decreased by choosing a shielded version for the choke.

Refer to the E910.27 demo board as an example layout.

10 Applications Information

10.1 Block X1

10.1.1 Block Diagram

Figure 10.1.1-1: Blockdiagram of Block X1

10.1.2 Functional Description

10.2 Application Gallery

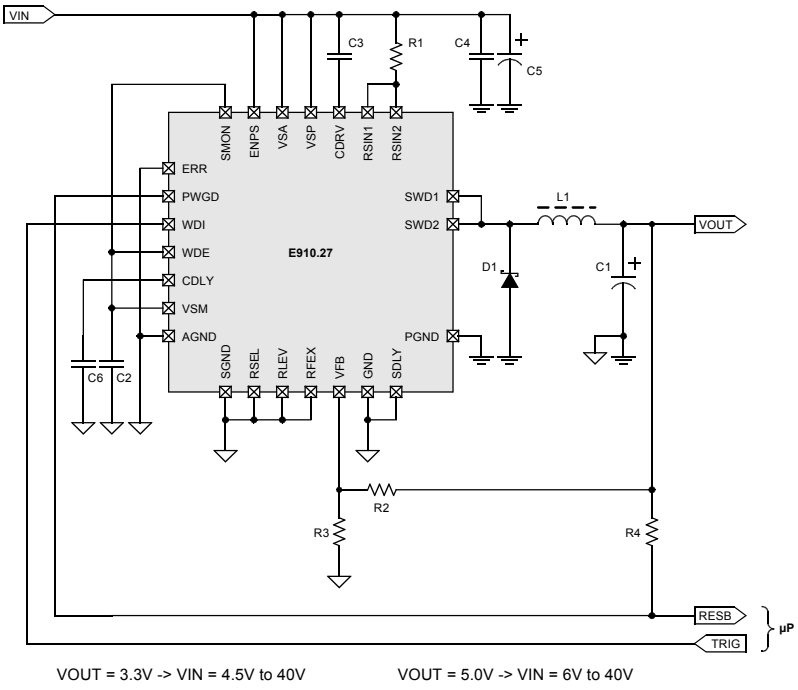


Figure 10.2-1: µP Power Supply with RESET and Watchdog

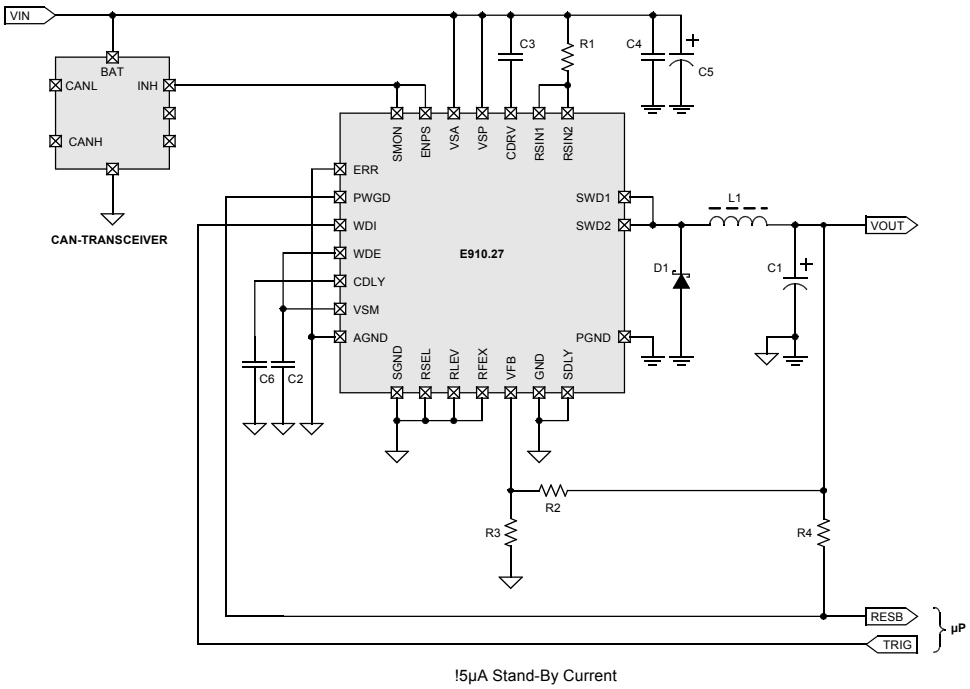


Figure 10.2-2: µP Power Supply Wake-Up by CAN-Transceiver

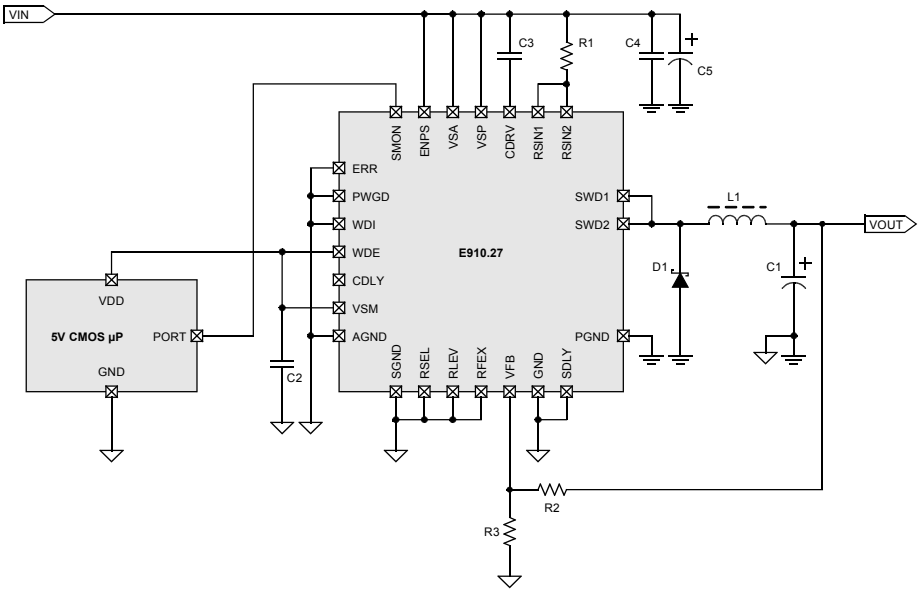


Figure 10.2-3: Main Power Supply Wake-Up by auxiliary CMOS Processor

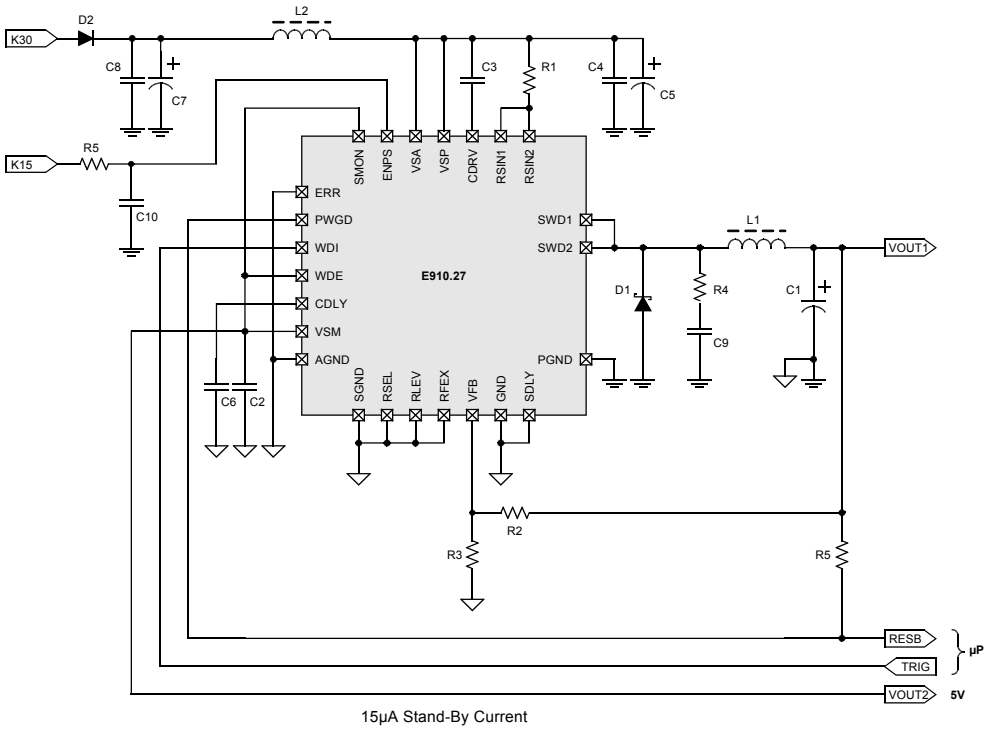


Figure 10.2-4: Discontinous Mode Automotive Power Supply

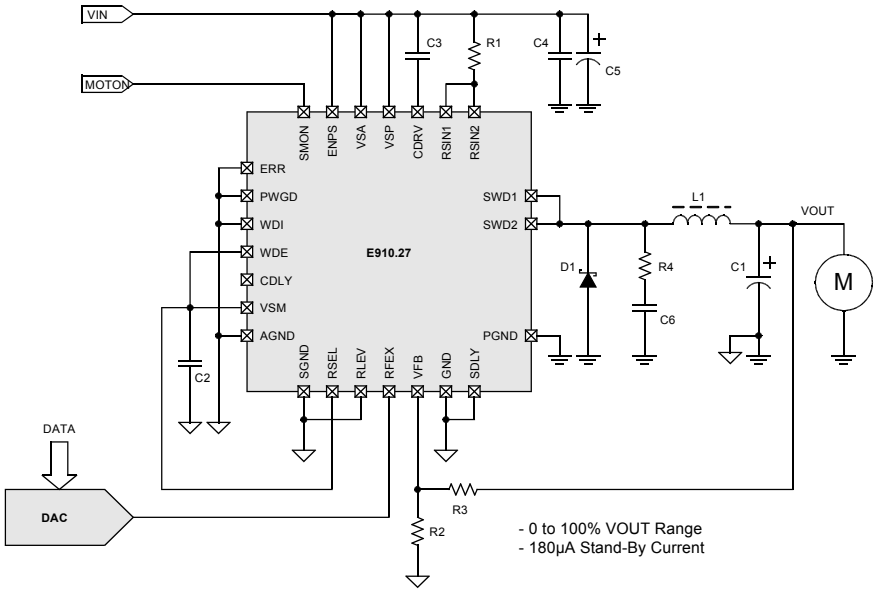


Figure 10.2-5: External programmable Power Amplifier

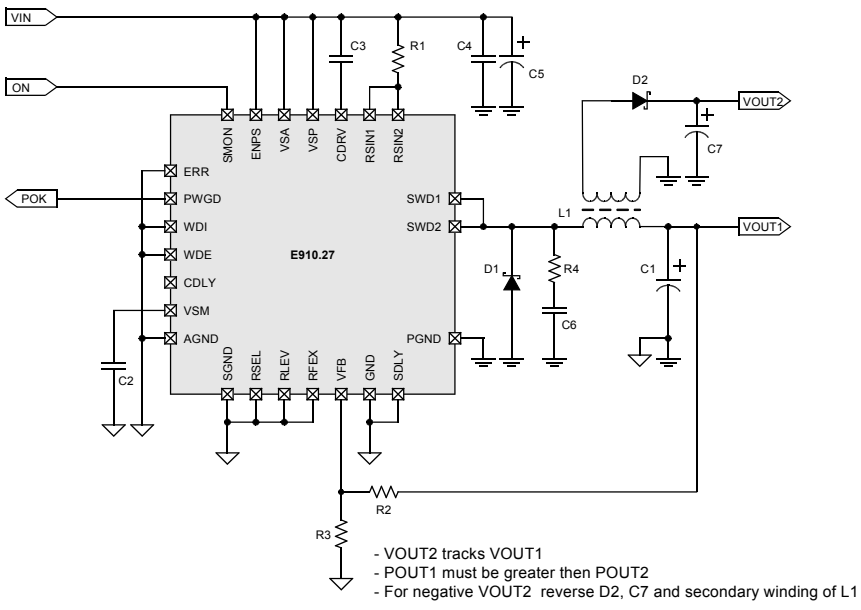


Figure 10.2-6: Step-Down Converter with tracking auxiliary Output

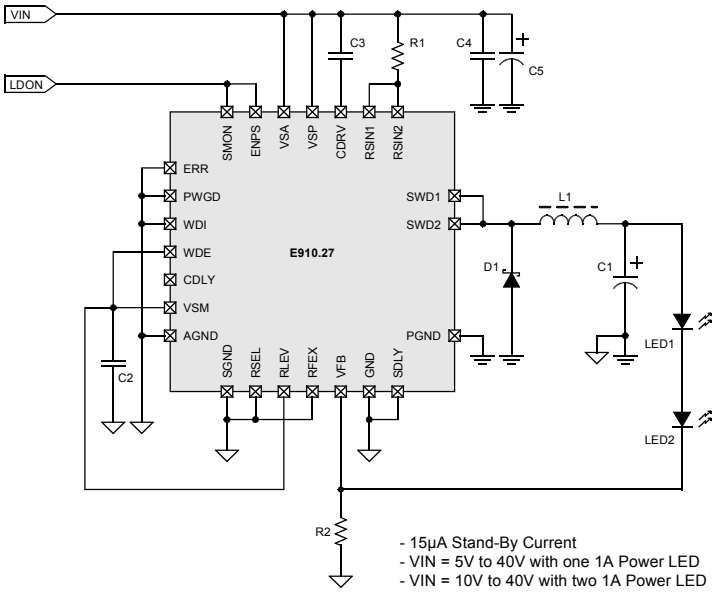


Figure 10.2-7: Extremely low Stand-By Current high efficiency 1A LED Driver

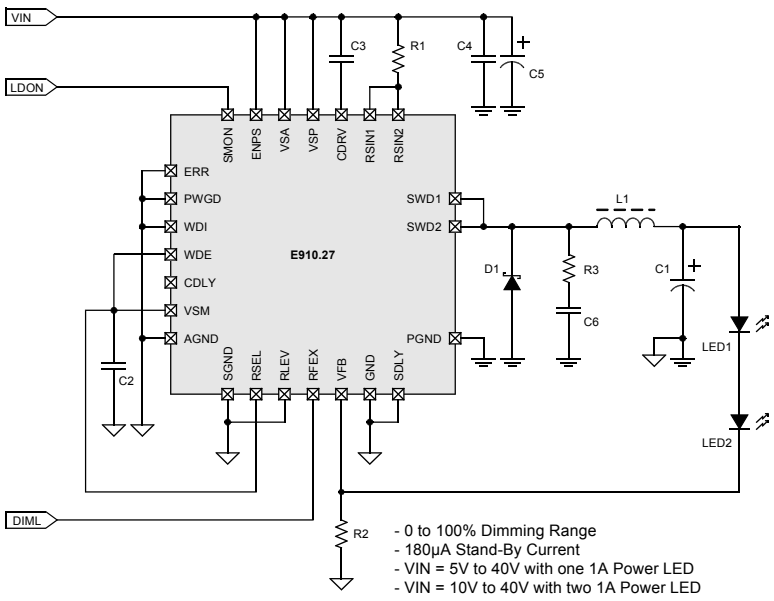


Figure 10.2-8: High efficiency Step-Down 1A LED Driver with Dimming

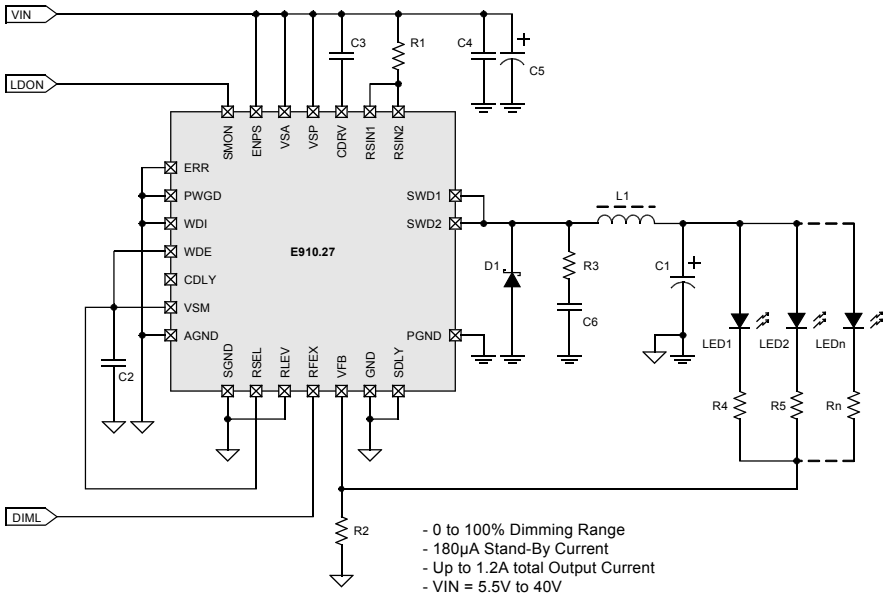


Figure 10.2-9: Dimmable high current LED Cluster Driver

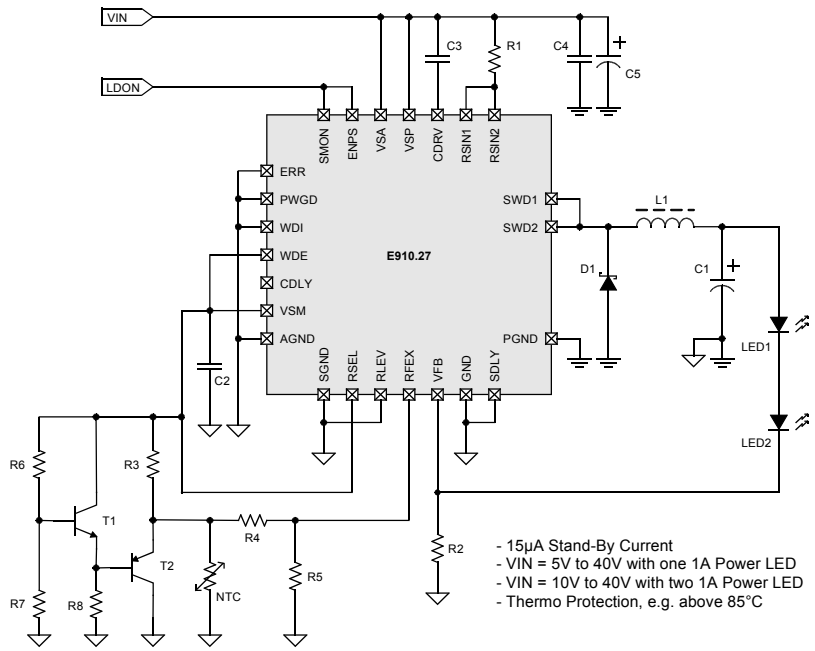


Figure 10.2-10: 1A LED Driver with temperature Protection

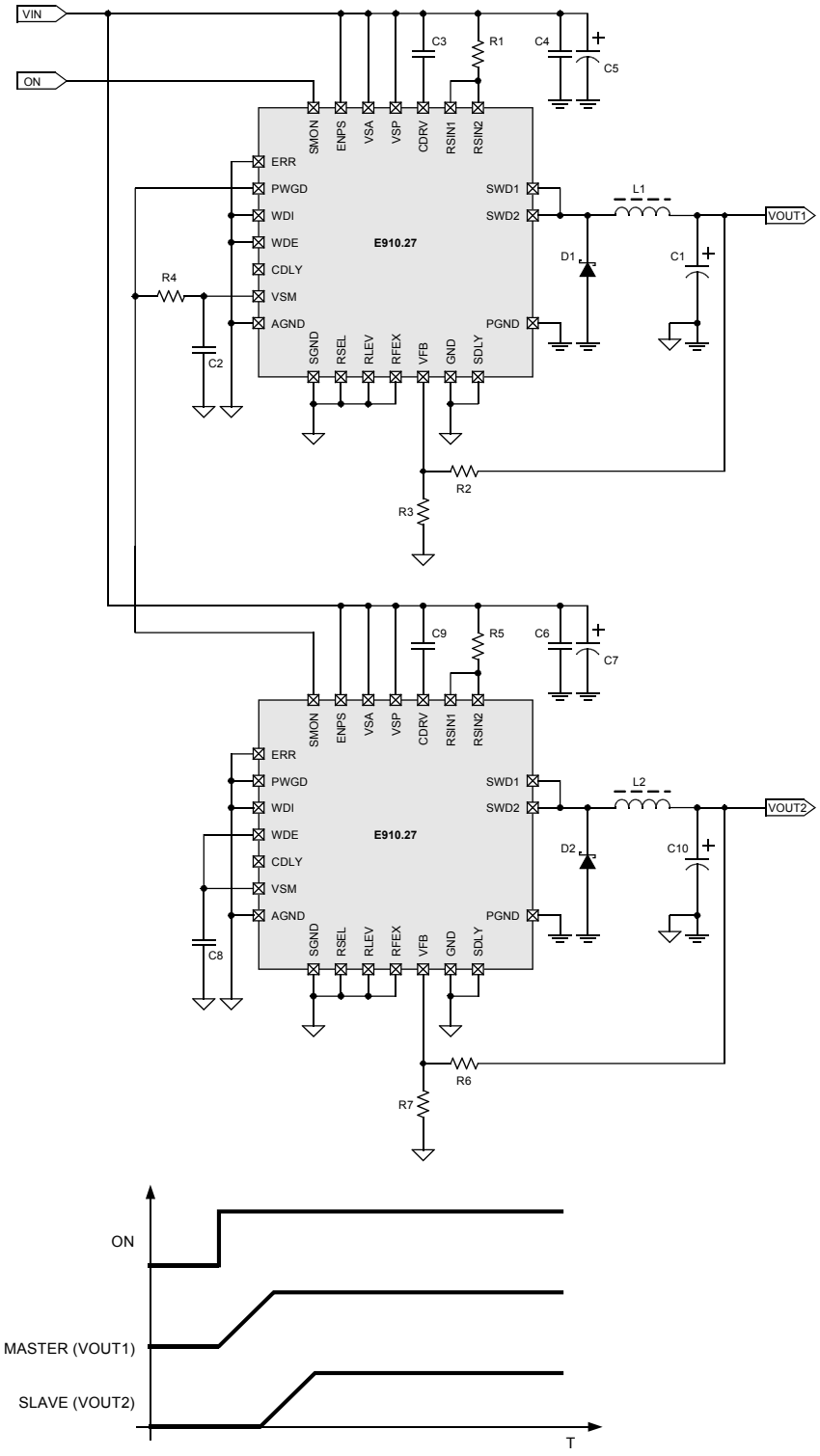


Figure 10.2-11: Power-Up Sequencing Example

11 Package

11.1 Marking

11.1.1 Top Side

ELMOS (Logo)
E 910.27A
XXX#YWW*@

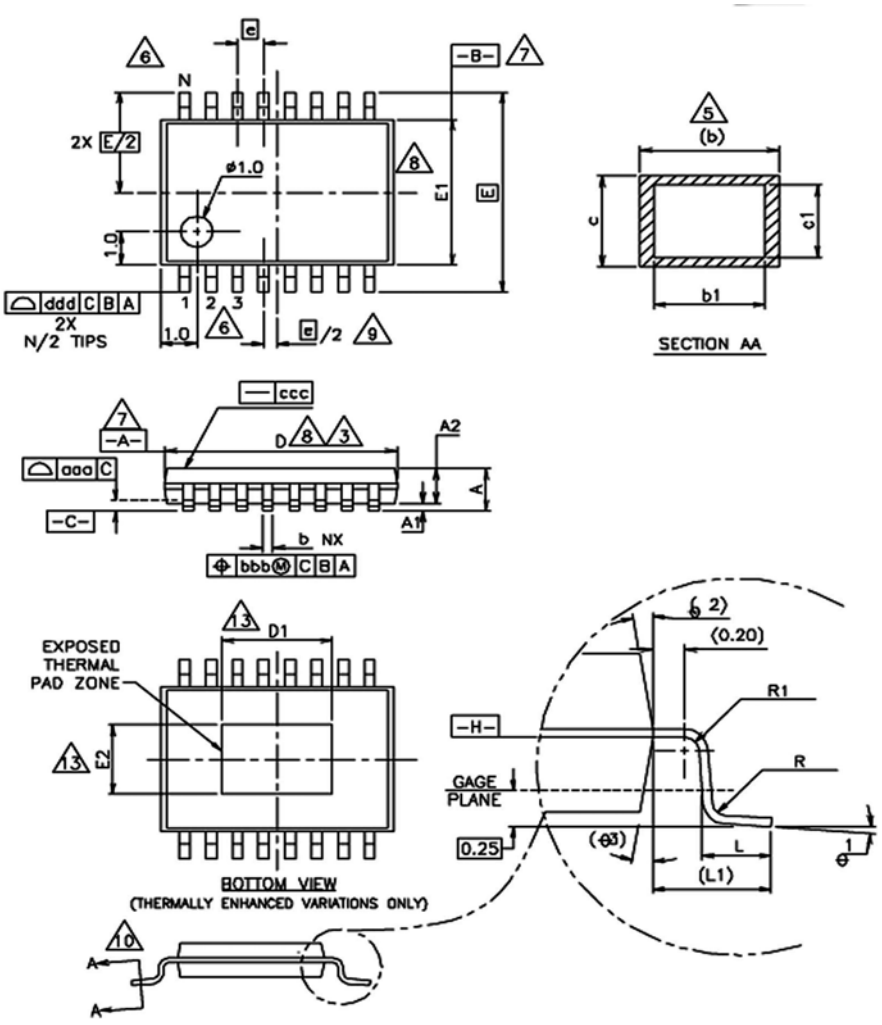
where

E / M / T	Volume Production / Prototype / Test Circuit
910.27	ELMOS Project Number
A	Version
XXX	Lot Number
#	Assembler Code
YWW	Year and Week of Fabrication
*	Mask Revision Number
@	ELMOS internal Marking

11.1.2 Bottom Side

No Marking

11.2 Package Dimensions



Thermally Enhanced Variation

Figure 11.2-1: Package Outlines of TSSOP24 ADT-1

SYMBOL	DIMENSION(MILLIMETERS) 0.65mm LEAD PITCH		
	MIN	NOM	MAX
A	---	---	1.10
A1	0.05	---	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	---	---
R1	0.09	---	---
b	0.19	---	0.30
b1	0.19	0.22	0.25
c	0.09	---	0.20
c1	0.09	---	0.16
θ1	0°	---	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
θ2	12° REF		
θ3	12° REF		

SYMBOL	VARIATION ADT-1 (Thermally Enhanced Variation)		
	MIN	NOM	MAX
D	7.70	7.80	7.90
D1	5.5 Ref		
E1	4.30	4.40	4.50
E2	3.0 Ref		
E	6.4 BSC		
e	0.65 BSC		
N	24		

12 General

12.1 ELMOS Documents

QM-Nr.: 07PL0009.XX Standard Qualifikations Plan

QM-Nr.: 07SP0001.XX Reliability Test Methods

QM-Nr.: 07VA0013.XX Reliability Testing

QM-Nr.: 07VA0005.XX Finalpart Release for Shipment

QM-Nr.: 07SP0028.XX Taping of Devices

13 Record of Revisions

Chapter	Rev.	Change and Reason for Change	Date	Released
-	1	Initial Revision	17.11.05	FJP
	2	Complete Rework		FJP

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